National Semiconductor

ADVANCE INFORMATION
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LM2502
Mobile Pixel Link (MPL) Transceiver

General Description

The LM2502 device is a dual link Transceiver that adapts existing CPU / video busses to a low power current-mode serial MPL link.

The Master Transceiver resides beside an application processor or baseband processor and translates a parallel bus from LVCMOS levels to serial MPL levels for transmission over a flex cable and PCB traces to the Slave Transceiver located near the display module.

Dual display support is provided for a primary and sub display through the use of two ChipSelect signals.

The Power_Down (PD*) input controls the power state of the MPL interface. When PD* is asserted on the Master, the MD1/0 and MC signals are powered down to save current.

The LM2502 implements the physical layer of the MPL Standard (MPL-0). The MPL logic layer is currently in definition.

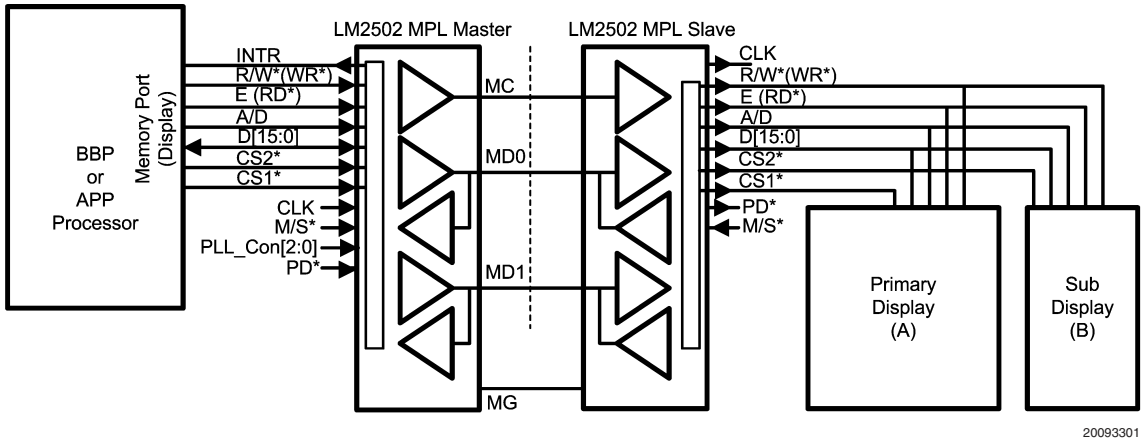
Features

- 320 Mbps Dual Link Raw Throughput
- MPL Physical Layer (MPL-0)
- Pin selectable Master / Slave mode
- Frequency Reference Transport
- Complete LVCMOS / MPL Translation
- CPU Interface Modes:
  — 16-bit data path
  — Intel or Motorola Interface
- Link power down mode reduces quiescent power under ~ 10 µA (actual TBD)
- Dual Display Support (CS1* & CS2*)
- Via-less MPL interconnect feature
- 3.0V Supply Voltage
- Interfaces to 1.7V to 3.3V Logic

System Benefits

- Small Interface
- Low Power
- Low EMI
- Frequency Reference Transport
- Intrinsic Level Translation

Typical Application Diagram

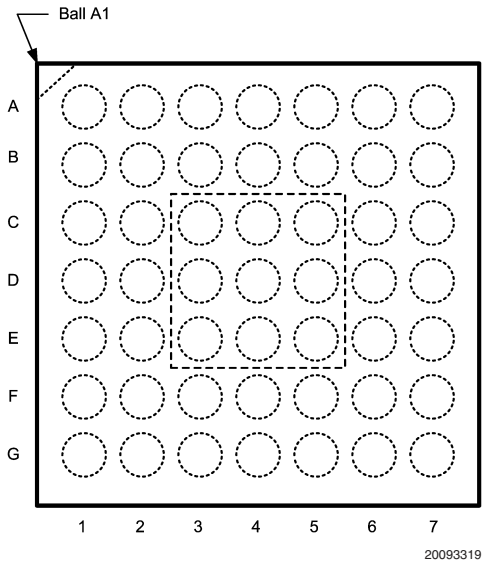


20093301

Ordering Information

NSID	Package Type	Package ID
LM2502GR	49(40) lead FBGA style, 4.0 X 4.0 X 1.0 mm, 0.5 mm pitch	GRA49A

Connection Diagram



TOP VIEW
(not to scale)

TABLE 1. Ball Assignment

Ball #	Master	Slave		Ball #	Master	Slave
A1	D0	D0		D5	-	-
A2	D1	D1		D6	V_{SScore}	V_{SScore}
A3	D2	D2		D7	V_{DDcore}	V_{DDcore}
A4	V_{DDA}	V_{DDA}		E1	D8	D8
A5	**INTR**	**NC**		E2	D9	D9
A6	**MD1**	**MD0**		E3	-	-
A7	MC	MC		E4	-	-
B1	D3	D3		E5	-	-
B2	D4	D4		E6	CS1*	CS1*
B3	D5	D5		E7	PLLCON2	*PLLCON2*
B4	V_{SSA}	V_{SSA}		F1	D10	D10
B5	M/S*	M/S*		F2	D11	D11
B6	Mode	Mode		F3	D12	D12
B7	**MD0**	**MD1**		F4	V_{SSIO}	V_{SSIO}
C1	D6	D6		F5	MF0	MF0
C2	D7	D7		F6	PLLCON1	*PLLCON1*
C3	-	-		F7	PD*	PD*
C4	-	-		G1	D13	D13
C5	-	-		G2	D14	D14
C6	CS2*	CS2*		G3	D15	D15
C7	MF1	MF1		G4	V_{DDIO}	V_{DDIO}
D1	V_{DDIO}	V_{DDIO}		G5	A/D	A/D
D2	V_{SSIO}	V_{SSIO}		G6	PLLCON0	*PLLCON0*
D3	-	-		G7	CLK	CLK
D4	-	-		Table is for REV B ES Silicon, see note.		

Note:
ES units REV A does not implement the swap function – A6 = MD1, B7 = MD0.
ES units REV B implements the swap function – A6 = MD0, B7 = MD1.

Pin Descriptions

Pin Name	No. of Pins	I/O, Type	Description	
			Master	Slave
MPL SERIAL BUS PINS				
MD[1:0]	2	IO, MPL	MPL Data Line Driver/Receiver	MPL Data Receiver/Line Driver
MC	1	IO, MPL	MPL Clock Line Driver	MPL Clock Receiver
CONFIGURATION/PARALLEL BUS PINS				
M/S*	1	I, LVCMOS	Master/Slave* High for Master Mode	Master/Slave* Low for Slave Mode
PD*	1	IO, LVCMOS	Power_Down* Input, H = Active L = Power Down Mode	Power_Down* Output, H = Link Active L = Link in Power_Down Mode
MF0 (E or RD*)	1	IO, LVCMOS	Multi-function Input Zero (0): If MODE = 0 (MOT mode) E input pin, data is latched on E High-to-Low transition or E may be static High and Data is latched on CS* Low-to-High edge If MODE = 1 (Intel mode) Read Enable input pin, active low. Read data is driven when both RD* and CS* are Low.	Multi-function Output Zero (0): If MODE = 0 (MOT mode) E output pin, static High. If MODE = 1 (Intel mode) Read Enable output pin, active Low.
MF1 (R/W* or WR*)	1	IO, LVCMOS	Multi-function Input One (1): If Mode = 0 (MOT mode) Read/Write* pin, Read High, Write* Low If Mode = 1 (Intel mode) Write* enable input pin, active Low. Write data is latched on the Low-to-High transition of either WR* or CS* (which ever occurs first).	Multi-function Output One (1): If Mode = 0 (MOT mode) Read/Write* pin, Read High, Write* Low If Mode = 1 (Intel mode) Write* enable output pin, active Low.
CS1*	1	IO, LVCMOS	ChipSelect1* – Input H = Ignored L = Active	ChipSelect1* – Output H = Ignored L = Active
CS2*	1	IO, LVCMOS	ChipSelect2* – Input H = Ignored L = Active	ChipSelect2* – Output H = Ignored L = Active
A/D (RS or A0)	1	IO, LVCMOS	Address/Data – Input H = Data L = Address (Command)	Address/Data – Output H = Data L = Address (Command)
D[15:0]	16	IO, LVCMOS	Data Bus – Inputs/Outputs	Data Bus – Outputs/Inputs
INTR	1	O, LVCMOS	INTR is asserted when the read data is ready and de-asserted upon a second CPU Read cycle.	No Connect – leave open on board
CLK	1	IO, LVCMOS	Clock Input	Clock Output (Frequency Reference) – no phase relationship to data – frequency reference only.
Mode	1	I, LVCMOS	Mode Input Pin High = Intel Mode, Low = MOT Mode	Mode Input Pin High = Intel Mode, Low = MOT Mode
PLL_CON [2:0]	3	I, LVCMOS	PLL Configuration Input Pins	Clock Divisor Configuration Input Pins

Pin Descriptions (Continued)

Pin Name	No. of Pins	I/O, Type	Description	
			Master	Slave
POWER/GROUND PINS				
V_{DDA}	1	Power	Power Supply Pin for the MPL Interface. 2.9V to 3.3V	
V_{SSA}	1	Ground	Ground Pin for the MPL Interface, also known as MG (MPL Ground)	
V_{DDcore}	1	Power	Power Supply Pin for the digital core. 2.9V to 3.3V	
V_{SScore}	1	Ground	Ground Pin for the digital core.	
V_{DDIO}	2	Power	Power Supply Pin for the parallel interface. 1.7V to 3.3V	
V_{SSIO}	2	Ground	Ground Pin for the parallel interface.	

Note:
I = Input, O = Output, IO = Input/Output, $V_{DDIO} \leq V_{DD}$ ($V_{DDA} = V_{DDcore}$). Do not float input pins.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DDA})	−0.3V to +TBDV
Supply Voltage (V_{DD})	−0.3V to +TBDV
Supply Voltage (V_{DDIO})	−0.3V to +TBDV
LVCMOS Input/Output Voltage	−0.3V to (V_{DDIO} +0.3V)
MPL Input/Output Voltage	TBD
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature Soldering, 4 Seconds	+260˚C
ESD Ratings:	
HBM, 1.5 kΩ, 100pF	≥±2 kV
EIAJ, 0Ω, 200 pF	≥±200V
Maximum Package Power Dissipation Capacity at 25˚C	
TBD Package	TBD W
Derate TBD Package above 25˚C	TBD mW/˚C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage				
V_{DDA} to V_{SSA}	2.9	3.0	3.3	V
V_{DDcore} to V_{SScore}	2.9	3.0	3.3	V
V_{DDIO} to V_{SSIO}	1.7		3.3	V
Clock Frequency	8		20	MHz
Ambient Temperature	0	25	70	˚C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
MPL							
I_{OH}	Logic High Current			2.8 I_B	3.0 I_B	3.3 I_B	µA
I_{OMS}	Mid Scale Current				2.0 I_B		µA
I_{OL}	Logic Low Current			0.8 I_B	1.0 I_B	1.2 I_B	µA
I_B	Current Bias				I_B		µA
LVCMOS (1.7V to 3.3V Operation)							
V_{IH}	Input Voltage High Level			0.7 V_{DDIO}		V_{DDIO} +0.3	V
V_{IL}	Input Voltage Low Level			−0.3		0.3 V_{DDIO}	V
I_{IH}	Input Current High Level			−1	0	+1	µA
I_{IL}	Input Current Low Level			−1	0	+1	µA
V_{OH}	Output Voltage High Level	I_{OH} = −2 mA		0.8 V_{DDIO}			V
V_{OL}	Output Voltage Low Level	I_{OL} = 2 mA				0.2 V_{DDIO}	V
I_{OS}	Output Short-Circuit Current	V_{OUT} = 0V		TBD	TBD	TBD	mA
I_{OZ}	Output TRI-STATE Current			−5		+5	µA
V_{CL}	Clamp Voltage				TBD	−1.5	V
SUPPLY CURRENT							
I_{CC}	Total Supply Current — Enabled	Master	V_{DDIO}		TBD	TBD	µA
			V_{DD}/V_{DDA}		TBD	TBD	mA
		Slave	V_{DDIO}		TBD	TBD	µA
			V_{DD}/V_{DDA}		TBD	TBD	µA
I_{CCZ}	Supply Current — Disable	Power_Down Mode			TBD	TBD	µA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
PARALLEL BUS TIMING							
t_{SET}	Set Up Time	Inputs		5	2		ns
t_{HOLD}	Hold Time			5	2		ns
t_{RISE}	Rise Time	Outputs,			4	TBD	ns
t_{FALL}	Fall Time	C_L = 15 pF			4	TBD	ns
t_1			*Figures 14, 15, 16, 17 Table 4. WRITE—MOT 6800 µP Interface Parameters, Table 5. READ—6800 µP Interface Parameters, Table 6. READ—80xx µP Interface Parameters, Table 7. READ—Intel µP Interface Parameters*				
t_2							
t_3							
t_4							
t_5							
t_6							
t_7							
t_8							
t_9							
t_{10}							
t_{11}							
t_{12}							
t_{13}							
t_{14}							
t_{15}							
SERIAL BUS TIMING							
t_{DVBC}		Master-to-Slave		TBD			ns
t_{DVAC}				TBD			ns
t_{RVAC}		Slave-to-Master		TBD			ns
POWER UP TIMING							
t_1	PD* to MC L-H (Master)		*Figure 9*				
t_2	MC Pulse Width HIGH (Master)						
t_3	MC H-L to Idle State (Master)						
t_4	PD*-Out Delay (Slave)						
t_0	Master PLL Lock Time				1	TBD	ms
MPL POWER OFF TIMING							
t_{PAZ}	Disable Time to Power Down	*Figure 10*				TBD	µs
SLAVE CLOCK OUTPUT							
F	Clock Output Frequency						MHz
CLK_{DC}	Duty Cycle				50		%
t_T	Transition Time	C_L = 7 pF					ns

Input Timing Requirements

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MASTER R EFERENCE CLOCK (CLK)						
f	Clock Frequency		8		20	MHz
t_{CP}	Clock Period					ns
CLK_{DC}	Clock Duty Cycle		45	50	55	%
t_T	Clock Transition Times (Rise or Fall, 10%–90%)				6	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for VDDIO = 1.8V and VDD = VDDA = 3.0V and T_A = 25˚C.

Note 3: Current into a device pin is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to Ground unless otherwise specified.

Timing Diagrams

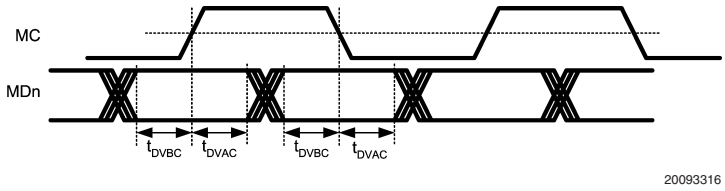


FIGURE 1. Serial Data Valid—Master to Slave

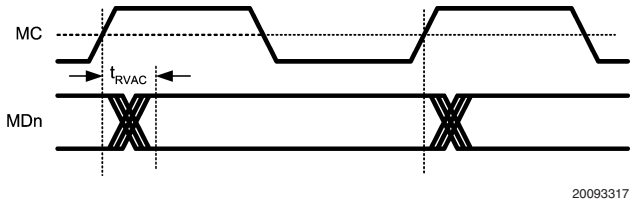


FIGURE 2. Serial Data Valid—Slave to Master

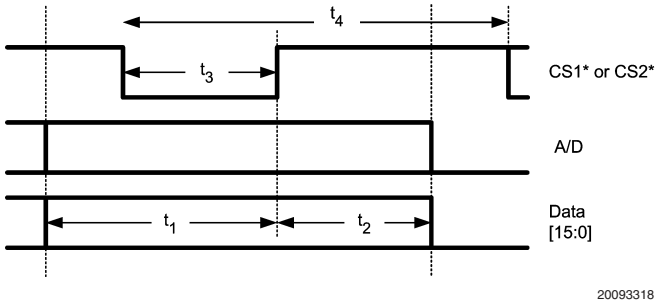


FIGURE 3. Slave Output Timing

Application Information

The LM2502 provides a swap function of MPL MD lines depending upon the state of the M/S* pin. This facilitates a straight through MPL interface design eliminating the needs for via and crossovers as shown on *Figure 4*. See also Connection Diagram and *Table 1. Ball Assignment*.

Feature is supported on ES Rev B and Production Silicon.

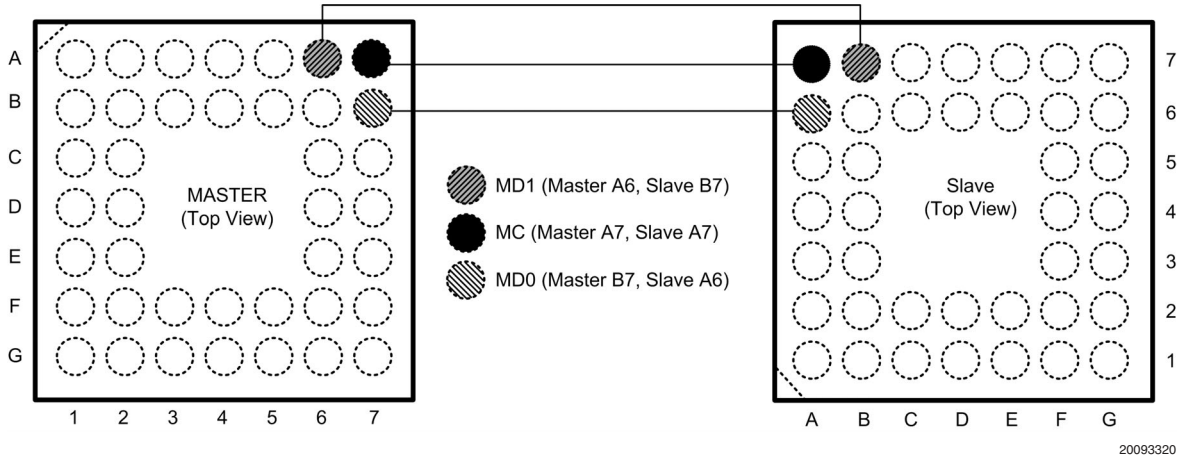


FIGURE 4. MPL Interface Layout

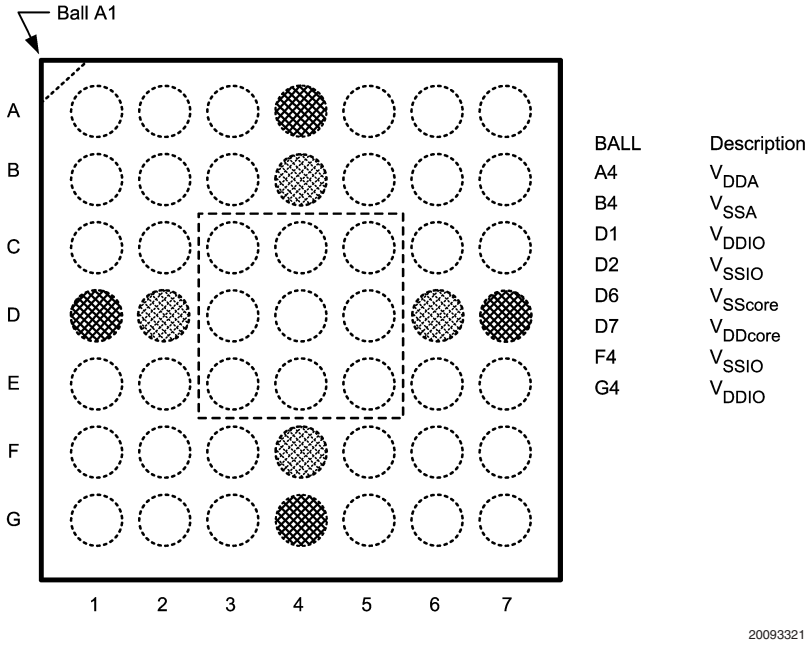


FIGURE 5. LM2502 PWR (V_{DD}) and GND (V_{SS}) Balls

Functional Description

BUS OVERVIEW

The LM2502 is a dual link Transceiver configurable part that supports a 16-bit CPU (68xx or 80xx) style interface. The MPL physical layer is purpose-built for an extremely low power and low EMI data transmission while requiring the fewest number of signal lines. No external line components are required, as termination is provided internal to the MPL receiver. A maximum raw throughput of 320 Mbps is possible. When the protocol overhead is taken into account, a maximum data throughput of 256 Mbps is possible. The MPL interface is designed for use with common 50Ω lines using standard materials and connectors. Lines may be microstrip or stripline construction. Total length of the interconnect is expected to be less than 0.1 meters.

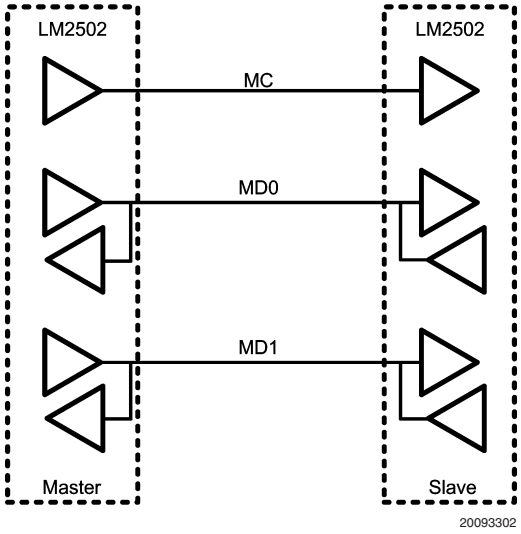


FIGURE 6. MPL Point-to-Point Bus

SERIAL BUS TIMING

Data valid is relative to both edges as shown in *Figure 7*. Data valid is specified as: Data Valid before Clock, Data Valid after Clock, and Skew between data lines is TBD.

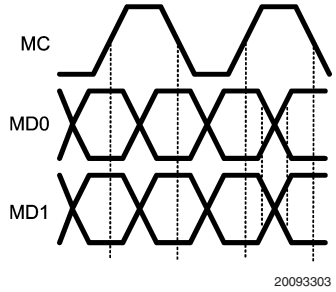


FIGURE 7. Dual Link Timing (WRITE)

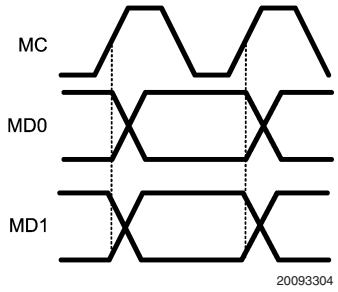


FIGURE 8. Dual Link Timing (READ)

SERIAL BUS PHASES

There are four bus phases on the MPL serial bus. These are determined by the state of the MC and MD lines. The MPL bus phases are shown in *Table 2. Link Phases*.

TABLE 2. Link Phases

Name		MC State	MDn State	Phase Description	Pre-Phase	Post-Phase
OFF (O)		0	0	Link is Off	A, I or LU	LU
IDLE (I)		A	L	Data is Static (Low)	A or LU	A or O
Active (A)	Data Out WRITE	A	X	Data Out (Write) — includes command, Data Out Phases	LU, A, or I	A, I, or O
	Data In READ	A	X	Data In (Read) — includes command, TA', Data In, and TA" phases	LU, A, or I	A, I, or O
LINK-UP (LU)	Master	H	-	Master initiated Link-Up	O	A, I, or O

Notes on MC/MD Line State:
0 = no current (off)
L = Logic Low — The higher level of current on the MC and MD lines
H = Logic High — The lower level of current on the MC and MD lines
X = Low or High
A = Active Clock

Functional Description (Continued)

SERIAL BUS START UP TIMING

In the Serial Bus OFF phase, Master transmitters for MD0, MD1 and MC are turned off such that zero current flows over the MPL lines. In addition, both the Master and the Slave are internally held in a low power state. When the Master's PD* input pin is de-asserted (driven High) the Master enables its PLL and waits for enough time to pass for its PLL to lock. After the Master's PLL is locked (t0 = 4,096 CLK Cycles), the Master will perform an MPL start up sequence.

The MPL start up sequence gives the Slave an opportunity to optimize the current sources in its transceiver and to emerge from its low power state. The Master begins the sequence by driving the MC line logically Low for 11 CLK cycles (t1). During this part of the sequence the Slave's transceiver samples the MC current flow and adjusts itself to interpret that amount of current as a logical Low. Next the Master drives the MC line logically HIGH for 11 CLK cycles (t2). On the Low-to-High transition of the MC – point B – the Slave latches the current source configuration. This optimized configuration is held as long as the MPL remains up. Next, the Master drives both the MC and the MD lines to a logical Low for another 11 CLK cycles (t3), after which it begins to toggle the MC line at a rate determined by its PLL Configuration pins. The Master will continue to toggle the MC line as long as its PD* pin remains de-asserted (High). At this point the MPL bus may remain in IDLE phase, enter the ACTIVE phase or return to the OFF phase. Data transmission is not gated by the Slave PD* output signal. Active data will occur at the Slave output latency delays (Master + line + Slave) after the data is applied to the Master input. Possible start points are shown by the "C" arrow in *Figure 9*.

After seven subsequent MC cycles the Slave will start toggling its CLK pin at a rate configured by its CLK Divisor pins. The Slave then waits an additional 17 CLK cycles before de-asserting its PD* Output pin (t4).

In the *Figure 9* example, an IDLE bus phase is shown until point C, after which the bus is active and the High start bit on MD initiates the transfer of information.

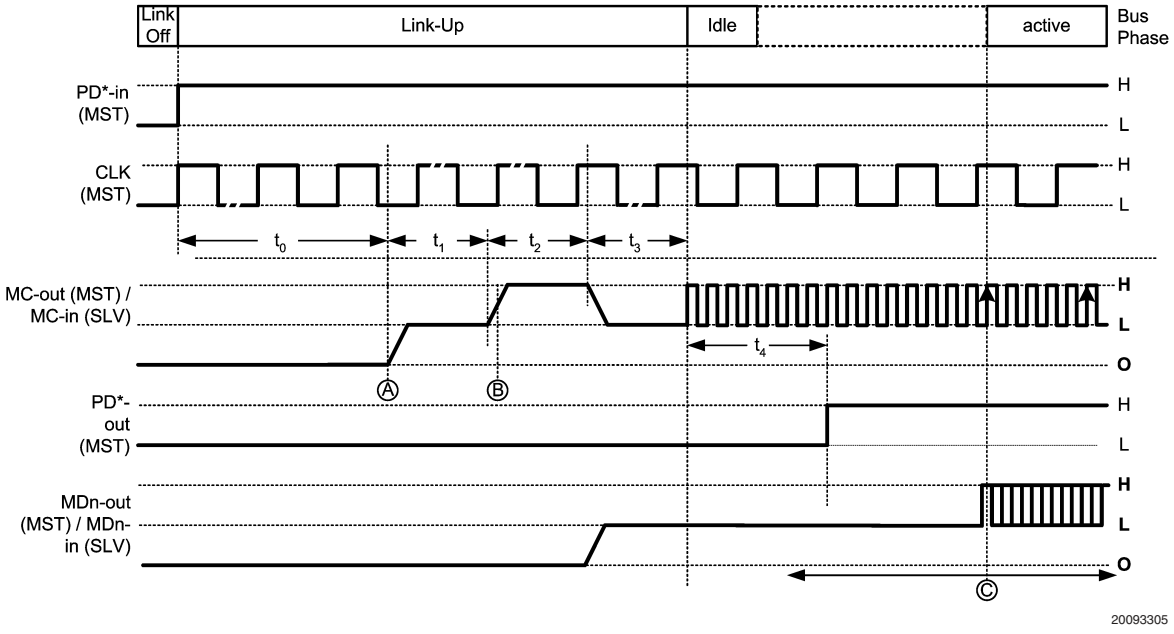


FIGURE 9. Bus Power Up Timing

OFF PHASE

In the OFF phase, both Master and Slave MPL transmitters are turned off with zero current flowing on the MC and MD lines. *Figure 10* shows the transition of the MPL bus into the OFF phase. If an MPL line is driven to a logical Low (high current) when the OFF phase is entered it may temporarily pass through as a logical High (low current) before reaching the zero line current state.

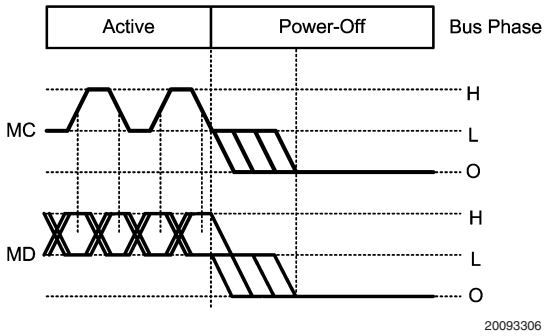


FIGURE 10. Bus Power Down Timing

Functional Description (Continued)

The link may be powered down by asserting the Master's PD* input pin (Low). This causes the Master to immediately put the link to the OFF Phase and internally enter a low power state. When the Slave detects a lack of current flow on the MC it will immediately also enter a low power state and assert its PD* output pin (Low). To avoid loss of data the Master's PD* input should only be asserted after the MPL bus has been in the IDLE state for at least 5 MC clock cycles. This gives the Slave enough time to complete any write operations received from the MPL bus.

CPU INTERFACE COMPATIBILITY

The CPU Interface mode provides compatibility between a CPU Interface and a small form factor (SFF) Display or other fixed I/O port application. Two options are allowed:

TABLE 3. Modes

Mode	Description
0	MOT 68xx Interface (E, R/W*), 16-bit support
1	Intel 80xx Interface (WR*, RD*), 16-bit support

It is not required that both the Master and the Slave to be configured in the same mode. For example the Master may be configured as an 80xx interface while the Slave is configured for an 68xx interface.

Control information is carried over both MD lines. MD0 carries the D0–7 data bits while MD1 the D8–15 data bits. See *Figure 11*.

WRITE TRANSACTION

The WRITE transaction consists of two MC edges of control information followed by 8 MC edges of write data. Since WRITE transactions transfer information on both edges of MC it takes 5 MC cycles to complete a write transaction. The MD0 line carries the Start bit (High), the A/D (Address/Data) bit and then the data payload of 8 bits (D0–7). The MD1 line carries the R/W* bit (Read/Write*), the CS1/2 bit and then the data payload of 8 bits (D8–15). The data payload is sent least significant bit (LSB) first. The CS1/2 bit denotes which Chipset pin was active. CS1/2 = HIGH designates that CS1* is active (Low). CS1/2 = LOW designates that CS2* is active (Low). CS1* and CS2* LOW is not allowed.

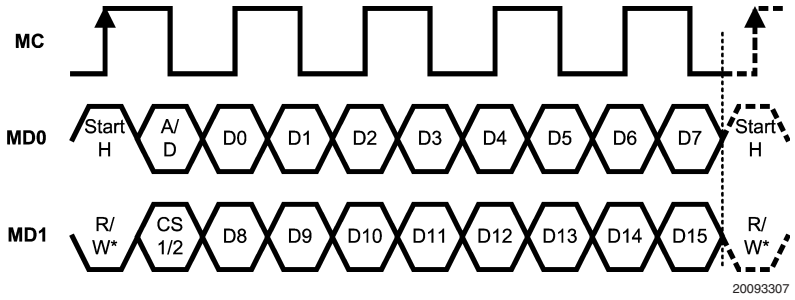


FIGURE 11. Dual MD Link WRITE Transaction

READ TRANSACTION

The READ transaction is variable in length. It consists of four sections.

In the first section the Master sends a READ_Command to the slave. This command is sent in a single MC cycle (2 edges) and uses a similar format to the 1st cycle of the WRITE transaction. The MD0 line carries the Start bit (High) and the A/D (Address/Data) bit. The MD1 line carries the R/W* bit (High for reads) and the CS1/2 bit.

In the second section (TA') the MD lines are turned around, such that the Master becomes the receiver and Slave becomes the transmitter. The Slave must drive the MD lines low by the 14th clock edge. It may then idle the line at the Logic Low state or drive the line High to indicate that read data transmission is starting. This ensures that the MD lines are a stable LOW state and that the Low-to-High transition of the "Start" bit is seen by the Master.

Functional Description (Continued)

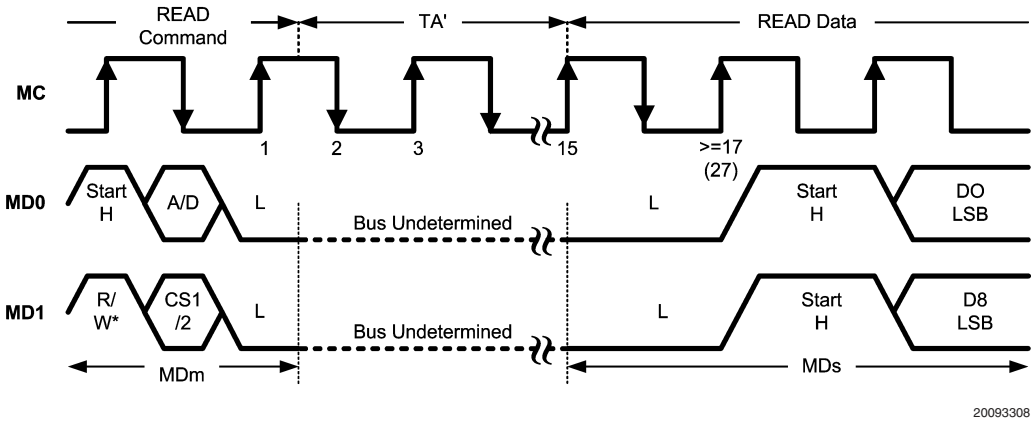


FIGURE 12. READ_Command and TA'

The third section consists of the transfer of the read data from the Slave to the Master. Note that the READ_Data operates on single-edge clocking (Rising Edge ONLY). Therefore the back channel data signaling rate is ½ of the forward channel (Master-to-Slave direction). When the Slave is ready to transmit data back to the Master it drives the MD lines High to indicate start of read data, followed by 8 MC cycles of the actual read data payload. As in the WRITE command MD0 carries D0–7 and MD1 carries D8–5.

The fourth and final section (TA") occurs after the read data has been transferred from the Slave to the Master. In the fourth section the MD lines are again turned around, such that the Master becomes the transmitter and the Slave becomes the receiver. The Slave drives the MD lines Low for 1 bit with and then turns off. The MD lines are off momentarily to avoid driver contention. The Master then drives the MD line Low for 1 bit time and then idles the bus until the next transaction is sent.

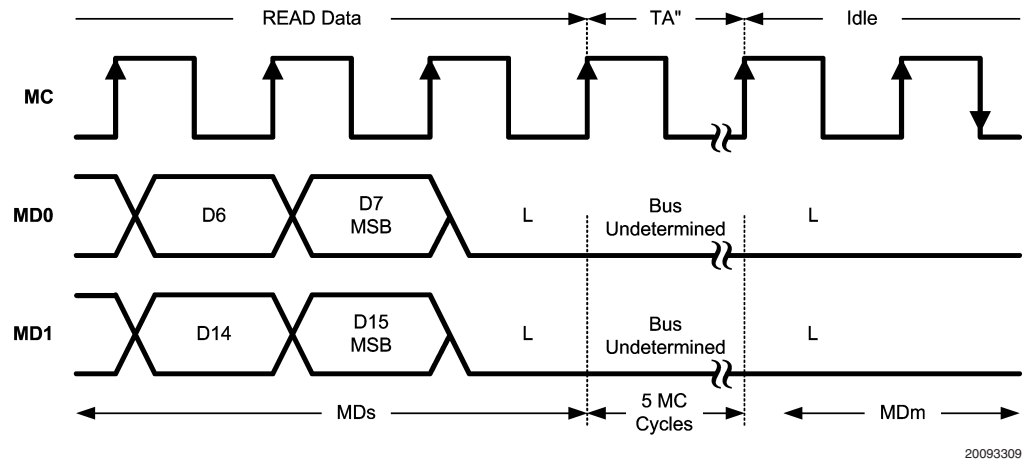


FIGURE 13. READ_Data and TA"

Functional Description (Continued)

CPU MODE — WRITE — MOT68xx

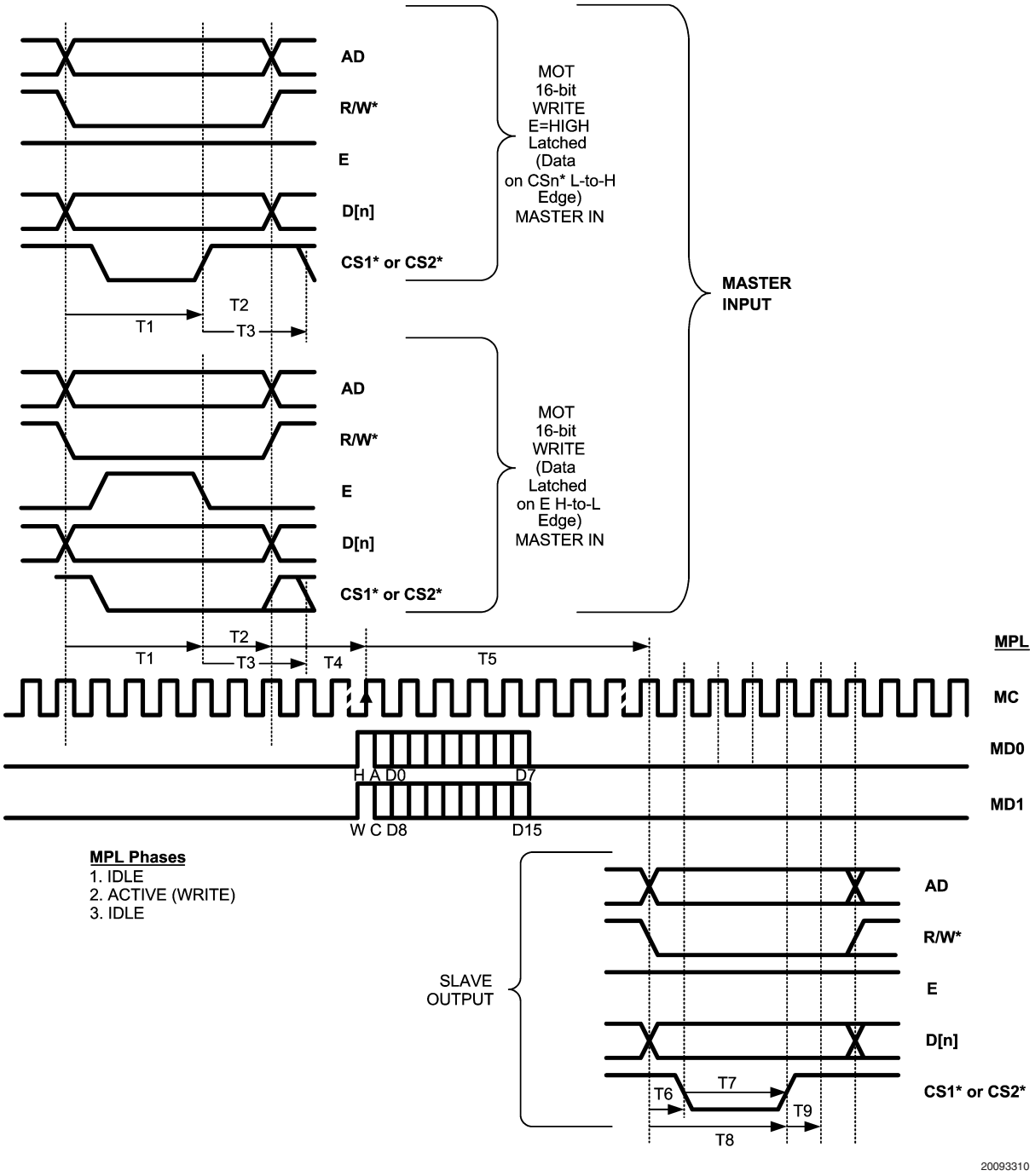


FIGURE 14. WRITE — MOT 6800 µP Interface

Functional Description (Continued)

TABLE 4. WRITE—MOT 6800 µP Interface Parameters

No.		Parameter	Min	Typ	Max	Units
T1	MasterIN	Data Setup Time before ChipSelect* Low-High (or E High-Low)	TBD	3.6		ns
T2	MasterIN	Data Hold after ChipSelect* Low-High (or E High-Low)	0	TBD		ns
T3	MasterIN	ChipSelect* Recovery Time		TBD		MC Cycles
T4	Master	Master Latency		4		MC Cycles
T5	Slave	Slave Latency		8		MC Cycles
T6	SlaveOUT	Data Valid before ChipSelect* High-Low		1		MC Cycles
T7	SlaveOUT	CS* Low Pulse Width		3		MC Cycles
T8	SlaveOUT	Data Valid before ChipSelect* Low-High		4		MC Cycles
T9	SlaveOUT	Data Valid after ChipSelect* Low-High		1		MC Cycles

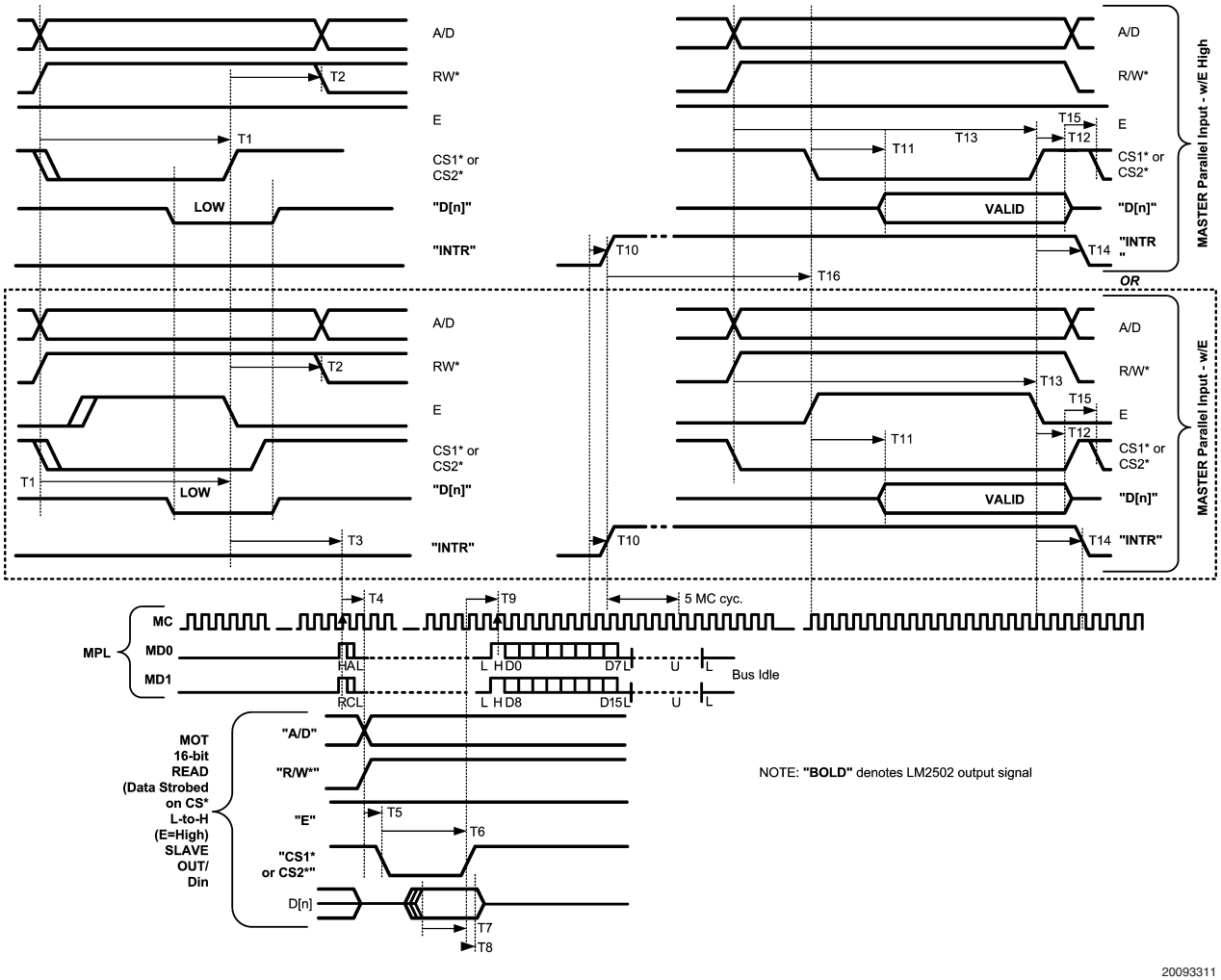


FIGURE 15. READ—6800 µP Interface

Functional Description (Continued)

TABLE 5. READ—6800 µP Interface Parameters

No.		Parameter	Min	Typ	Max	Units
T1	MasterIN	Set Up Time		3.6		ns
T2	MasterIN	Hold Time		0		ns
T3	Master	Master Latency		4		MC Cycles
T4	Slave	Slave Latency		5		MC Cycles
T5	Slave	ChipSelect* Delay		1		MC Cycles
T6	Slave	ChipSelect Low Pulse Width		6		MC Cycles
T7	Slave	Data Set Up Time		3.6		ns
T8	Slave	Data Hold Time		0		ns
T9	Slave	Slave Read Latency		6		MC Cycles
T10	Master	INTR Delay		1		MC Cycles
T11	Master	Data Delay		18.6		ns
T12	MasterOUT	Data Valid after Strobe		TBD		ns
T13	MasterOUT	CS* or E active pulse width	3.6			ns
T14	MasterOUT	INTR De-assert		4		MC Cycles
T15	MasterOUT	Recovery Time		TBD		MC Cycles
T16	MasterOUT	INTR Response	0			MC Cycles

For the MOT CPU 68xx mode, the Master accepts data on the CS* Low-to-High transition or the E High-to-Low transition, which ever come first. The Slave output only uses the CS* pin for data strobe/latch, as the E signal is held constantly High.

Functional Description (Continued)

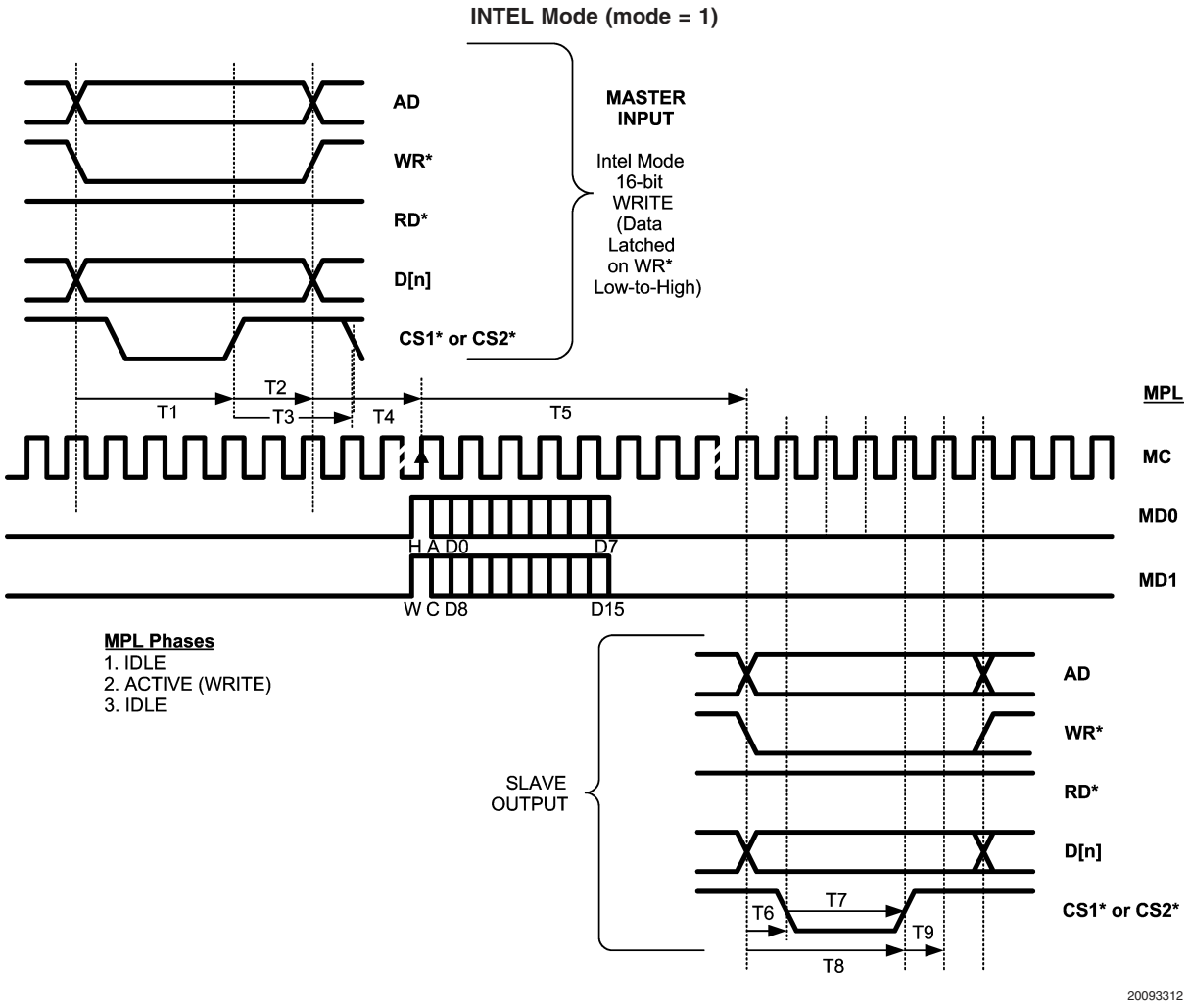


FIGURE 16. WRITE—80xx µP Interface

TABLE 6. READ—80xx µP Interface Parameters

No.		Parameter	Min	Typ	Max	Units
T1	MasterIN	Data Setup before ChipSelect* High		3.6		ns
T2	MasterIN	Data Hold after ChipSelect* High	0	TBD		ns
T3	MasterIN	ChipSelect* Recovery Time		TBD		ns
T4	Master	Master Latency		4		MC Cycles
T5	Slave	Slave Latency		8		MC Cycles
T6	SlaveOUT	Data Valid before ChipSelect* High-to-Low		1		MC Cycles
T7	SlaveOUT	CS* Pulse Width Low		3		MC Cycles
T8	SlaveOUT	Data Valid before ChipSelect* Low-to-High		4		MC Cycles
T9	SlaveOUT	Data Valid after ChipSelect* Low-to-High		1		MC Cycles

Functional Description (Continued)

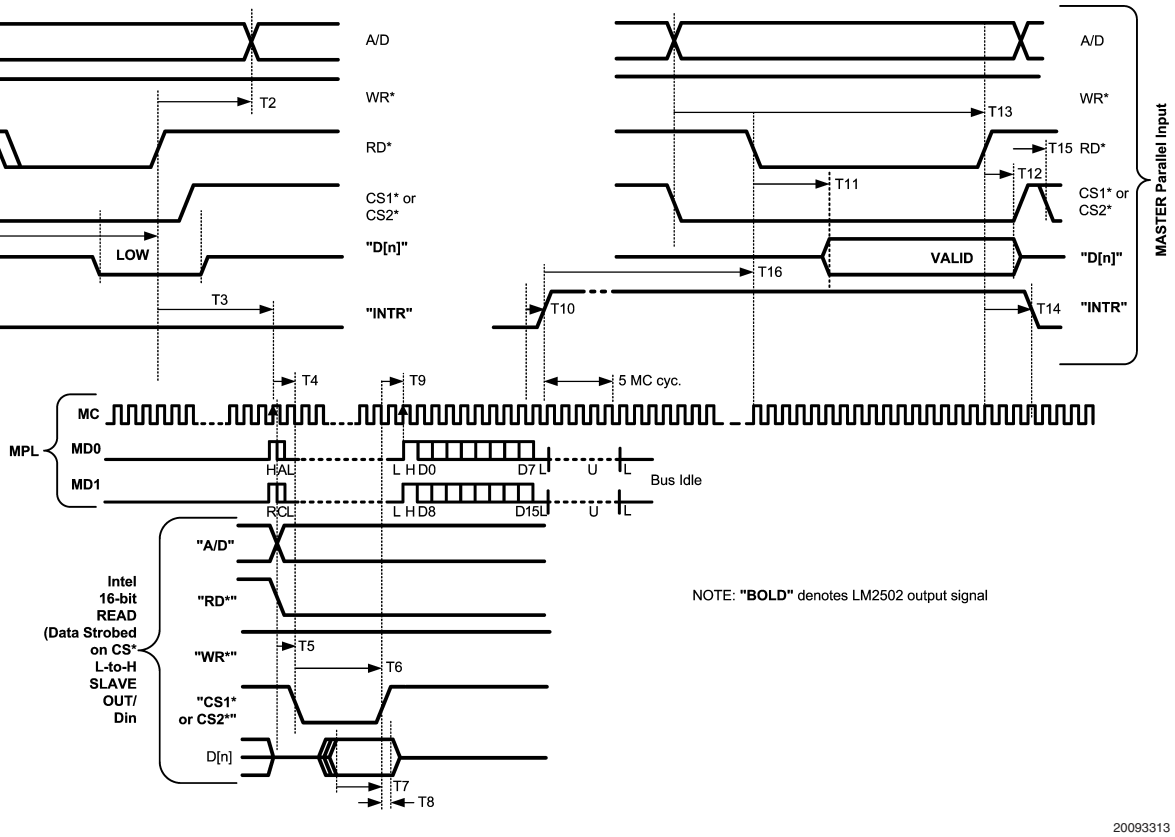


FIGURE 17. READ—INTEL µP Interface

TABLE 7. READ—Intel µP Interface Parameters

No.		Parameter	Min	Typ	Max	Units
T1	MasterIN	Set Up Time		3.6		ns
T2	MasterIN	Hold Time		0		ns
T3	Master	Master Latency		4		MC Cycles
T4	Slave	Slave Latency		5		MC Cycles
T5	Slave	ChipSelect* Delay		1		MC Cycles
T6	Slave	ChipSelect Low Pulse Width		6		MC Cycles
T7	Slave	Data Set Up Time		3.6		ns
T8	Slave	Data Hold Time		0		ns
T9	Slave	Slave Read Latency		6		MC Cycles
T10	Master	INTR Delay		1		MC Cycles
T11	Master	Data Delay		18.6		ns
T12	MasterOUT	Data Valid after Strobe		TBD		ns
T13	MasterOUT	RD* active pulse width		TBD		MC Cycles
T14	MasterOUT	INTR De-assert		4		MC Cycles
T15	MasterOUT	Recovery Time		TBD		MC Cycles
T16	MasterOUT	INTR Response	0			MC Cycles

To account for the latency through the MPL link, a dual READ operation is required by the host. The first read returns invalid data (all Low). Once data has returned to the Master LM2502, the INTR signal is asserted to inform the host to initiate a second read operation. When the Master LM2502 sees the Read signal/CS* combination, it will de-assert the INTR signal and Valid data is presented.

Functional Description (Continued)

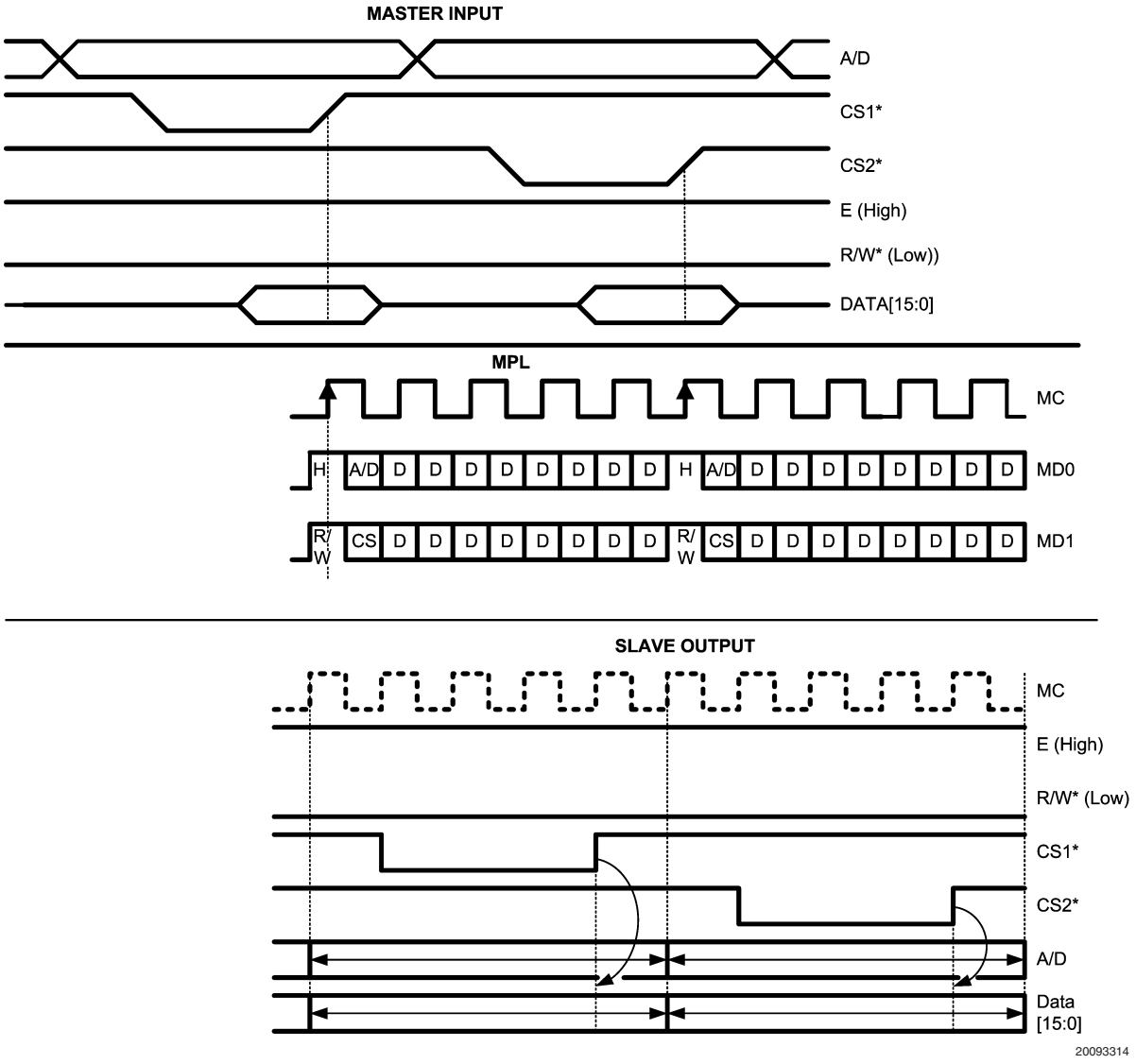


FIGURE 18. Back-to-Back WRITE Operations—68xx Mode

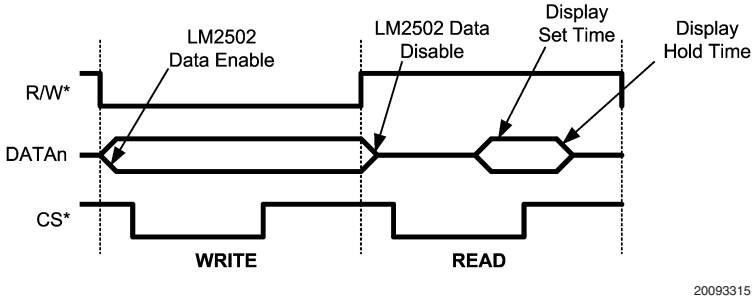


FIGURE 19. Slave WRITE and Slave READ Operation

LM2502 Features and Operation

POWER DOWN/OFF

A Master configured device may be powered by the PD* pin. A Low on this pin will power down the entire device and turn off the line current to MD0, MD1, and MC. The Slave device senses this MC state and also powers down. In this state the following outputs are driven to:

Master:

INTR = Low

Slave:

PD* = L, AD = DATAn = CLK = Low,

CS1* = CS2* = MF0 = MF1 = High

UN-USED/OPEN PINS

Unused inputs must be tied to the proper input level — do not float them. Unused outputs should be left open to minimize power dissipation.

PHASE-LOCKED LOOP

When the LM2502 is configured as a Master, a PLL is provided to generate the serial link clock. The Phase-locked loop system generates the serial data clock at several multiples of the input clock. The PLL operates with an input clock between 8 and 20MHz. See *Table 8. PLL_CON Settings* below, Multiplier/Divisor times CLK rate must also be less than 80 MHz. The 80 MHz limitation is based on the semiconductor process used on this implementation — it is not an MPL limitation.

Line rate should also be selected such that it is faster the input load rate when bursting data across the link. Otherwise 8/10 X Line rate must be greater than the input load rate to the Master. At the maximum raw data rate of 320 Mbps, the maximum information rate is 256 Mbps. Thus the parallel load rate at the Master input must not exceed 16 Mega Transfers per second sustained (of 16 data bits). The Master can accommodate up to four words at a higher rate due to internal FIFOs.

Configuration pins (PLL_CON[2:0], and M/S*) are used to determine the mode of which the part is operating in. In the Slave configuration the PLL block is disabled. The Slave PLL_CON pins are required to set up the proper divisor for the CLK pin. Slave PLL_CON[2:0] pins do not need to be set the same as the Master, this allows for clock multiplication / division to be supported for the output clock reference signal.

TABLE 8. PLL_CON Settings

PLLCON2	PLLCON1	PLLCON0	Multiplier/Divisor	Maximum CLK Input (MC ≦ 80 MHz)
0	0	0	CLK X 2	20 MHz
0	0	1	CLK X 4	20 MHz
0	1	0	CLK X 6	13.3 MHz
0	1	1	CLK X 7	11.43 MHz
1	0	0	CLK X 8	10 MHz
1	0	1	CLK X 9	8.89 MHz
1	1	0	CLK X 10	8 MHz
1	1	1	CLK/2	(TEST MODE)

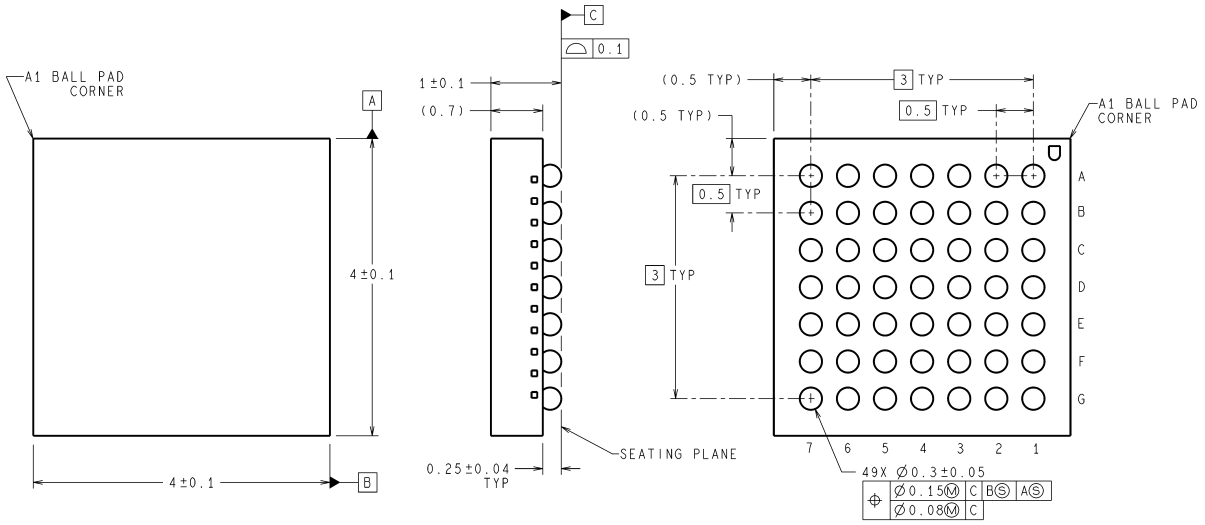
RESET

The LM2502 has two reset domains: Master and Slave. The PD* pin resets the Master logic and the lack of current flow on the MC resets the Slave logic. There is no internal power-on reset circuit, thus it is necessary to power up the Master with PD* asserted.

MASTER/SLAVE SELECTION

The M/S* pin is used to configure the device as either a Master or Slave device. When the M/S* pin is a Logic High, the Master configuration is selected. The Driver block is enabled for the MC line, and the MD lines. When the M/S* pin is a Logic Low, the Slave configuration is selected. The Receiver block is enabled for the MC line, and the MD lines.

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

GRA49A (Rev A)

Note: ES units may be offered in a footprint compatible 49 Ball FBGA package.

Preliminary Drawing 49 Ball MICRO ARRAY, 0.5mm pitch
Order Number LM2502GR
NS Package Number GRA49A

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