APPLICATIONS:
•
PDA
•
Digital Camera

LH28F320S3 32M (4M × 8/2M × 16) Smart 3 Flash Memory

FEATURES

- Smart 3 technology
  - 2.7 V or 3.3 V V_{CC}
  - 2.7 V, 3.3 V or 5 V V_{PP}
- Common flash interface (CFI)
  - Universal and upgradable interface
- Scalable command set (SCS)
- High speed write performance
  - 32 Bytes × 2 plane page buffer
  - 2.7 µs byte write transfer rate
- High speed read performance
  - 110/140 ns (3.3 V ±0.3 V)
  - 130/160 ns (2.7 V – 3.6 V)
- Enhanced automated suspend options
  - Write suspend to read
  - Block erase suspend to write
  - Block erase suspend to read
- Industry-standard packaging
  - 56-pin SSOP
- Chip size packaging
  - 64-ball CSP
- SRAM-compatible write interface
- User-configurable × 8 or × 16 operation
- High-density symmetrically-blocked architecture
  - Sixty-four 64K erasable blocks
- Enhanced data protection features
  - Absolute protection with V_{PP} = GND
  - Flexible block locking
  - Erase/write lockout during power transitions
- Extended cycling capability
  - 100,000 block erase cycles
  - 6.4 million block erase cycles/chip
- Low Power management
  - Deep power-down mode
  - Automatic power savings mode
  - Decreases I_{CC} in static mode
- Automated write and erase
  - Command user interface
  - Status register
- ETOX™ V nonvolatile flash technology
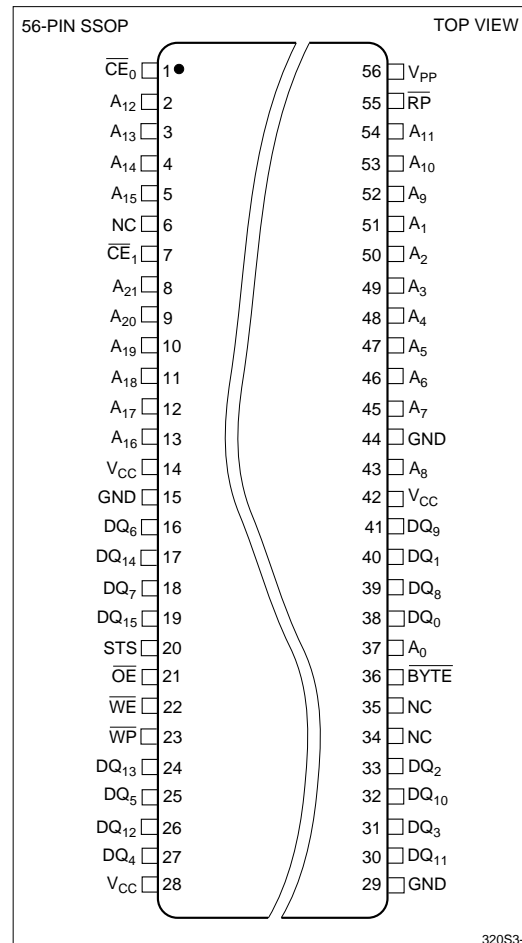- Not designed or rated as radiation hardened

DESCRIPTION

SHARP's LH28F320S3 Flash memory with Smart 3 technology is a high-density, low-cost, nonvolatile, read/write storage solution for a wide range of applications. Its symmetrically-blocked architecture, flexible voltage and extended cycling provide for highly flexible component suitable for resident flash arrays, SIMMs and memory cards. Its enhanced suspend capabilities provide for an ideal solution for code and data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the LH28F320S3 offers three levels of protection: absolute protection with V_{PP} at GND, selective hardware block locking, or flexible software block locking. These alternatives give designers ultimate control of their code security needs.

56-PIN SSOP PINOUT

56-PIN SSOP   TOP VIEW

Pin	Left		Pin	Right
1	$\overline{CE}_0$		56	V_{PP}
2	A_{12}		55	$\overline{RP}$
3	A_{13}		54	A_{11}
4	A_{14}		53	A_{10}
5	A_{15}		52	A_9
6	NC		51	A_1
7	$\overline{CE}_1$		50	A_2
8	A_{21}		49	A_3
9	A_{20}		48	A_4
10	A_{19}		47	A_5
11	A_{18}		46	A_6
12	A_{17}		45	A_7
13	A_{16}		44	GND
14	V_{CC}		43	A_8
15	GND		42	V_{CC}
16	DQ_6		41	DQ_9
17	DQ_{14}		40	DQ_1
18	DQ_7		39	DQ_8
19	DQ_{15}		38	DQ_0
20	STS		37	A_0
21	$\overline{OE}$		36	$\overline{BYTE}$
22	$\overline{WE}$		35	NC
23	$\overline{WP}$		34	NC
24	DQ_{13}		33	DQ_2
25	DQ_5		32	DQ_{10}
26	DQ_{12}		31	DQ_3
27	DQ_4		30	DQ_{11}
28	V_{CC}		29	GND

320S3-1

64-BALL CSP PINOUT

64-BALL CSP   TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	NC	NC			NC	NC	NC	A_{20}	A_{21}	NC	$\overline{WP}$	$\overline{OE}$	STS	NC	NC	NC			NC	NC
B							A_{17}	A_{18}	A_{19}	$\overline{CE}_1$	$\overline{WE}$	DQ_{15}	DQ_7	DQ_{14}						
C							A_{15}	V_{CC}	A_{14}	A_{16}	DQ_6	DQ_5	GND	DQ_{13}						
D							A_{12}	$\overline{CE}_0$	A_{13}	NC	NC	DQ_{12}	V_{CC}	DQ_4						
E							$\overline{RP}$	V_{PP}	A_{11}	NC	NC	DQ_3	GND	DQ_{11}						
F							A_9	A_8	A_{10}	GND	DQ_9	DQ_{10}	V_{CC}	DQ_2						
G							A_7	A_6	A_5	A_2	NC	DQ_0	DQ_8	DQ_1						
H	NC	NC			NC	NC	NC	A_4	A_3	A_1	NC	BYTE	A_0	NC	NC	NC			NC	NC

320S3-2