EB-2060x

DDX All-Digital, High Efficiency Evaluation Amplifier

FEATURES

DDX-2000/2060 CHIP SET
- OPERATION 9 to 30 VDC
- 2x35 W into 8 Ω @ 1% THD
- 1x70 W into 4 Ω @ 1% THD

TYPICAL PERFORMANCE
- THD+N - 0.08% (1W, 1kHz)
- SNR - 93 dB (A-weighted)
- EFFICIENCY - 88%

DIGITAL INPUT
- S/PDIF COAX/OPTICAL
- I^2S LOOP THROUGH

DIGITAL PREAMP FEATURES
- VOLUME
- BALANCE
- ANTICLIPPING
- AUTOMATIC MUTE

GENERAL DESCRIPTION

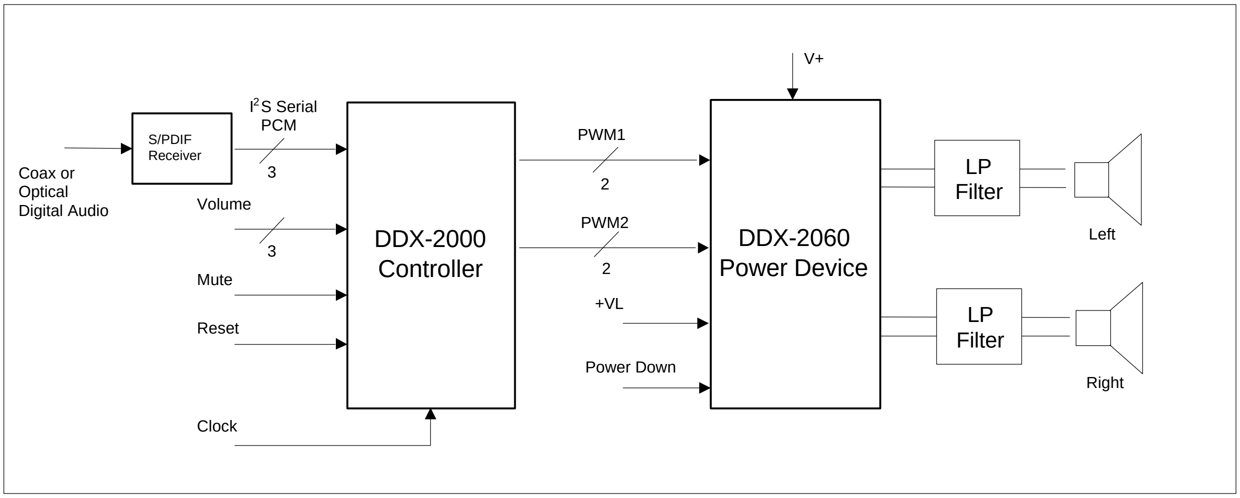
The EB-2060x is an evaluation amplifier that showcases Apogee's all-digital, high efficiency Direct Digital Amplification (DDX®) technology. The board features a DDX-2000 Controller and DDX-2060 Power Device which provide full digital audio preamplifier functions and power amplification. The board includes both coaxial and optical S/PDIF interfaces, digital volume and balance controls and local power regulation to operate from a signal supply voltage.

The EB-2060x is available in both a stereo 35W (EB-2060S) and a mono 70W version (EB-2060M).

ORDERING INFO

EB-2060S – DDX stereo amplifier board
EB-2060M – DDX mono amplifier board

EB-2060x BLOCK DIAGRAM



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DESIGN OVERVIEW

The EB-2060x is an all-digital amplifier evaluation board that demonstrates Apogee's DDX-2000/2060 chip set solution. The board features – coaxial and optical S/PDIF digital interfaces, volume and balance controls, expansion headers for off-board processing, and local power regulation enabling single supply operation from +10 to +28 VDC. The all-digital amplifier board may be configured as either 2 x 35W into 8Ω or 1 x 70W into 4Ω.

DDX-2000/2060 OVERVIEW

The DDX-2000 Controller is a 3.3V digital integrated circuit that converts serial PCM digital audio signals into Apogee's patented damped ternary outputs. The device supports two modes of digital volume control, muting and anti-clipping functions. A block diagram of the device is shown in Figure 1.

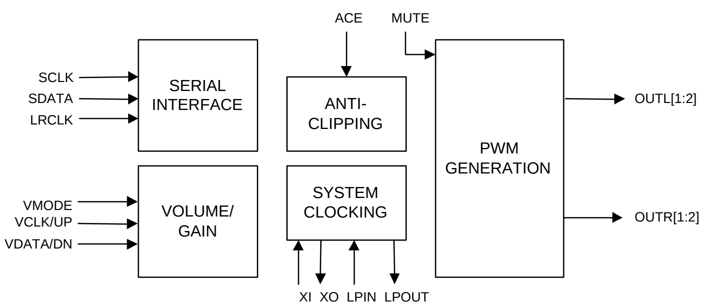


Figure 1 - DDX-2000 Functional Diagram

The DDX-2060 Power Device is a dual channel H-Bridge that can deliver over 35 watts per channel of audio output power. The DDX-2060 includes; a logic interface, integrated bridge drivers, high efficiency MOSFET outputs and protection circuitry. Two logic level signals per channel are used to control high-speed MOSFET switches to connect the speaker load to the input supply or to ground in a bridge configuration, according to Apogee's patented damped ternary PWM. The DDX-2060 includes over-current, thermal, and over-voltage protection and under-voltage lockout with automatic recovery. A thermal warning status is also provided.

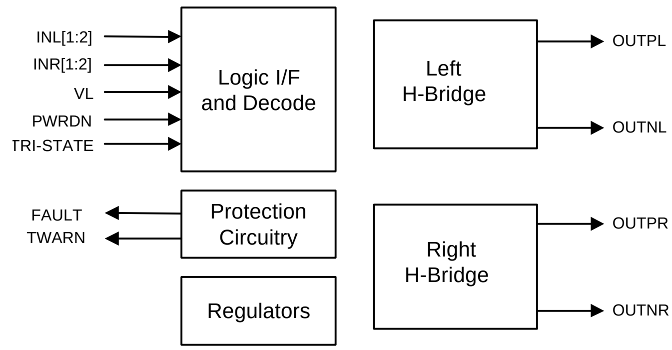


Figure 2 - DDX-2060 Block Diagram

SCHEMATIC DESCRIPTION

S/PDIF INPUT INTERFACE (FIG. 3A)

The EB-2060x accommodates either a coaxial or an optical S/PDIF digital audio interface. Either input may be selected by moving jumper J2. Connect J2 pins 1-2 for coaxial or J2 pins 2-3 for optical S/PDIF. A Crystal CS8415A digital audio interface receiver is utilized to convert the incoming S/PDIF signal to serial I^2S used by the DDX-2000. The receiver also recovers a 256*Fs clock synchronized to the incoming signal which is used as the master clock to the DDX-2000. The design will support sample rates from below 32 kHz to above 48 kHz. The receiver PLL out-of-lock signal is used to mute the amplifier's output when a valid S/PDIF signal is not present. Zero ohm jumpers R6,R9,R10,R11,R42 are provided to disconnect the outputs of the S/PDIF receiver from the inputs to the DDX-2000 so that external signals may be applied via the expansion header J7, (see Fig. 3D).

DIGITAL SIGNAL PROCESSING (FIG. 3B)

The DDX-2000 converts serial I^2S digital audio signals into pulse-width-modulated digital signals output at 8*Fs, according to Apogee's patented damped ternary architecture. Signals from the S/PDIF receiver are applied as inputs to the DDX processor and signals from the DDX processor are applied to the inputs of the DDX power stage.

A low-cost microcontroller with an ADC is used to implement the volume and balance controls. The amplifier's volume and balance levels are adjusted using two potentiometers. The DC voltage set by the potentiometers is read by the microcontroller interfaced to the volume serial port of the DDX-2000. The DDX-2000 has independent volume control registers that have an adjustment range from –82.5 dB to +12.0 dB in 0.75 dB increments. A 0 dB flag is included on the microcontroller to set the volume level for both channels to be unity gain. This setting is particularly useful for audio measurements.

The EB-2060x permits three separate methods for clocking the DDX-2000. The default is via the 256*Fs recovered clock output from the S/PDIF receiver IC. The second is via the expansion header J7 used to apply an external clock source to synchronize, for example, multiple DDX-2000 ICs to the same clock. Zero-ohm jumper R35 is installed to pass either of these clock sources to the DDX-2000 master clock input. The last method is asynchronous from an external crystal. The DDX-2000 contains a crystal oscillator which may be used for single sample-rate applications. Oscillator circuit Y1, C30, C37, R24, R26 may be populated and jumper R35 removed for applications where a 256*Fs clock source is not convenient. The DDX-2000 tolerates a sample rate mismatch of +/-0.2% about the crystal frequency without performance degradation. The crystal footprint is a surface mount Epson MA-506.

There are additional provisions for demonstrating DDX-2000 functionality. The GCEN flag is used to disable the anticlipping function and is controlled by DIP rocker switch SW1. Jumper R29 is provided to change the serial port mode on the DDX-2000 from I^2S to left-justified to accommodate an external set of signals. Jumpers R13, R14, R30 are provided for test modes and must not be changed. A channel reverse flag is provided which inverts LRCLK causing left channel data to be output on the right channel and vice versa. This function is intended to be used for multiple amplifiers configured as mono when used in a multichannel audio demonstration.

POWER OUTPUT (FIG. 3C)

The DDX-2060 provides power amplification by translating logic level PWM signals into power level signals. These power level signals are applied to a passive two-pole lowpass filter to reconstruct the audio signal providing power to the load. The output filter functions to attenuate unwanted high frequency signals from reaching the load. A filter design for 8 Ω loads is shown in the Fig. 3C schematic for reference.

The DDX-2060 is designed for stereo operation as either two independent full-bridges or for mono operation as one full-bridge with twice the current capability, enabling higher output power. The EB-2060x is designed to demonstrate both configurations via component substitutions. The schematic notes in Fig. 3C detail component changes to convert from stereo to mono operation. Evaluation boards configured as either stereo or mono may be ordered with the appropriate part number designations. Jumpers R19, R22, R25, R33 are used to configure PWM inputs for stereo operation. Jumpers R17, R23, R27, R36 are used to configure PWM inputs for mono operation. Jumpers JP1 and JP3 parallel the output bridges enabling higher output current. Jumpers JP2 and JP4 parallel the output filter sections to a 4Ω load. Capacitor C29 is the differential capacitor required for the 4Ω filter only.

In applications where <u>only</u> mono 70W / 4Ω operation is desired, e.g. subwoofer, the output filter may be simplified. Two filter sections may be employed in lieu of sections in parallel. Inductors may be ½ the value with twice the current rating. Capacitors are double the value and resistors are ½ the value at twice the power rating.

Snubbers are employed to protect the output MOSFETs from inductive transients. Peak voltage on the DDX-2060 output and power pins must not exceed 40V. Output snubbers for the stereo implementation are R15,C23 and R31,C40 and the snubber for the mono implementation is R21,C32.

Input protection is provided for the amplifier by diode D1. D1 will protect from overvoltage and reverse power applications by shunting the power supply.

A thermal warning indicator is activated by the DDX-2060 when its junction temperature exceeds +130°C. The thermal warning output is used to force the power LED to change color from green to red forecasting the potential of an overtemperature shutdown.

HEADERS / REGULATORS (FIG. 3D)

The EB-2060x features local power regulation to facilitate operation from a unipolar +10 to +28 VDC supply. Alternatively, auxiliary power may be applied at J8 (removing bead L7) separating logic and output power supplies. Output from the onboard +5V regulator is available on the J6 test header. Output from the onboard +3.3V regulator is available on the J7 expansion header. There is capability available to power external circuits from either the +5V or the +3.3V supplies or a combination not to exceed a total current of 0.33A.

Expansion header J7 is provided to monitor or apply input signals to the DDX-2000. Jumper R42 may be removed to pass serial data provided by an external processor. Test header J6 is provided to monitor signals output from the DDX-2000. Signals INLC, INLD, INRC, INRD are driven low by the DDX-2000 and are used for test purposes only. DIP switch SW1 is used for control functions: POS1 reverses data channels when open, normal when closed; POS2 sets unity gain for test when closed, normal when open; POS3 forces the DDX-2060 into low power mode when closed, normal when open; POS4 disables the anticlipping function when closed, normal when open.

Supervisor U8 is used for power-on-reset, power-off sequencing, and as a convenient means of commanded reset via pushbutton.

ADDITIONAL INFORMATION

Bill of Materials

A bill of materials for the evaluation board is provided in Table 1 for reference. Note equivalent components from alternate manufacturers may be substituted. No warranty of system performance is implied by Apogee through use of the reference bill of materials.

Power Dissipation/Heat Sink Requirements

The DDX-2060 is a high efficiency dual channel design intended for audio applications needs up to 35 Watts RMS per channel. The power dissipation of the device will depend primarily on the supply voltage, load impedance, and output modulation level. The thermal performance of the evaluation board is consistent with a steady-state duty rating of 25W RMS per channel with both channels driven into 8Ω.

The DDX-2060 surface mount package includes an exposed thermal pad on the bottom of the device to provide a direct thermal path from the integrated circuit to the PCB. This pad must be soldered to a low thermal impedance path at circuit ground potential for proper operation, e.g. a PCB ground plane. For continuous duty rated applications, careful consideration must be made to the overall thermal design.

Performance Measurements

Typical performance measurements for the evaluation board are shown in Figs 4 through 11.

Class D amplifiers produce measurable switching distortion outside the audio bandwidth. Apogee's DDX amplifier uses a patented PWM modulation scheme that significantly reduces the size of these products compared to typical Class D designs. However, in order to obtain accurate performance measurements in the audio bandwidth (i.e., 20Hz to 20kHz) additional filtering is required.

The Typical Performance data in was taken using a brick wall filter with a break frequency of 22kHz. This type of filter is often provided as part of audio measurement systems.

OPERATING INSTRUCTIONS

Refer to Fig. 12 evaluation amplifier assembly drawing. Attach a regulated power supply at J3 set between +10V and +28VDC. At +28V, the power supply must be capable of delivering 3A minimum for two channels. Attach a digital audio input source at either the coaxial or optical S/PDIF connectors. Select the digital input source via J2. Connect 8 Ohm speakers to J4 (left speaker) and J5 (right speaker). Configure SW1 as POS1 closed, POS2,3,4 open. Note, the speaker outputs are bridged. Do not ground any speaker connections, e.g. through an oscilloscope. Apply power, digital source material and enjoy!

FIG. 3A - DDX EVAL AMPLIFIER SCHEMATIC: S/PDIF INPUT INTERFACE

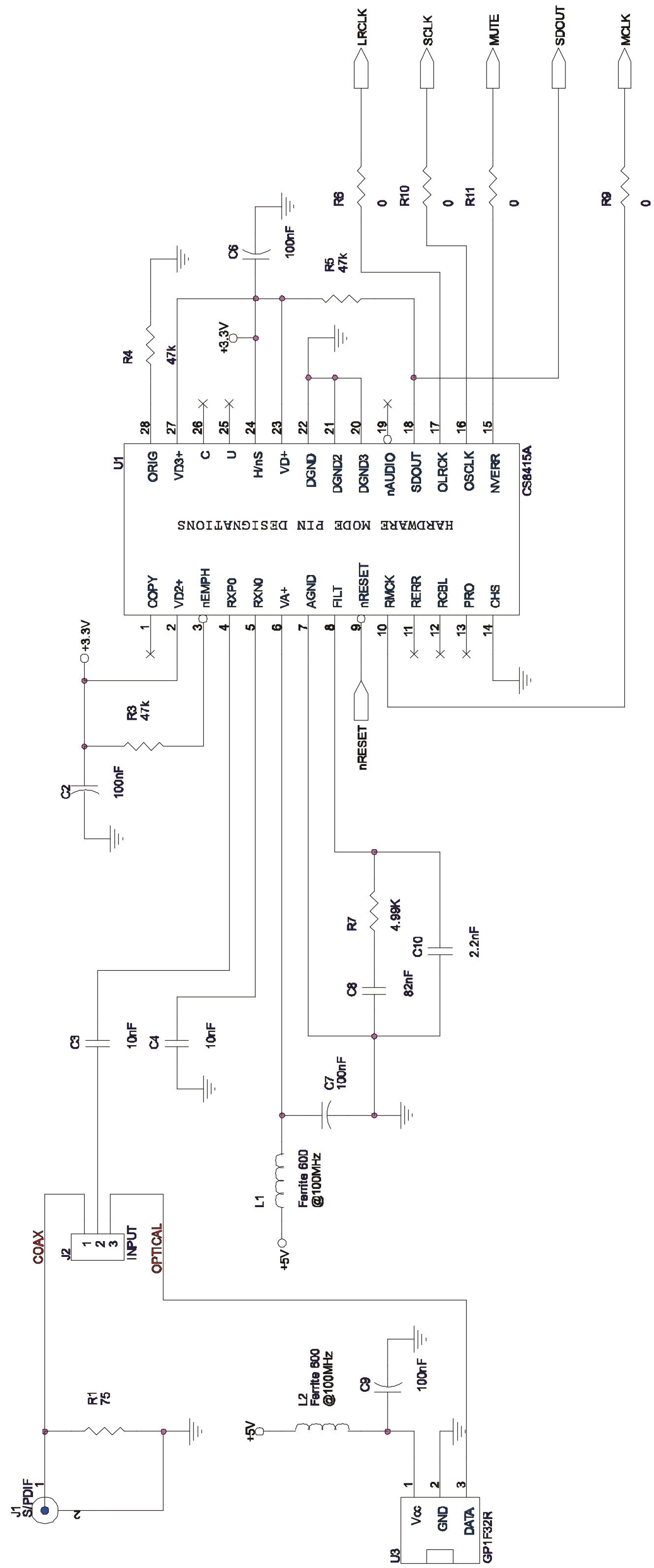


FIG. 3B - DDX EVAL AMPLIFIER SCHEMATIC: DIGITAL SIGNAL PROCESSING

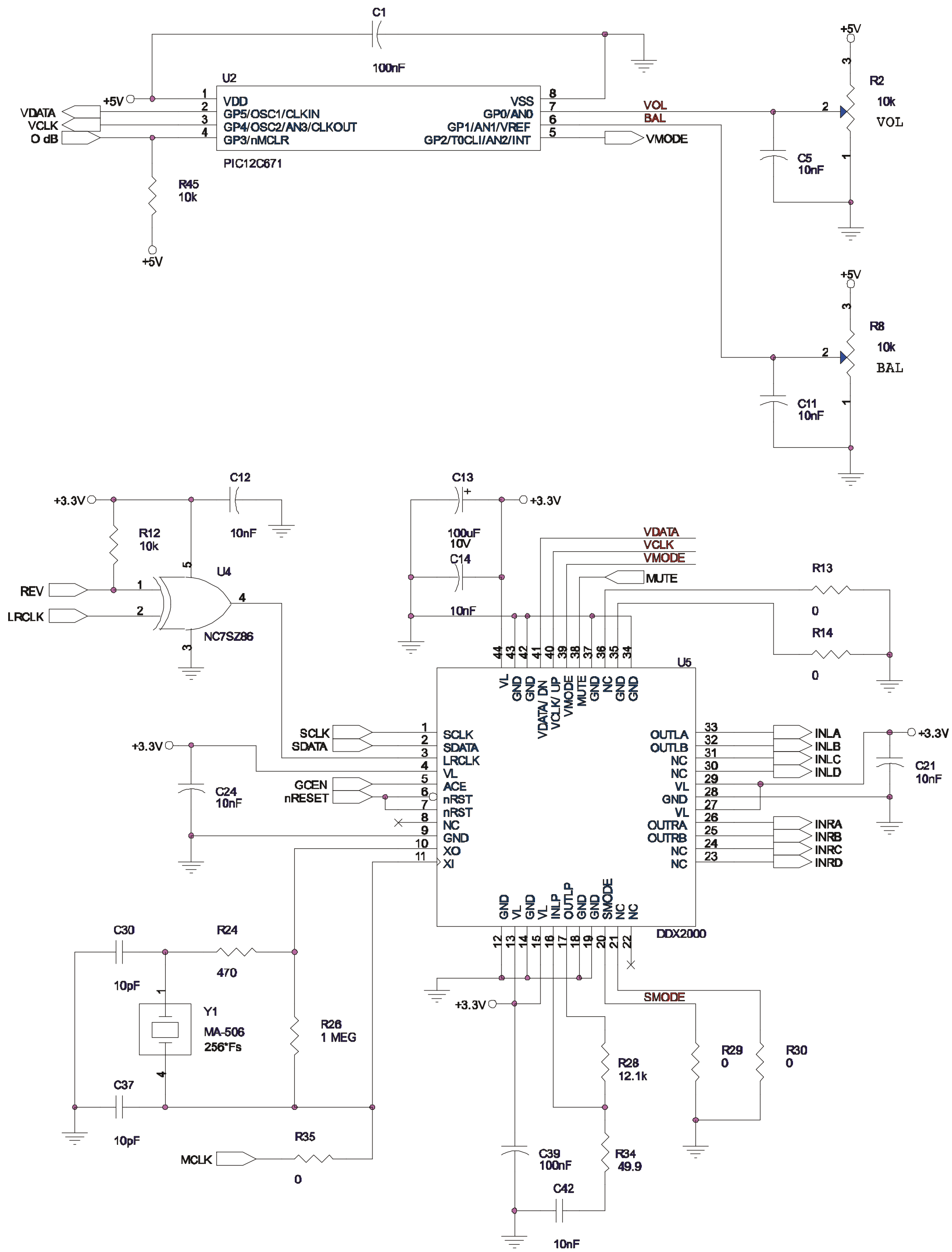


FIG. 3C - DDX EVAL AMPLIFIER SCHEMATIC: POWER OUTPUT

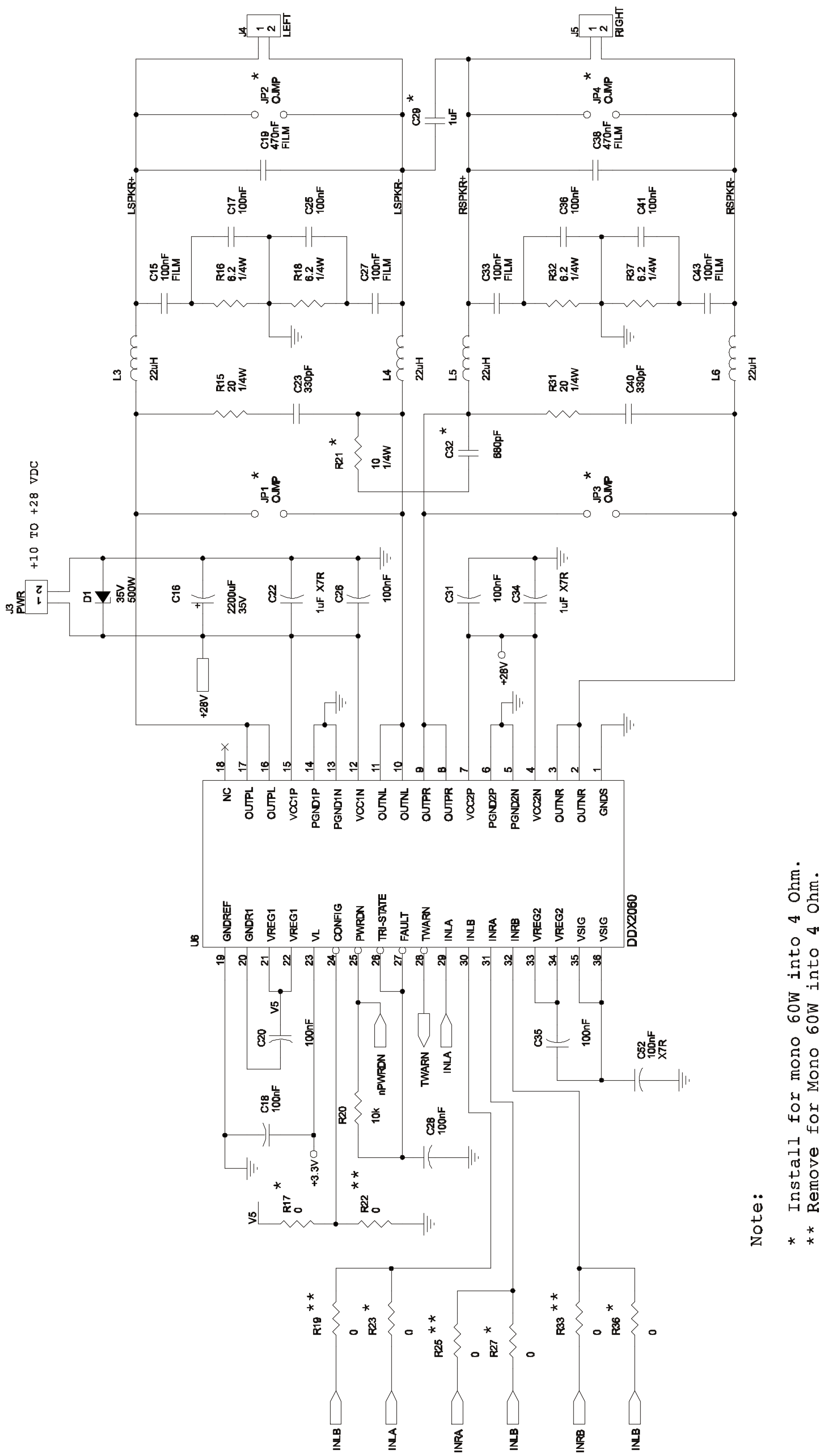


FIG. 3D - DDX EVAL AMPLIFIER SCHEMATIC: HEADERS / REGULATORS

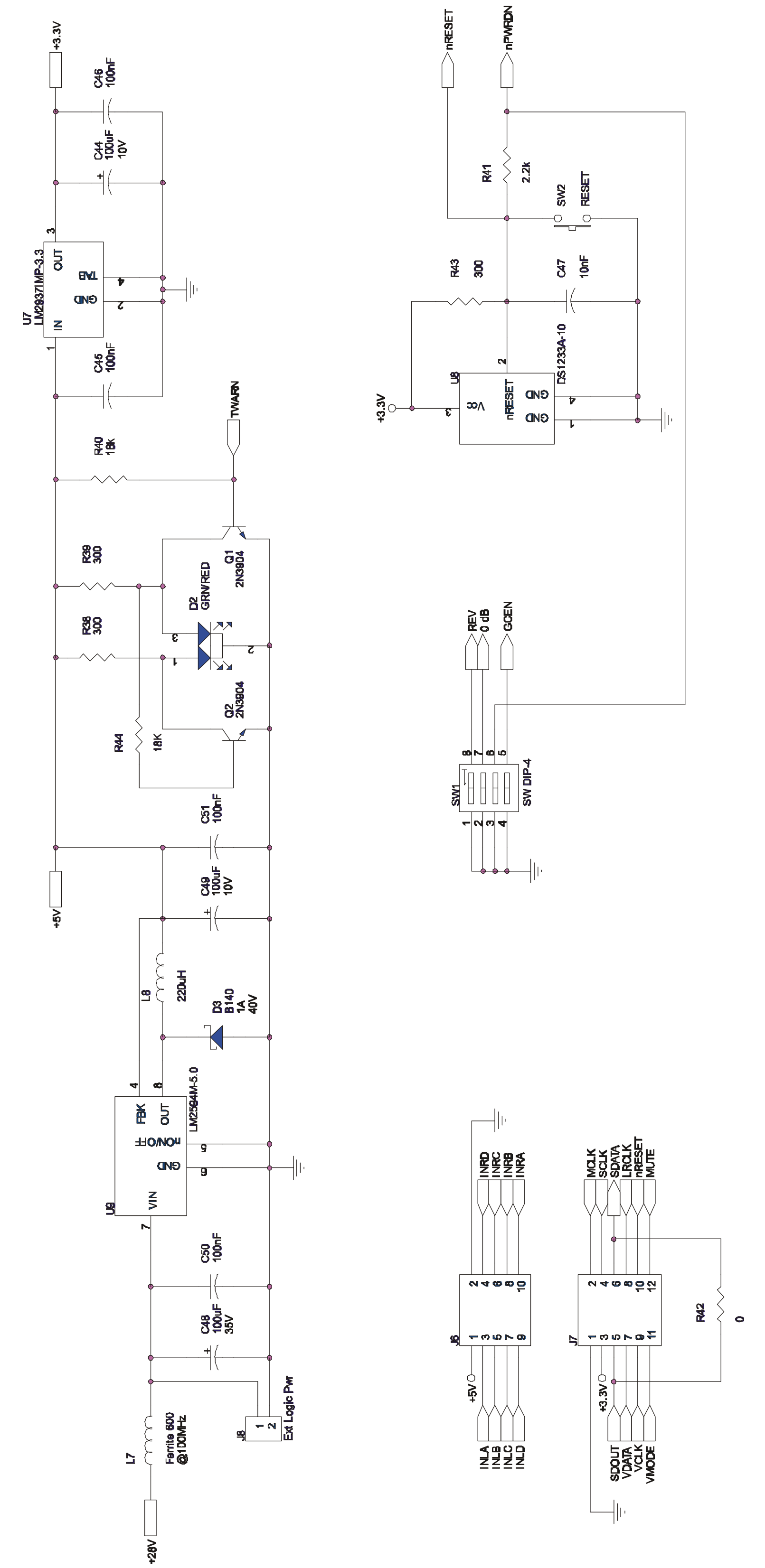


TABLE 1 - DDX EVALUATION AMPLIFIER BOM

Item	Quantity	Reference	Description	Mfr. Part No.	Mfr.
1	13	C1,C2,C6,C7,C9,C18,C20,	Capacitor, Ceramic, Y5V, 100nF, 25V, +80/ -20%	ECJ-2VF1E104Z	Panasonic
		C28,C35,C39,C45,C46,C51			
2	3	C26,C31,C50	Capacitor, Ceramic, Y5V, 100nF, 50V, +80/ -20%	ECJ-2VF1H104Z	Panasonic
3	2	C22,C34	Capacitor, Ceramic, X7R, 1uF, 25V, 10%	ECJ-3YB1E105K	Panasonic
		NOTE 1	Capacitor, Ceramic, X7R, 1uF, 50V, 10%	C1812C105K5RAC	Kemet
4	5	C17,C25,C36,C41,C52	Capacitor, Ceramic, X7R, 100nF, 50V, 10%	ECJ-3VB1H104K	Panasonic
5	4	C15,C27,C33,C43	Capacitor, Polyester Film, 100nF, 100V, 5%	2222 370 22104	Centralab
6	9	C3,C4,C5,C11,C12,C14,C21,C24,C47	Capacitor, Ceramic, Y5V, 10nF, 50V, +80/ -20%	ECJ-2VF1H103Z	Panasonic
7	1	C42	Capacitor, Ceramic, X7R, 10nF, 50V, 10%	ECU-V1H103KBG	Panasonic
8	1	C8	Capacitor, Ceramic, X7R, 82nF, 25V, 10%	ECJ-2VB1E823K	Panasonic
9	1	C10	Capacitor, Ceramic, X7R, 2.2nF, 50V, 10%	ECU-V1H222KBN	Panasonic
10	2	C19,C38	Capacitor, Polyester Film, 470nF, 63V, 5%	2222 370 12474	Centralab
11	1	C16	Capacitor, Aluminum Electrolytic, M-Series, 2200uF, 35V, 20%	ECA-1VM222	Panasonic
12	2	C23,C40	Capacitor, Ceramic, X7R, 330pF, 50V, 10%	ECJ-2VC1H331J	Panasonic
13	1	C32	Capacitor, Ceramic, X7R, 680pF, 50V, 10%	ECJ-2VC1H681J	Panasonic
14	1	C29	Capacitor, Polyester Film, 1uF, 63V, 5%	2222 370 12105	Centralab
15	2	C30,C37	Capacitor, Ceramic, NPO, 10pF, 50V, 10%	ECU-V1H100DCN	Panasonic
16	1	C48	Capacitor, Aluminum Electrolytic, HFS-Series, 100uF, 35V, 20%	ECE-A1VFS101	Panasonic
17	3	C13,C44,C49	Capacitor, Aluminum Electrolytic, HFS-Series, 100uF, 10V, 20%	ECE-A1AFS101	Panasonic
18	1	D1	Diode, TVS, 1.5KW, Uni-Directional, 30V Standoff, 35.8VBR, 7%, SMCJ	SMCJ30A	Diodes Inc.
19	1	D2	LED, T1 3/4, Green/Red, White Diffused	LN11WP23	Panasonic
20	1	D3	Diode, Schottkey Barrier, SMD, 1A, 40V	B140	Diodes Inc.
21	4	JP1,JP2,JP3,JP4	Buss Wire Jumper, 22 AWG, 0.1"		
22	1	J1	RCA Phono connector, Right Angle PCB, Tin Plate	901	Keystone
23	1	J2	Header, 3-pin, 1X3, 0.10 spacing.	TSW-103-07-S-S-LL	Samtec
24	3	J3,J4,J5	Connector, Terminal Block Plug, 5.08mm, 12-30 AWG, Two-position	EMKDS 2.5/2-5.08	Phoenix Contact
25	1	J6	Header, 10-pin, 2X10, 0.10 spacing.	TSW-105-07-S-D-LL	Samtec
26	1	J7	Header, 12-pin, 2X10, 0.10 spacing.	TSW-106-07-S-D-LL	Samtec
27	3	L1,L2,L7	Ferrite Chip, EMI Supression, SMD, 600 Ohm @100MHz, 0.5A	HZ0805E601R-00	Steward
28	4	L3,L4,L5,L6	Inductor, 22uH, 2.0A, .062 DCR	CT622LY-220K	Central Technologies
		ALTERNATE	Inductor, 22uH, 3.5A, .047 DCR	CTDO5022P-223	Central Technologies
		ALTERNATE	Inductor, 22uH, 2.6A, .046 DCR	RL-5480-4-22	Renco
29	1	L8	Inductor, 220uH, 10%, .64A, .68DCR	CT622LY-221K	Central Technologies
30	2	Q1, Q2	Transistor, NPN, 330mW, 40V CEO	FMMT3904	Zetex
31	1	R1	Resistor, Chip, Thk Film, 75, 5%, 1/10W, 200ppm	ERJ-6GEYJ750V	Panasonic
32	1	R2	Potentiometer, 10k, 9mm Audio, Linear taper, Right angle	EVU-E2AF25B14	Panasonic
33	1	R8	Potentiometer, 10k, 9mm Audio, Linear taper, Right angle, Center Detent	EVU-E3AF25B14	Panasonic
34	3	R3,R4,R5	Resistor, Chip, Thk Film, 47k, 5%, 1/10W, 200ppm	ERJ-6GEYJ473V	Panasonic
35	18	R6,R9,R10,R11,R13,R14,	Zero Ohm Jumper, SMD 0805	ERJ-6GEYJ000V	Panasonic
		R17,R19,R22,R23,R25,R27,			
		R29,R30,R33,R35,R36,R42			
36	1	R7	Resistor, Chip, Thk Film, 4.99K, 1%, 1/10W, 100ppm	ERJ-6ENF4991V	Panasonic
37	3	R12,R20,R45	Resistor, Chip, Thk Film, 10K, 5%, 1/10W, 200ppm	ERJ-6GEYJ103V	Panasonic
38	2	R15,R31	Resistor, Chip, Thk Film, 20, 5%, 1/4W, 200ppm	ERJ-14YJ200U	Panasonic
39	4	R16,R18,R32,R37	Resistor, Chip, Thk Film, 6.2, 5%, 1/4W, 200ppm	ERJ-14YJ6R2U	Panasonic
40	1	R24	Resistor, Chip, Thk Film, 470, 5%, 1/10W, 200ppm	ERJ-6GEYJ471V	Panasonic
41	1	R26	Resistor, Chip, Thk Film, 1Meg, 5%, 1/10W, 200ppm	ERJ-6GEYJ105V	Panasonic
42	1	R28	Resistor, Chip, Thk Film, 12.1k, 1%, 1/10W, 100ppm	ERJ-6ENF1212V	Panasonic
43	1	R34	Resistor, Chip, Thk Film, 49.9, 1%, 1/10W, 100ppm	ERJ-6ENF49R9V	Panasonic
44	3	R38,R39,R43	Resistor, Chip, Thk Film, 300, 5%, 1/10W, 200ppm	ERJ-6GEYJ301V	Panasonic
45	2	R40, R44	Resistor, Chip, Thk Film, 18k, 5%, 1/10W, 200ppm	ERJ-6GEYJ183V	Panasonic
46	1	R41	Resistor, Chip, Thk Film, 2.2k, 5%, 1/10W, 200ppm	ERJ-6GEYJ222V	Panasonic
47	1	R21	Resistor, Chip, Thk Film, 10, 5%, 1/4W, 200ppm	ERJ-14YJ100U	Panasonic
48	1	SW1	DIP Switch, 4-position, Raised-rocker, sealed	76SB04S	Grayhill
49	1	SW2	Switch, Momentary Tact, SMD, 230gf	B3S-1002	Omron
50	1	U1	Digital Audio Interface Receiver IC	CS8415A-CS	Crystal/Cirrus logic
51	1	U2	Microcontroller, 8-Bit, 8-Pin, w/ADC	PIC12C671-04/SM	Microchip
52	1	U3	Toslink Light Receiving Unit	GP1F32R	Sharp
53	1	U4	TinyLogic CMOS XOR gate	NC7SZ86M5	Fairchild
54	1	U5	DDX Digital Processing ASIC	DDX2000	Apogee
55	1	U6	DDX Power IC	DDX2060	Apogee
56	1	U7	Regulator, Linear, 3.3V, .5A	LM2937IMP-3.3	NSC
57	1	U8	Supervisor, 3.3V Econoreset	DS1233A-10/SM	Dallas
58	1	U9	Switching Regulator, Step Down, 45V, 0.5A, Fixed +5V, 150KHz	LM2594M-5.0	NSC
59	1	Y1	Crystal, 11.2896 MHz, 50ppm, Fundamental Mode, SMD	MA-506-11.2896M-C2	EPSON
		ALTERNATE	Crystal, 12.288 MHz, 50ppm, Fundamental Mode, SMD	MA-506-12.288M-C2	EPSON
60	1	J8	Header, 2 pin, 1x2, .100 spacing, w/Locking ramp.	22-01-2027	Molex

NOTE 1: The evaluation board is shipped using 1uF, 25V capacitors due to PCB footprint. For applications up to 30V, use 50V rated capacitors.

Typical Performance Characteristics at Vcc = 28V, 8 Ohm load.

Fig 4: Efficiency vs Output Power

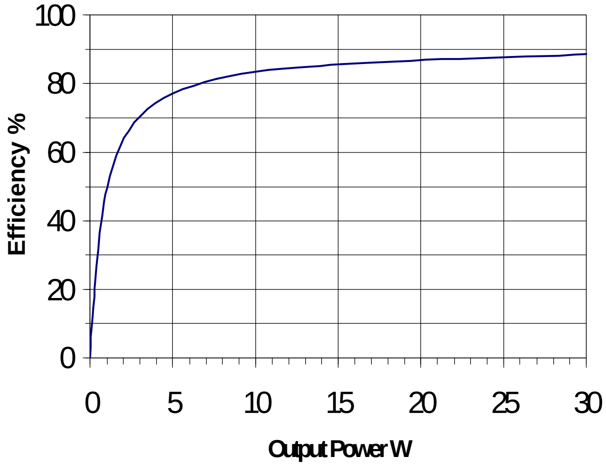


Fig 5: Frequency response

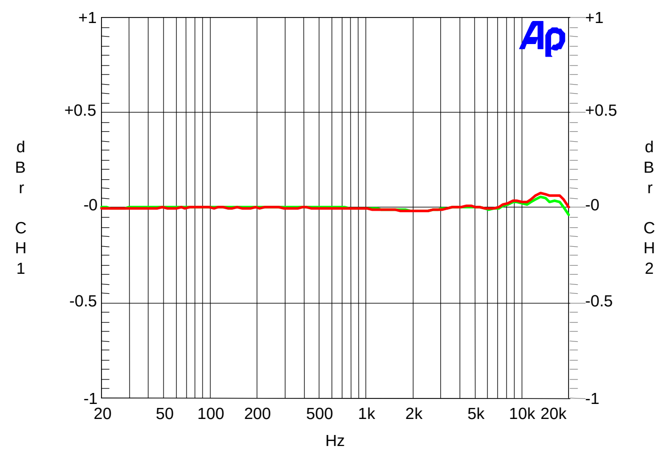


Fig 6: THD+N vs Frequency

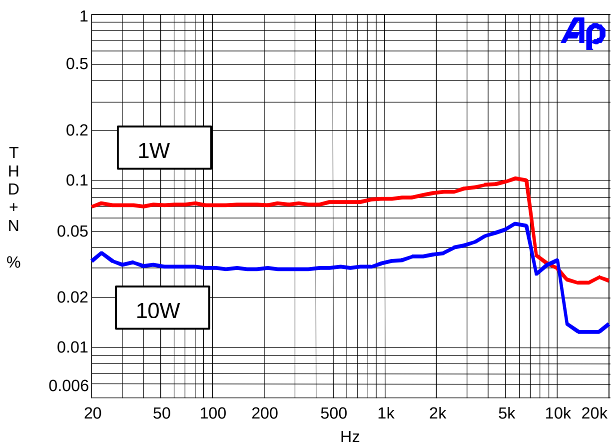
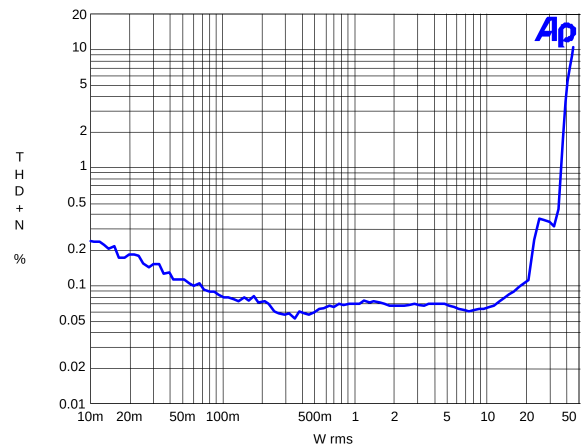


Fig 7: THD+N vs Outpwr at 1 KHz



Details are subject to change without notice.

Typical Performance Characteristics at Vcc = 24V, 4 Ohm load.

Fig 8: THD+N vs Frequency

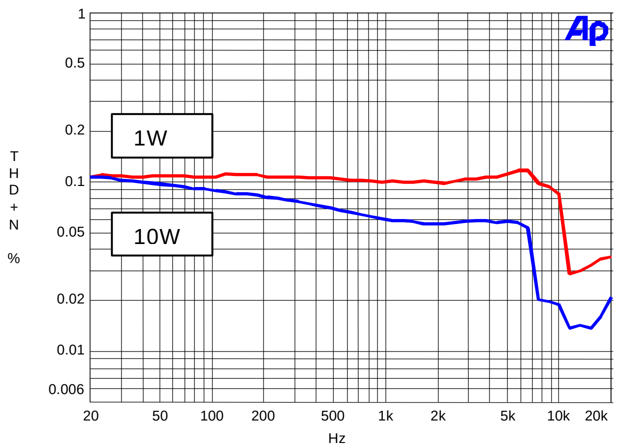
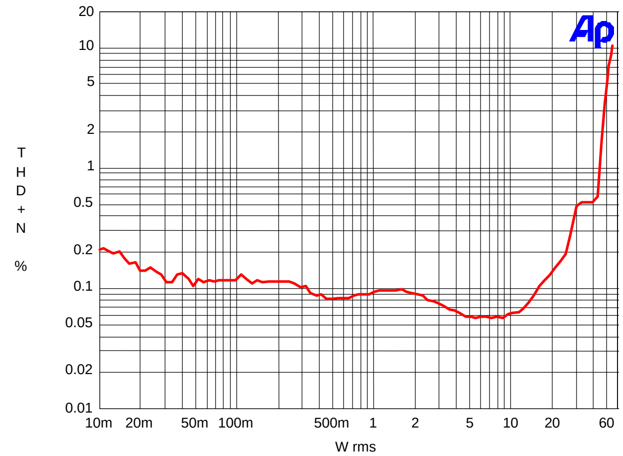


Fig 9: THD+N vs Outpwr at 1 KHz
(w/ ANTICLIPPING DISABLED)



Typical Performance Characteristics at Vcc = 28V, 4 Ohm load, configured for Mono.

Fig 10: THD+N vs Frequency

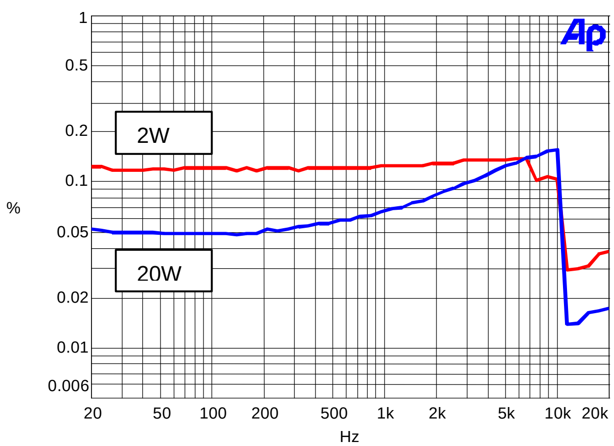


Fig 11: THD+N vs Outpwr at 1 KHz
(w/ ANTICLIPPING DISABLED)

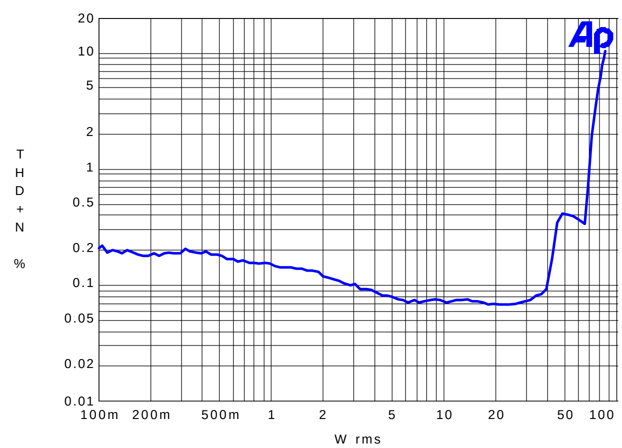


FIGURE 12 - DDX EVALUATION AMPLIFIER ASSEMBLY DRAWING