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AS95L2100

Product Brief

Resilient Packet Ring Controllers™

Overview

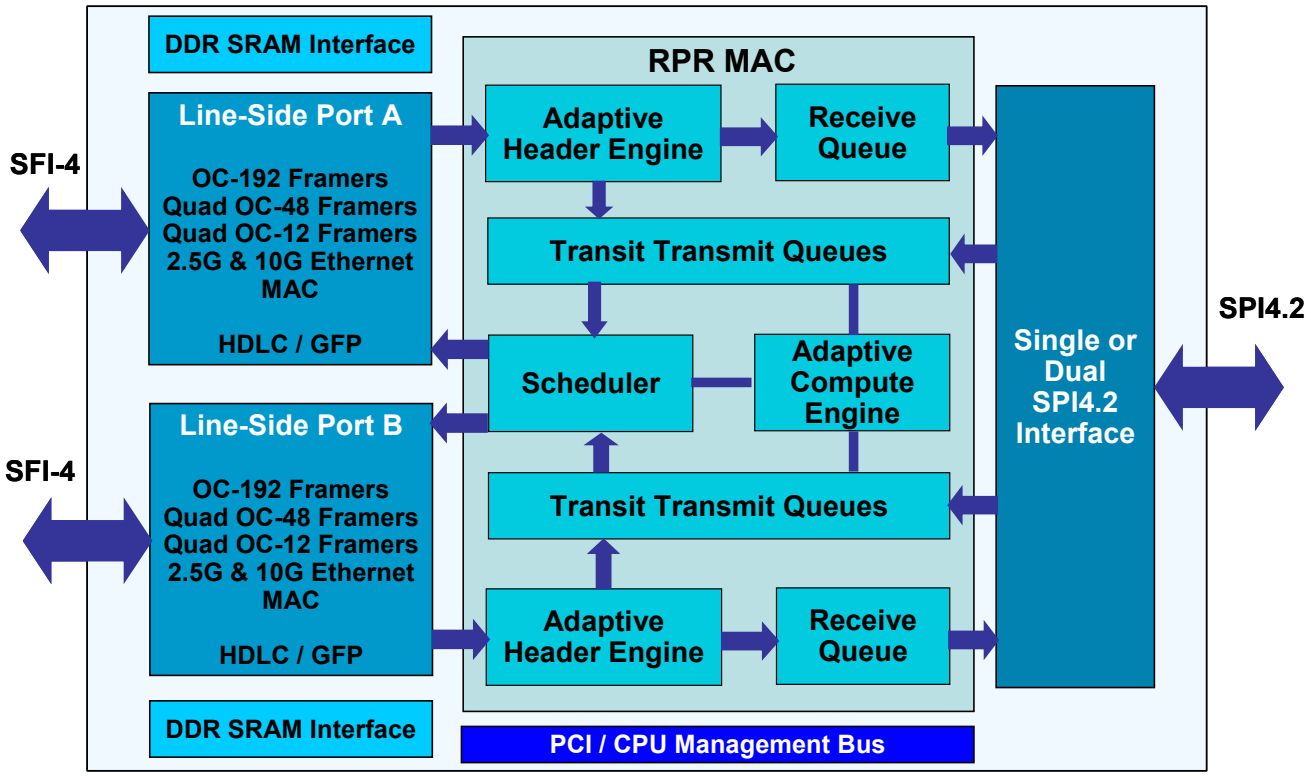
The AS95L2100 family of Resilient Packet Ring Controllers is especially designed to support the emerging IEEE 802.17 Resilient Packet Ring (RPR) standard at various line interface speeds including OC-12, OC-48 and OC-192 for SONET, and 2.5G & 10G for Ethernet and PacketPHY.

The AS95L2100 family is based on a unique patented Adaptive Compute Architecture that combines wire-speed processing power with adaptive logic. This technology provides an unparalleled control over hardware and software that enable the same device to be adapted – without performance penalty - to various ring protocols such as the emerging IEEE 802.17 draft 3.x, Cisco's SRP™ and other proprietary protocols.

The RPR Controller family uniquely supports multiple physical interfaces, modes, protocols and standards. The AS95L2100 family incorporates the resilient ring Media Access Control (MAC) along with layer 1 and layer 2 functions that include: SONET framers, Ethernet MACs, POS/HDLC, GFP and WIS frame delineators. The family also integrates on-chip address matching Content Addressable Memory (CAMs), and large buffer memory for insert and high priority transit queues.

The AS95L2100 family includes on-chip configuration, performance and fault-management features that support RPR requirements for Operation, Administration, Maintenance and Provisioning (OAM&P). The AS95L2100 family is ideally suited for a variety of vertical markets including networking, communications, computing, cable infrastructure, servers and storage cluster systems.

Device Block Diagram



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Functional Description

The AS95L2100 family includes three devices based on the same architecture that incorporate the same set of features. They are software compatible and differ in the bandwidth and line rate they support. The AS95L2100 has a 20Gbps bandwidth and supports OC192, OC48 and 10GE line interfaces. The AS95L2102 has 10Gbps max bandwidth and supports OC48 and OC12 line interfaces. The AS95L2101 has 5Gbps max bandwidth and supports OC48, OC12 and 2.5GE line interfaces. Each device is comprised of two major subsystems: the line-side ports and the RPR MAC.

The two line-side ports (A and B) are symmetrical and each incorporates a PHY interface, frame delineation logic, SONET framers, Ethernet MACs and multiplexing logic. They are used to connect the AS95L2100 family to the rings through an external PHY device (Serdes).

The RPR MAC performs the MAC functions and incorporates two Adaptive Header Engines (AHE), each with and address-matching CAM. It also includes protection switching logic and an Adaptive Control Engine (ACE) for executing fairness algorithms and controlling dispatching regimes.

In addition, one or two SPI-4 phase-2 (SPI4.2) client-side ports (depending on the device) are used to connect to a client FPGA or to a Network Processor (NPU). A control plane interface is used to configure and manage the operation of the AS95L2100 Resilient Packet Ring Controllers.

The AS95L2100 family operates in two modes. In standard topology mode (framer mode), it operates as a dual full-duplex Ethernet MAC or as multiple SONET Framers. In ring mode, the AS95L2100 family additionally has all the logic required for packet ring processing, bandwidth management and protection switching.

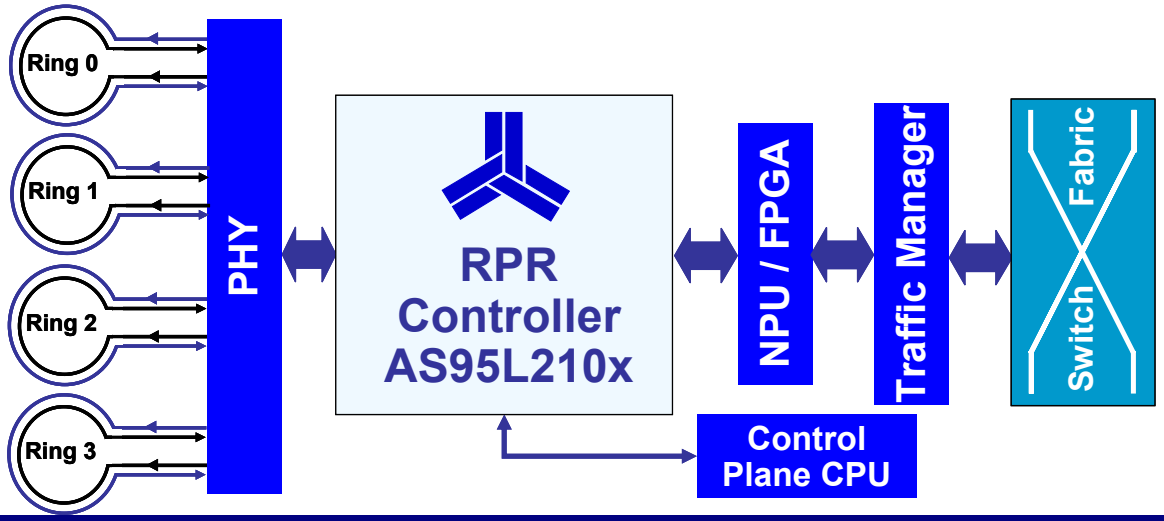
Each packet received on the line-side ports is delineated, processed and reassembled in accordance with the appropriate protocol and framing convention (Ethernet, SONET, GFP, or HDLC) and passed to the AHE. The AHE performs CRC checks and discards or marks corrupt packets. In ring mode it matches the packet's destination address with CAM entries to determine packet routing. Local traffic is stripped from the ring and the packet type is classified as data or control. Local data packets are transferred to the client-side SPI4.2 port for delivery to the application processor. Control packets, consisting of provisioning information, fairness messages, ring status, topology and others are passed to the control plane CPU or to the client-side port for processing.

The AS95L2100 family supports multiple queuing options including single or dual transit buffers with up to three priority classifications (high, medium and low).

The AHE can extract information from encapsulated headers for various frame delineation protocols enabling it to adapt to a wide spectrum of industry and proprietary standards as well as to custom header processing requirements.

The AS95L2100 family of Resilient Packet Ring Controllers operates in either single-line card or dual-line card modes. In single line-card mode, a single device terminates the rings for cost efficiency. In dual-line card mode, two AS95L210x (on two line cards) terminate the rings (one for each ringlet) for redundancy.

Single-Line Card System Block Diagram



Software

A complete Linux-based software kernel driver and user-space API is available that allows for configuration and management of all line and client–side interfaces for the AS95L2100 Resilient Packet Ring Controller family is available.

The driver consists of two logical portions: the main kernel driver that manages the hardware and a kernel "Snap-in" – referred to as Profile – that manages the ring protocol specific features. A different Profile is needed for each of the ring protocols such as IEEE 802.17 Draft 3.x, Cisco's SRP and others. The following figure illustrates the Software modules. The driver also supports the two modes of operation: framer mode and ring mode.

Each Profile consists of two portions: a binary executable file that is directly downloaded to the AS95L2100 family during system initialization; and a host executable that interacts with the Profile and with the main kernel driver.

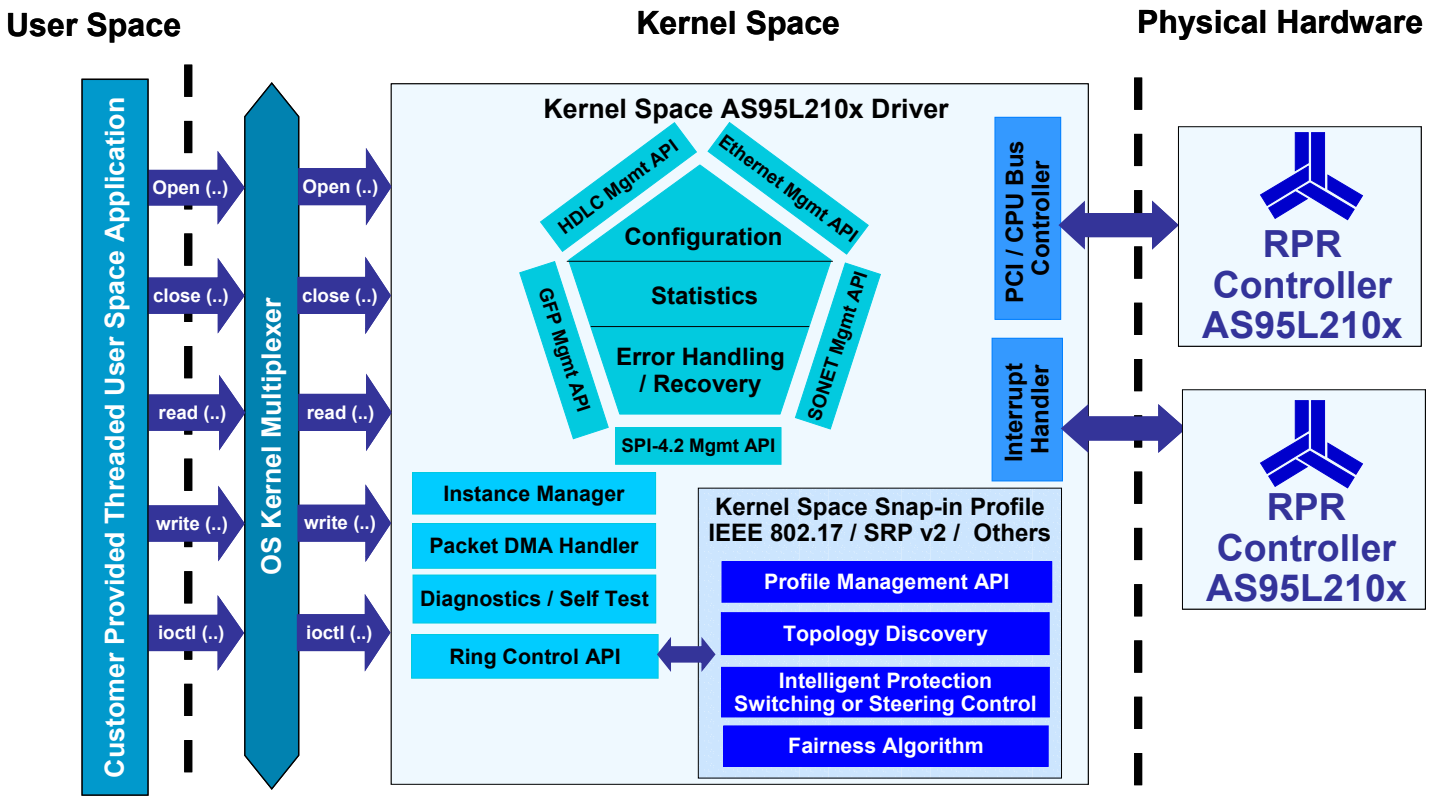
The binary file portion of the Profile contains execution code for the Adaptive Control Engine (running the fairness algorithm). Binary file generation tools and Assembler tools are included as part of the software module.

The Host kernel snap-in executable contains the software to manage the fairness algorithm (running in the Adaptive Control Engine), the topology discovery protocol, the intelligent protection switching and steering control as well as other ring control protocols such as LRTT (Loop Round Trip Time) and FDD (Fairness differential Delay) calculations.

The AS95L2100 family provides a number of on-chip configurations and fault management features that support RPR requirements for Operations, Administration, Maintenance and Provisioning (OAM&P). Equipment manufacturers use these adaptive features to provide more robust and flexible multi-service solutions.

A user-level API tester is provided to allow each driver and ring-level API to be tested. The API tester also provides an easy mechanism to bring up the AS95L2100 family in ring mode or framer mode.

Software Modules



AS95L2100 Family Feature Comparison Table

	AS95L2101	AS95L2102	AS95L2100
Forwarding and processing bandwidth	5Gbps	10Gbps	20Gbps
Client-side interface	1 SPI4.2 port	1 SPI4.2 Port	2 SPI4.2 Ports
Line-side interface	2 Ports (A and B)	2 Ports (A and B)	2 Ports (A and B)
▪ Ethernet MAC per line-side port	2 x 2.5Gbps	N/A	2 x 10Gbps
▪ SONET (STS) / SDH (STM) protocol per line-side port	OC-12 and OC-48	OC-12 and OC-48	OC-48 and OC-192
▪ Frame delineation	POS/HDLC, GFP and Ethernet / PacketPHY	POS/HDLC and GFP	POS/HDLC, GFP and Ethernet / PacketPHY
Ring protocols	IEEE 802.17 draft 2.x Cisco SRP v2 Others	IEEE 802.17 draft 2.x Cisco SRP v2 Others	IEEE 802.17 draft 2.x Cisco SRP v2 Others

* 1 ring = 2 ringlets

Key Features

- Highly integrated device with on-chip SONET Framers (OC12/OC48/OC192), Ethernet MACs (2.5G and 10G) and RPR MAC
- Supports IEEE 802.17 draft 3.x, Cisco SRP v2 and others
- Adaptive compute architecture accommodates modifications and proprietary protocols without performance loss
- Supports packet ring header processing, bandwidth management and protection switching
  - Provides steered and wrapped protection switching (within 50 ms) per IEEE 802.17
- Supports up to 255 nodes per ring
- Up to 20Gbps bandwidth
- Single-line card and dual-line card modes
- Terminates up to 4 rings (8 ringlets)
- SONET/SDH section/line/path processing compliant with Telcordia GR-253, ANSI T1.105, T1.416 and ITU G.751, G.783 and G.804
- Full duplex 2.5-Gbps and 10-Gbps Ethernet MAC processing compliant with IEEE P802.3ae/D5.0
  - WIS (WAN Interface Sub-layer) support for 10-Gbps Ethernet Serial WAN applications
- Compliant with POS/HDLC IETF RFC 1662 and IETF RFC 2615
- SONET/SDH framers defined by IETF RFCs 2615 / 1662 and GFP framers defined by ANSI T1X1.5
- RMON counters comply with IETF RFC 2863 (802.3 MIBs)
- Supports the Generic Framing Procedure (GFP) encapsulation per ANSI T1.105.02 (SONET) and ITU-T G.709 (OTN)
- On-chip memory for high-priority transit traffic buffer and staging buffer for insert traffic
  - On-chip CAM for address matching
- Interface for external SRAM for medium & low priority transit traffic
- The control plane interface can be configured either as a 32-bit PCI bus or as a generic 16-bit CPU bus
- 928-pin HSBGA package

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