Touch Screen Controller

Description

The APT7843 Touch Screen Controller IC provides all the screen drive , A/D converter and control circuits to easily interface to 4 wire resistive touch screen. The IC continually monitors the screen waiting for a touch. When the screen touched , the IC performs A/D converter to determine the location of touch. Also , this device has 2 auxiliary input to A/D converter , allowing for the measurement of other inputs such as battery voltage.

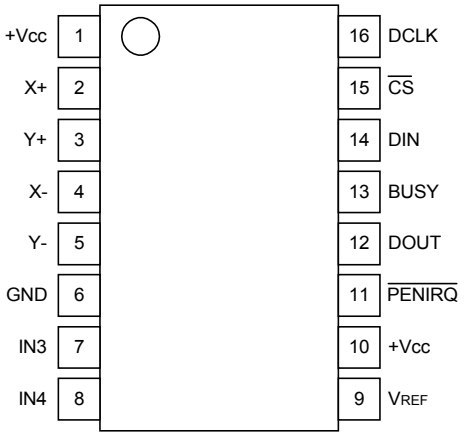
Applications

- PDAs
- Handheld computer
- Touch-screen kiosks

Features

- 16 pin SSOP or TSSOP
- Operates with four wire touch screen
- 8-bit or 12 bit A/D converter
- Ratiometric Conversion eliminates screen calibration
- 2 auxiliary analog inputs
- 4 wire serial interface
- Full power down control

Pin Assignment



Order Information

APT7843 □□

Temp. Range

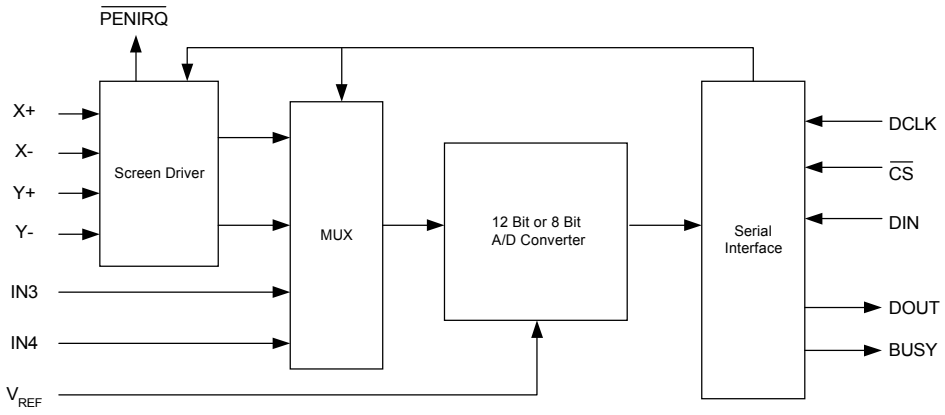
Package Code

Package Code
N : SSOP O : TSSOP
Temp. Range
I : - 40 to 85°C

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Rev. A.8 - Apr., 2002

Block Diagram



Pin Descriptions

PIN	NAME	DESCRIPTION
1	+Vcc	Power Supply,2.2V to 5V.
2	X+	Connect to X+ on touch screen.
3	Y+	Connect to Y+ on touch screen.
4	X-	Connect to X- on touch screen.
5	Y-	Connect to Y- on touch screen.
6	GND	Ground
7	IN3	Auxiliary Input of A/D converter.
8	IN4	Auxiliary input of A/D converter.
9	V_{REF}	Voltage Reference Input.
10	+Vcc	Power Supply,2.2V to 5V.
11	$\overline{PENIRQ}$	Pen interrupt. Open anode output (requires 10kΩ to 100kΩ pull-up resistor externally)
12	DOUT	Serial Data Output. This output is high impedance when $\overline{CS}$ is HIGH.
13	BUSY	Busy Output. This output is high impedance when $\overline{CS}$ is HIGH.
14	DIN	Serial Data input.
15	$\overline{CS}$	Chip Select. (Active Low)
16	DCLK	Serial Clock.

Electrical Characteristics

At T_A = -40°C to 85°C , V_{CC} = +2.7V , V_{REF} = +2.5V , f_{SAMPLE} = 125kHz , f_{CLK} = 16 • f_{SAMPLE} = 2MHz , 12-bit mode , and digital inputs = GND or V_{cc} , unless otherwise noted.

PARAMETER	CONDITIONS	APT7843			UNITS
		MIN	TYP	MAX	
DC ACCURACY					
Resolution			12		Bits
No missing code		11			Bits
Integral Nonlinearity				± 2	LSB
Offset Error				± 6	LSB
Offset Error Match			0.1	1	LSB
Gain Error				± 4	LSB
Gain Error Match			0.1	1	LSB
Noise			30		uV rms
Power Supply Rejection			70		dB
REFERANCE INPUT					
V_{REF} Input Voltage Range		1.0		Vcc	
DC Leakage Current			± 1		µA
V_{REF} Input Impedance	$\overline{CS}$ = GND or Vcc		5		GΩ
V_{REF} Input Current			13	40	µA
	F_{SAMPLE} = 12.5 kHz		2.5		µA
	$\overline{CS}$ = Vcc			3	µA
DYNAMIC PERFORENCE					
Aperture Delay			30		ns
Aperture Jitter			100		ps
Channel to Channel Isolation	V_{IN} = 2.5Vp-p ; F_{IN} = 50kHz		100		dB
CONVERSION RATE					
Conversion Time				12	DCLK cycles
Track/Hold Acquisition Time		3			DCLK cycles
Throughput Rate				125	KSPS
SWITCH DRIVERS					
On-Resistance					
Y+ , X+			4	15	Ω
Y- , X-			4	15	Ω
LOGIC OUTPUTS					
Output High Voltage , V_{OH}	$\|I_{OH}\| \leq$ -250µA	Vcc–0.2			V
Output Low Voltage , V_{OL}	$\|I_{OL}\| \leq$ 250µA			0.4	V
$\overline{PENIRQ}$ output low voltage , V_{OL}				0.2	V
Floating-State Leakage Current				± 10	µA
Floating-State Output Capacitance				10	pF
Output Coding		Straight (Natural) Binary			

Note : (1) LSB means least Significant Bit. With V_{REF} equal to +2.5V , one LSB is 610µV

Electrical Characteristics (Cont.)

PARAMETER	CONDITIONS	APT7843			UNITS
		MIN	TYP	MAX	
LOGIC INPUTS					
Input High Voltage , V_{INH}	$\|I_{INH}\| \leq +5\mu A$	2.4			V
Input Low Voltage , V_{INL}	$\|I_{INL}\| \leq +5\mu A$			0.8	V
Input Current , I_{IN}				± 1	µA
Input Capacitance , C_{IN}				10	pF
ANALOG INPUT					
Input Voltage Ranges		0		V_{REF}	Volts
DC Leakage Current			± 0.1		µA
Input Capacitance			30		pF
POWER REQUIREMENTS					
Vcc		2.7		3.6	V
Icc	Digital I/Ps =0V or Vcc				
Normal Mode (Static)	Vcc = 3.6V			650	µA
Normal Mode (F_{SAMPLE} = 12.5kSPS)	Vcc = 3.6V			540	µA
Shutdown Mode(Static)				3	µA
Showdown	Vcc = 3.6V			3.6	µW

Electrical Characteristics

At T_A = -40°C to 85°C, V_{CC} = +2.4V , V_{REF} don't care, f_{SAMPLE} = 1.25KHz, f_{CLK} = 16 • f_{SAMPLE} = 20KHz, 8-bit differential mode, no support single end mode, and digital inputs = GND or V_{cc} , unless otherwise noted.

PARAMETER	CONDITIONS	APT7843			UNITS
		MIN	TYP	MAX	
DC ACCURACY					
Resolution			8		Bits
No missing code		7			Bits
Integral Nonlinearity				± 2	LSB
Offset Error				± 6	LSB
Offset Error Match			0.1	1	LSB
Gain Error				± 4	LSB
Gain Error Match			0.1	1	LSB
Noise			30		uV rms
Power Supply Rejection			70		dB
DYNAMIC PERFORENCE					
Aperture Delay			30		ns
Aperture Jitter			100		ps
Channel to Channel Isolation	V_{IN} = 2.5Vp-p ; F_{IN} = 50kHz		100		dB
CONVERSION RATE					
Conversion Time				12	DCLK cycles
Track/Hold Acquisition Time		3			DCLK cycles
Throughput Rate				1.25	KSPS
SWITCH DRIVERS					
On-Resistance					
Y+ , X+				4	Ω
Y- , X-				4	Ω
LOGIC OUTPUTS					
Output High Voltage , V_{OH}	$\|I_{OH}\| \le$ -250µA	Vcc–0.2			V
Output Low Voltage , V_{OL}	$\|I_{OL}\| \le$ 250µA			0.4	V
$\overline{\text{PENIRQ}}$ output low voltage , V_{OL}				0.2	V
Floating-State Leakage Current				± 10	µA
Floating-State Output Capacitance				10	pF
Output Coding		Straight (Natural) Binary			

Electrical Characteristics (Cont.)

PARAMETER	CONDITIONS	APT7843			UNITS
		MIN	TYP	MAX	
LOGIC INPUTS					
Input High Voltage , V_{INH}	$\|I_{INH}\| \leq +5\mu A$	2.2		$V_{DD}+0.2$	V
Input Low Voltage , V_{INL}	$\|I_{INL}\| \leq +5\mu A$			0.6	V
Input Current , I_{IN}				± 1	µA
Input Capacitance , C_{IN}				10	pF
ANALOG INPUT					
Input Voltage Ranges		0		V_{REF}	Volts
DC Leakage Current			± 0.1		µA
Input Capacitance			30		pF
POWER REQUIREMENTS					
Vcc		2.2	2.4	3.6	V
Icc	Digital I/Ps =0V or Vcc				
Normal Mode (Static)	Vcc = 2.4V		280	650	µA
Normal Mode (F_{SAMPLE} = 12.5kSPS)	Vcc = 2.4V			540	µA
Shutdown Mode(Static)				3	µA
Showdown	Vcc = 2.4V			3.6	µW

Chip Overview

The APT7843 is a successive approximation analog-to-digital (A/D) converter based around a capacitive redistribution DAC. Figure 1 show basic operation of the APT7843.
The APT7843 communicates via a 4-wire serial interface. The device also requires an external reference voltage Vref. The value of the reference voltage directly sets the input range of the converter.

The APT7843 primary function is to control resistive touchscreens. When a touch is detected , pen interrupt pin will go low to wake up extenal microprocess. The microprocessor writes register to initiate conversion.
This A/D converter may also be used to measure voltage presented on the IN3 , IN4 pins.

Analog Input

The analog input to the converter is provided via a four-channel multiplexer. Figure 2 shows a simplified diagram of the APT7843 with the difference input of the A/D converter , and the converter's reference. Table I and Table II also show the relationship between the A2 , A1 , A0 , SER/$\overline{\text{DFR}}$ and the configuration of the APT7843. See the section of single-ended reference mode and differential reference mode for more details.

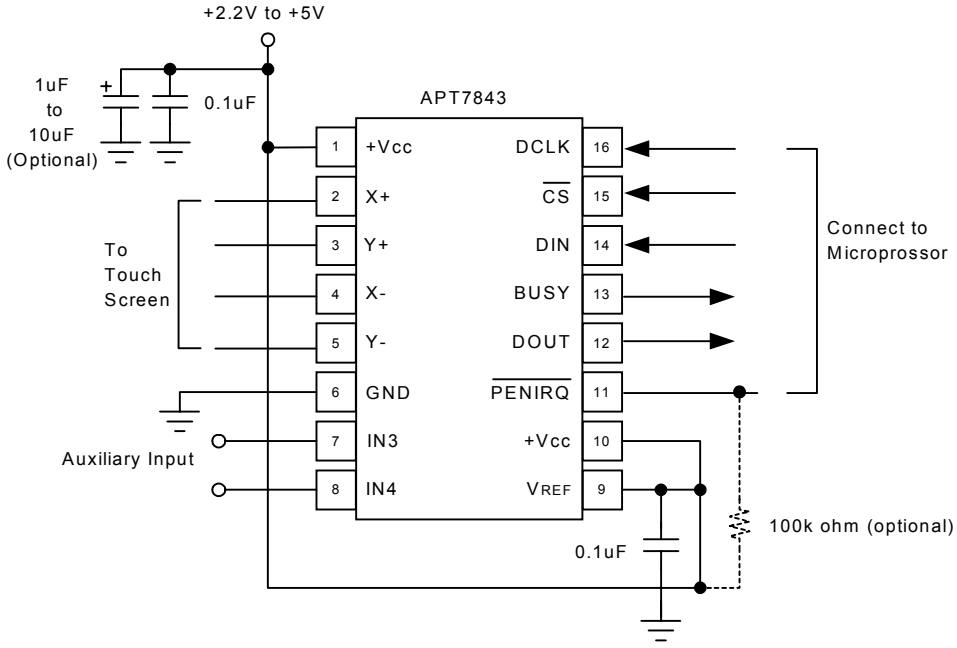


FIGURE 1. Basic Operation of the APT7843

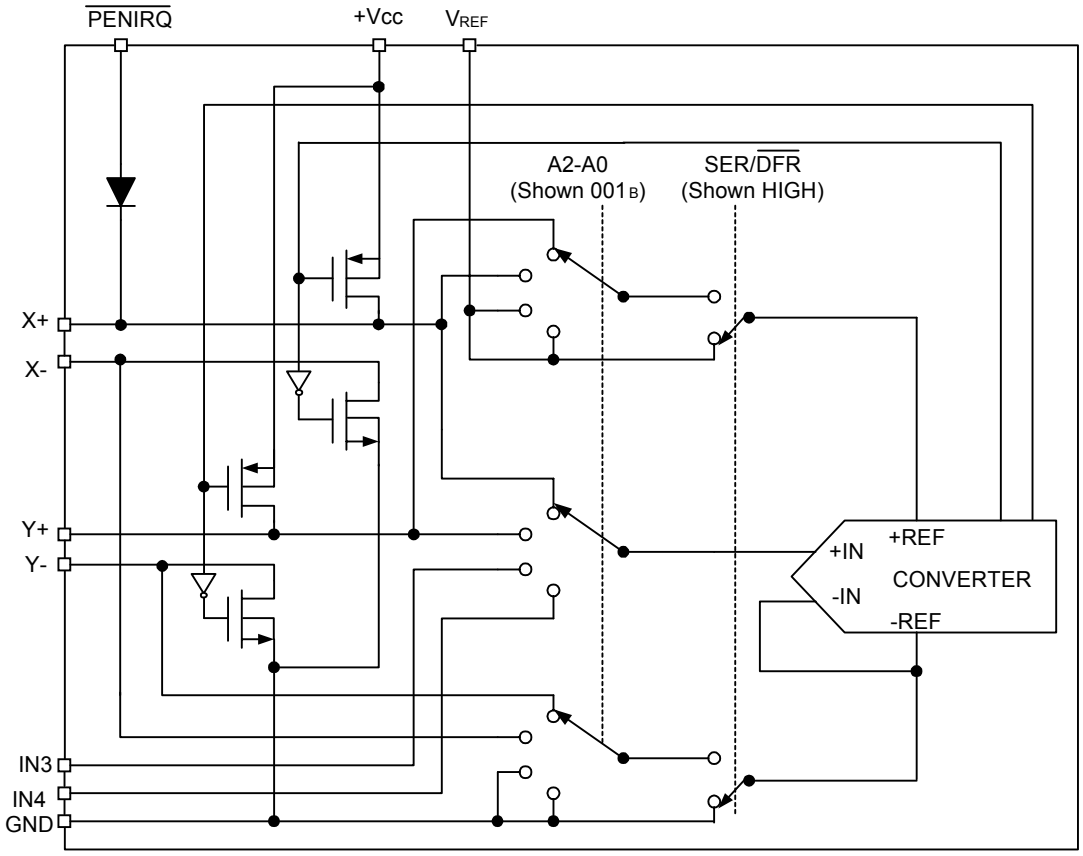


FIGURE 2. Simplified Diagram of Analog Input

A2	A1	A0	X+	Y+	IN3	IN4	-IN	X SWITCHES	Y SWITCHES	+REF	-REF
0	0	1	+IN				GND	OFF	ON	$+V_{REF}$	GND
1	0	1		+IN			GND	ON	OFF	$+V_{REF}$	GND
0	1	0			+IN		GND	OFF	OFF	$+V_{REF}$	GND
1	1	0				+IN	GND	OFF	OFF	$+V_{REF}$	GND

TABLE I. Input C onfiguration, Single-Ended Reference Mode (SER/$\overline{DFR}$ HIGH).

A2	A1	A0	X+	Y+	IN3	IN4	-IN	X SWITCHES	Y SWITCHES	+REF	-REF
0	0	1	+IN				-Y	OFF	ON	+Y	-Y
1	0	1		+IN			-X	ON	OFF	+X	-X
0	1	0			+IN		GND	OFF	OFF	$+V_{REF}$	GND
1	1	0				+IN	GND	OFF	OFF	$+V_{REF}$	GND

TABLE II. Input Configuration, Differential Reference Mode (SER/$\overline{DFR}$ LOW).

Single-Ended reference mode

Figure 3 shows the diagram of single-ended reference mode.

This application shows the measurement of current Y poisition is made by connecting the X+ input to the A/D converter, turning on the Y+ and Y- drivers, and digitizing the voltage on X+ . For this measurement, the resistance in the X+ lead does not affect the conversion. However, since the resistance between Y+ and Y- is fairly low, the on-resistance of the Y drivers does make a small difference. Under the situation outlined so far, it would not be possible to achieve a zero volt input or a full-scale input regardless of where the pointing device is on the touch screen because some voltage is lost across the internal switches. This situation can be remedied if use differential reference mode

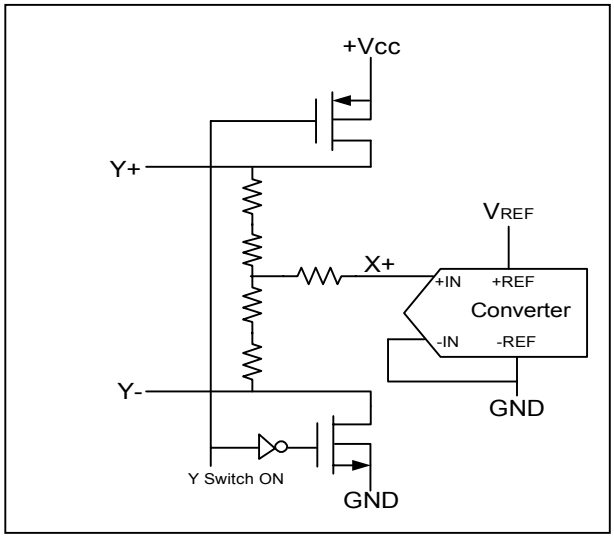


FIGURE 3.Single-Ended Reference Mode
(SER/$\overline{DFR}$ High, A2=Low,A1=Low,A0=High)

Differential reference mode

As shown in Figure 4,by setting the SER/$\overline{DFR}$ bit LOW, the +REF and -REF inputs are connected directly to Y+ and Y-. This makes the analog-to- digital conversion ratiometric.

The result of the conversion is always a percentage of the external resistance, reardless of how it changes in relation to the on-resistance of the internal switches. Note that there is an important consideration regarding power dissipation when using the ratiometric mode of operation,the external device should powered throughout the acquisition and conversion periods.

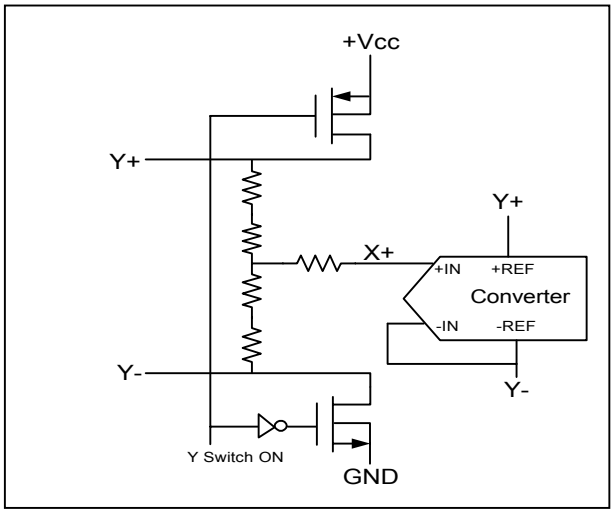


Figure 4. Differential Reference Mode
(SER/$\overline{DFR}$ LOW, A2=Low,A1=Low,A0=High)

Serial Interface

Data is written to,and read from , the APT7843 via the serial port. The serial port has 4 pins - serial clock (DCLK),chip select ($\overline{CS}$) ,data in (DIN) and data out (DOUT). The DCLK acts on the rising edge. The $\overline{CS}$ acts as a reset for the serial port with $\overline{CS}$ goes low initating a conversion cycle. The cycle consists of 2 parts - a write followed by a read. Figure 5 shows the typical timing of the APT7843's serial interface. A total of 24 clock cycles will complete one conversion.

Also shown in Figure 5 is the placement and order of the control bits within the control byte. Tables III and IV give detailed information about these bits.

The first bit, the 'S' bit, must always be HIGH and indicates the start of the control byte. The APT7843 will ignore inputs on the DIN pin until the start bit S detected.

The next three bits (A2 - A0) select the active input channel or channels of the input multiplexer (see Tables I and II and Figure 2).

The MODE bit determines the number of bits for each conversion, either 12 bits (LOW) or 8 bits (HIGH).

The SER/$\overline{DFR}$ bit controls the reference mode: either single-ended (HIGH) or differential (LOW). (The differential mode is also referred to as the ratiometric conversion mode.)

The last two bits (PD1 - PD0) select the power- down mode as shown in Table V. If both inputs are HIGH, the device is always powered up. If both inputs are LOW, the device enters a power-down mode between conversions.

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
S	A2	A1	A0	MODE	SER/$\overline{\text{DFR}}$	PD1	PD0

TABLE III. Order of the Control Bits in the Control Byte.

BIT	NAME	DESCRIPTION
7	S	Start Bit. Control byte starts with first HIGH bit on DIN. A new control byte can start every 15th clock cycle in 12-bit conversion mode or every 11th clock cycle in 8-bit conversion mode.
6-4	A2-A0	Channel Select Bits. Along with the SER/$\overline{\text{DFR}}$ bit, these bits control the setting of the multiplexer input, switches, and reference inputs, as detailed in Tables I and II.
	MODE	12-Bit/8-Bit Conversion Select Bit. This bit controls the number of bits for the following conversion: 12-bits(LOW) or 8-bits(HIGH).
2	SER/$\overline{\text{DFR}}$	Single-Ended/Differential Reference Select Bit. Along with bits A2-A0, this bit controls the setting of the multiplexer input, switches, and reference inputs, as detailed in Tables I and II.
1-0	PD1-PD0	Power-Down Mode Select Bits. See Table V for details.

TABLE IV. Descriptions of the Control Bits within the Control Byte.

PD1	PD0	PENIRQ	DESCRIPTION
0	0	Enabled	Power-down between conversions. When each conversion is finished, the converter enters a low power mode.
0	1	Enabled	Reserved for future use
1	0	Enabled	Reserved for future use.
1	1	Disabled	No power-down between conversions, device is always powered.

TABLE V. Power-Down Selection.

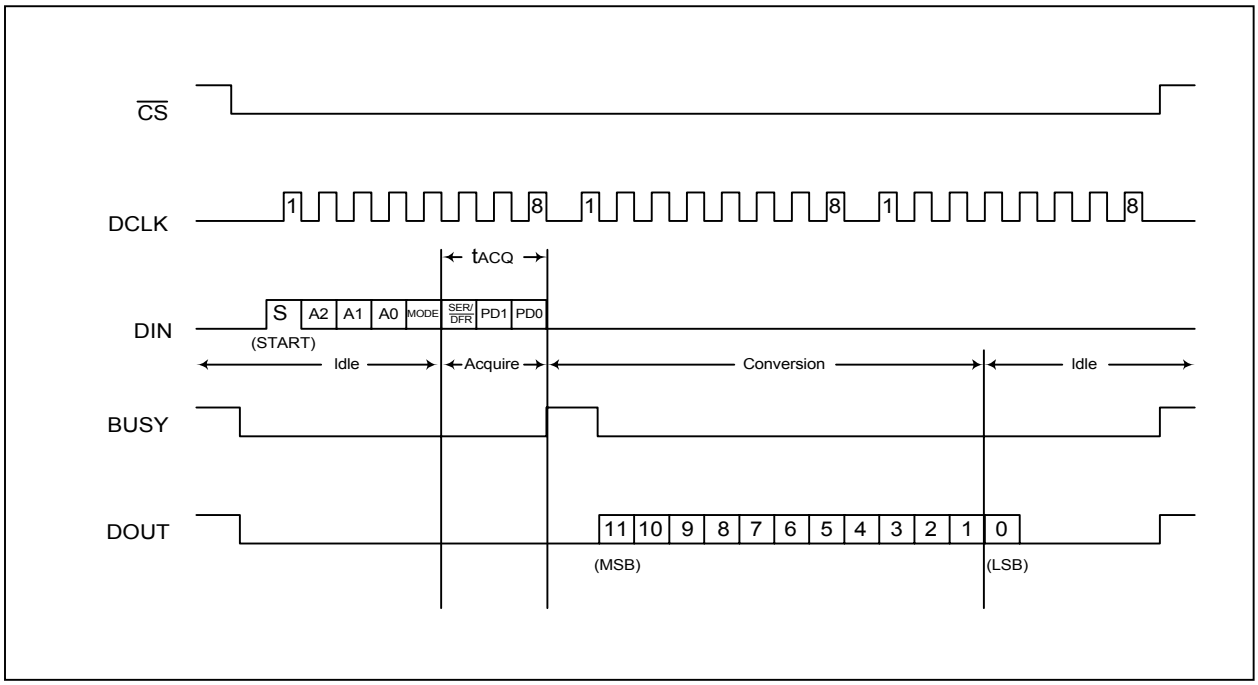


FIGURE 5. Conversion Timing, 24-Clocks per Conversion, 8-bit Bus Interface. No DCLK Delay Required with Dedicated Serial Port.

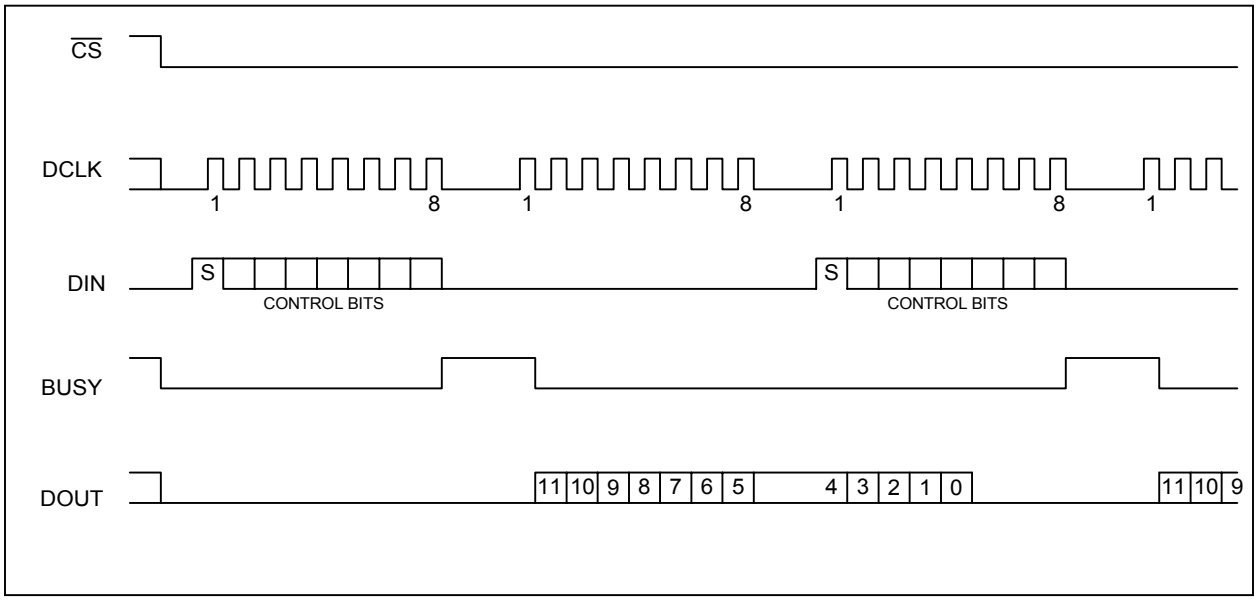


FIGURE 6. Conversion Timing, 16-Clocks per Conversion, 8-bit Bus Interface. No DCLK Delay Required with Dedicated Serial Port.

16-Clocks or 15-Clocks per Conversion

The APT7843 will alow a conversion every 16 clock cycles, as shown in Figure 6. This figure shows possible serial communication occurring with other serial peripherals between each byte transfer between the processor and the converter.

Figure 7 provides the fastest way to clock the APT7843. This method will not work with the serial interface of most microcontrollers and digital signal processors as they are generally not capable of providing 15 clock cycles per serial transfer. However, this method could be used with field programmable gate arrays (FPGAs) or application specific integrated circuits (ASICs). (Note that this effectively increases the maximum conversion rate of the converter).

AC Timing

Figure 8 and Table VI provide detailed timing of the APT7843. Table VII provide detailed timing of low power V_{CC}=2.4V.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{ACQ}	Acquisition Time	1.5			µs
t_{DS}	DIN Valid Prior to DCLK Rising	100			ns
t_{DH}	DIN Hold After DCLK HIGH	10			ns
t_{DO}	DCLK Falling to DOUT Vaild			200	ns
t_{DV}	$\overline{CS}$ Falling to DOUT Enabled			200	ns
t_{TR}	$\overline{CS}$ Rising to DOUT Disabled			200	ns
t_{CSS}	$\overline{CS}$ Falling to DCLK Rising	100			ns
t_{CSH}	$\overline{CS}$ Rising to DCLK Ignored	0			ns
t_{CH}	DCLK HIGH	200			ns
t_{CL}	DCLK LOW	200			ns
t_{BD}	DCLK Falling to BUSY Rising			200	ns
t_{BDV}	$\overline{CS}$ Falling to BUSY Enabled			200	ns
t_{BTR}	$\overline{CS}$ Rising to BUSY Disable			200	ns

TABLE VI. Timing Specifications (+Vcc=+2.7V and Above, T_A=-40°C to +85°C, C_{LOAD}=50pF).

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{ACQ}	Acquisition Time	20			µs
t_{DS}	DIN Valid Prior to DCLK Rising	400			ns
t_{DH}	DIN Hold After DCLK HIGH	20			ns
t_{DO}	DCLK Falling to DOUT Vaild			400	ns
t_{DV}	$\overline{CS}$ Falling to DOUT Enabled			400	ns
t_{TR}	$\overline{CS}$ Rising to DOUT Disabled			400	ns
t_{CSS}	$\overline{CS}$ Falling to DCLK Rising	200			ns
t_{CSH}	$\overline{CS}$ Rising to DCLK Ignored	0			ns
t_{CH}	DCLK HIGH	2.5			µs
t_{CL}	DCLK LOW	2.5			µs
t_{BD}	DCLK Falling to BUSY Rising			400	ns
t_{BDV}	$\overline{CS}$ Falling to BUSY Enabled			400	ns
t_{BTR}	$\overline{CS}$ Rising to BUSY Disable			400	ns

TABLE VI. Timing Specifications (+Vcc=+2.4V and Above, T_A=-40°C to +85°C, C_{LOAD}=50pF).

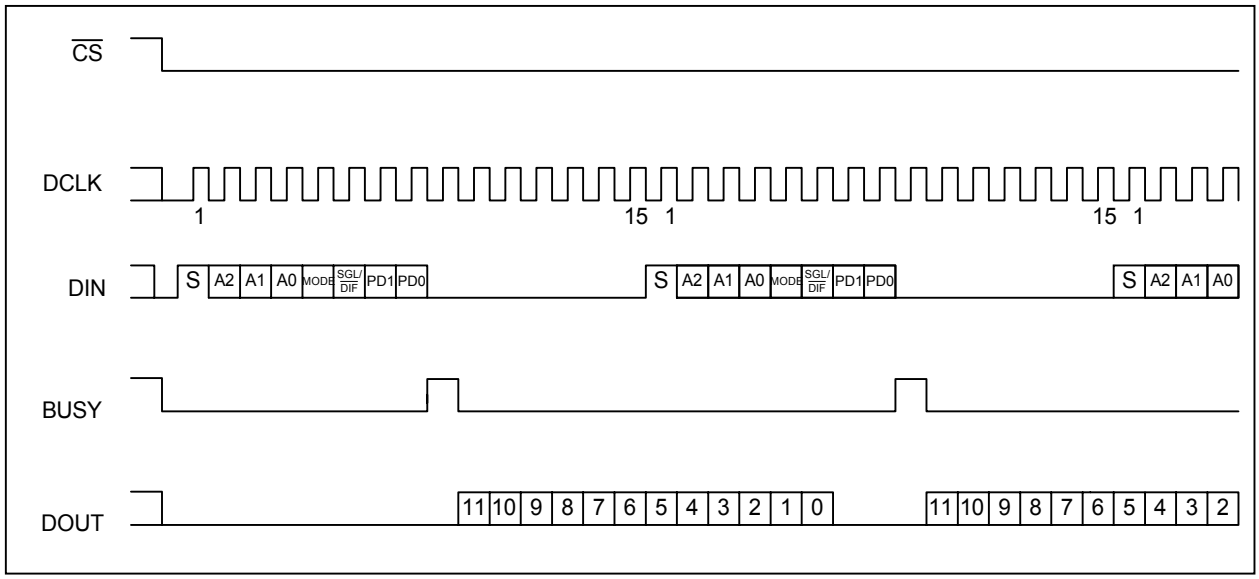


FIGURE 7. Maximum Conversion Rate, 15-Clocks per Conversion.

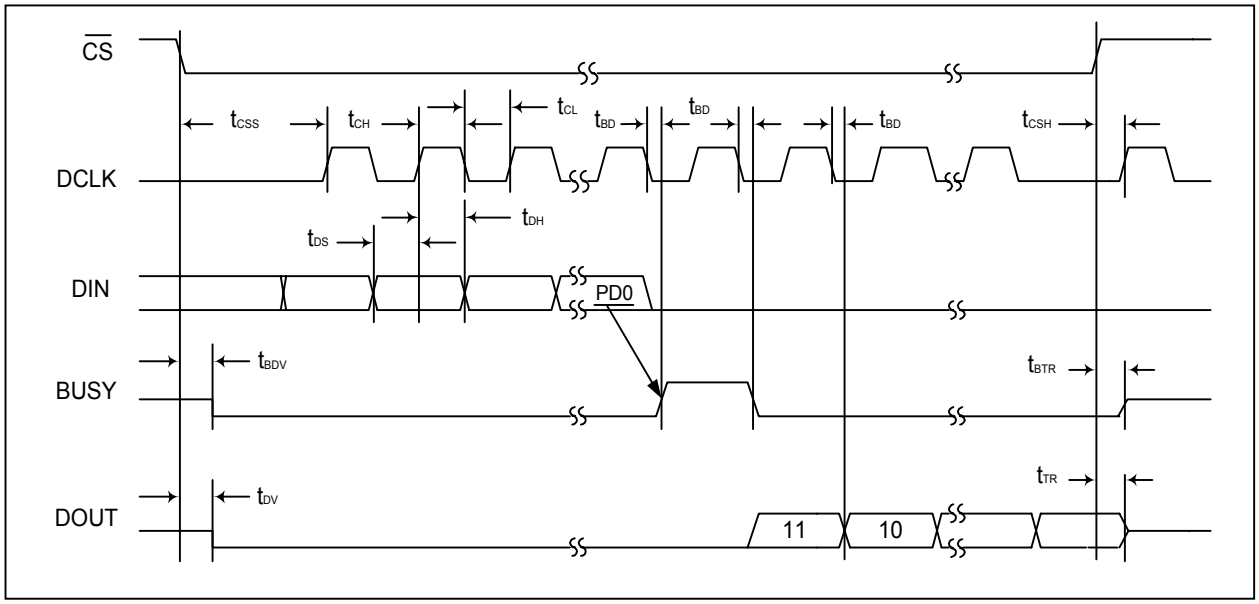
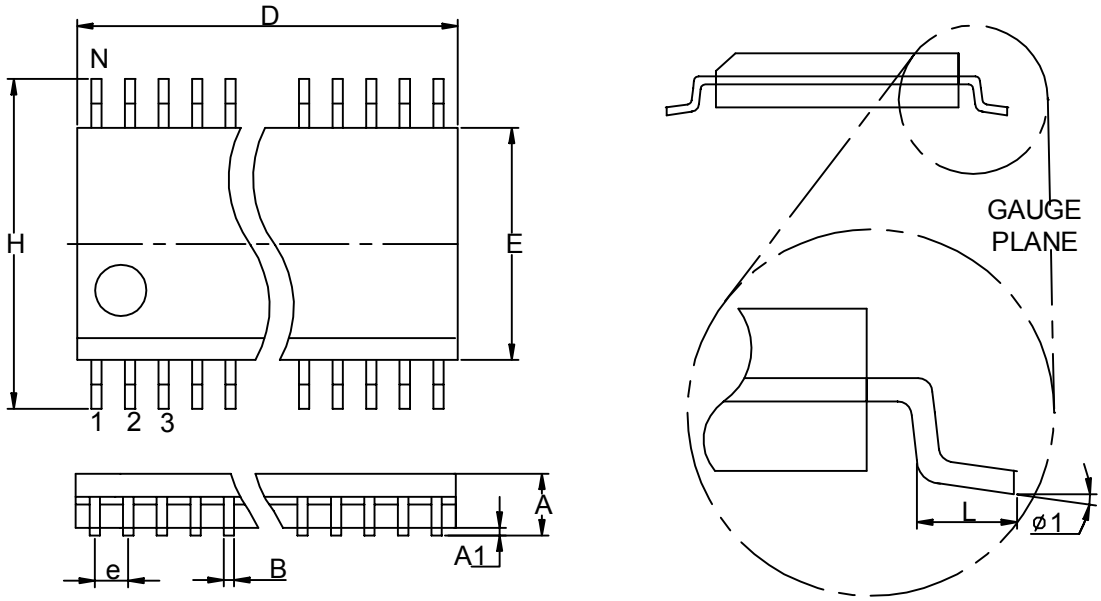


FIGURE 8. Detailed Timing Diagram.

Packaging Information

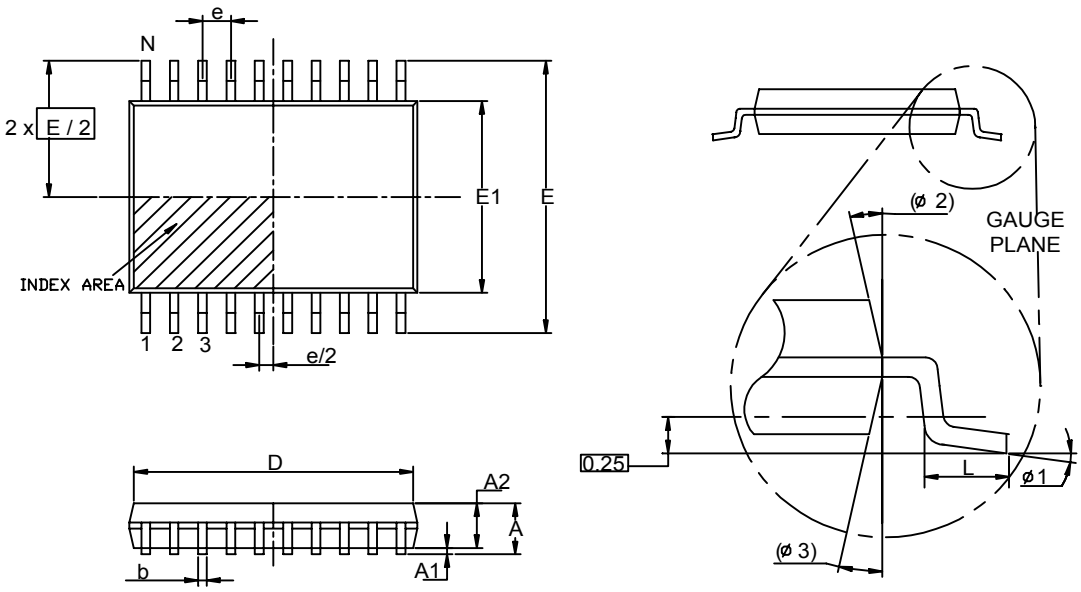
SSOP



Dim	Millimeters		Variations- D			Dim	Inches		Variations- D		
	Min.	Max.	Variations	Min.	Max.		Min.	Max.	Variations	Min.	Max.
A	1.350	1.75	SSOP-16	4.75	5.05	A	0.053	0.069	SSOP-16	0.187	0.199
A1	0.10	0.25				A1	0.004	0.010			
B	0.20	0.30				B	0.008	0.012			
D	See variations					D	See variations				
E	3.75	4.05				E	0.147	0.160			
e	0.625 TYP.					e	0.025 TYP.				
H	5.75	6.25				H	0.226	0.246			
L	0.4	1.27				L	0.016	0.050			
N	See variations					N	See variations				
ϕ 1	0°	8°				ϕ 1	0°	8°			

Packaging Information

TSSOP

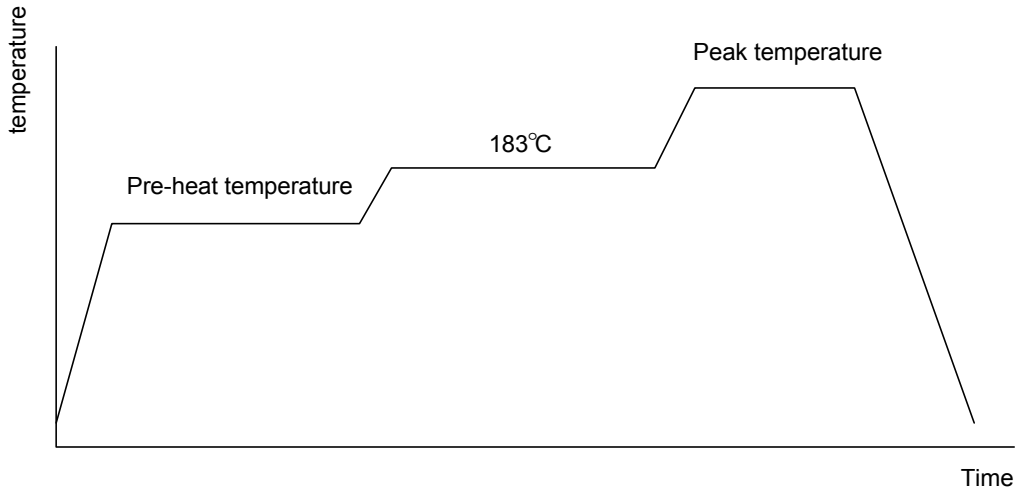


Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A		1.2		0.047
A1	0.00	0.15	0.000	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.011
D	4.9 (N=16PIN) 6.4 (N=20PIN) 7.7 (N=24PIN) 9.6 (N=28PIN)	5.1 (N=16PIN) 6.6 (N=20PIN) 7.9 (N=24PIN) 9.8 (N=28PIN)	0.193 (N=16PIN) 0.252 (N=20PIN) 0.303 (N=24PIN) 0.378 (N=28PIN)	0.201 (N=16PIN) 0.260 (N=20PIN) 0.311 (N=24PIN) 0.386 (N=28PIN)
e	0.65 BSC		0.026 BSC	
E	6.40 BSC		0.252 BSC	
E1	4.30	4.50	0.169	0.177
L	0.45	0.75	0.018	0.030
ϕ1	0°	8°	0°	8°
ϕ2	12° REF		12° REF	
ϕ3	12° REF		12° REF	

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb)
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classification Reflow Profiles

	Convection or IR/ Convection	VPR
Average ramp-up rate(183°C to Peak)	3°C/second max.	10 °C /second max.
Preheat temperature 125 ± 25°C)	120 seconds max	
Temperature maintained above 183°C	60 – 150 seconds	
Time within 5°C of actual peak temperature	10 –20 seconds	60 seconds
Peak temperature range	220 +5/-0°C or 235 +5/-0°C	215-219°C or 235 +5/-0°C
Ramp-down rate	6 °C /second max.	10 °C /second max.
Time 25°C to peak temperature	6 minutes max.	

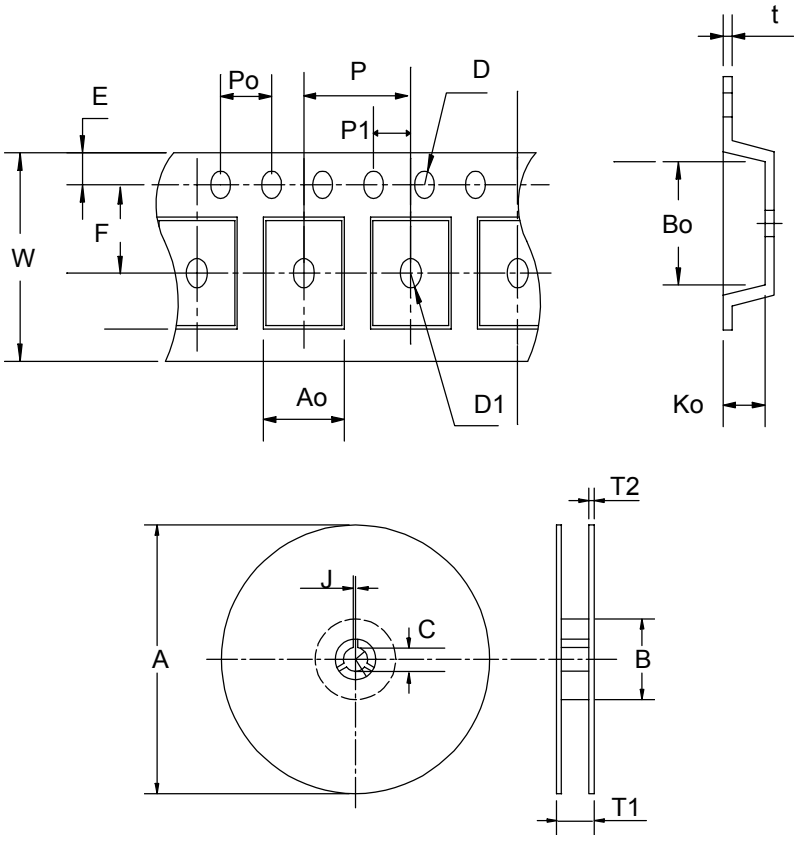
Package Reflow Conditions

pkg. thickness ≥ 2.5mm and all bgas	pkg. thickness < 2.5mm and pkg. volume ≥ 350 mm³	pkg. thickness < 2.5mm and pkg. volume < 350mm³
Convection 220 +5/-0 °C		Convection 235 +5/-0 °C
VPR 215-219 °C		VPR 235 +5/-0 °C
IR/Convection 220 +5/-0 °C		IR/Convection 235 +5/-0 °C

Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C,5 SEC
HOLT	MIL-STD 883D-1005.7	1000 Hrs Bias @ 125°C
PCT	JESD-22-B, A102	168 Hrs, 100% RH, 121°C
TST	MIL-STD 883D-1011.9	-65°C ~ 150°C, 200 Cycles

Carrier Tape & Reel Dimensions



Application	A	B	D0	D1	E	F	P0	P1	P2
SSOP-14/16	6.95	5.4	1.55±0.05	1.55±0.1	1.75±0.1	5.5±0.05	4.0±0.1	8.0±0.1	2.0±0.05
	T	T2	W	W1	C1	C2	T1	T2	C
	0.3±0.05	2.2	12.0±0.3	9.5	13±0.3	21±0.8	13.5±0.5	2.0±0.2	80±1

(mm)

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