NETWORK SEARCH ENGINE
32K x 72 Entries

Datasheet Brief 75P42100

To request the full IDT75P42100 datasheet, please contact your local IDT Sales Representative or call 1-831-754-4555

Device Description

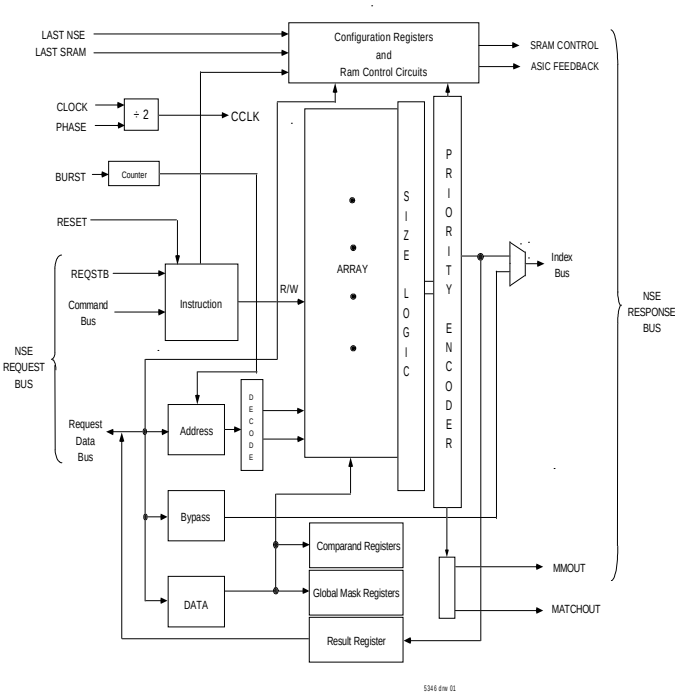
IDT provides proven, industry-leading network search engines (NSEs) and a comprehensive suite of software that enable and accelerate the intelligent processing of network services in communications equipment. As a part of the complete IDT classification subsystem that includes content inspection engines, the IDT family of NSEs delivers high-performance, feature-rich, easy-to-use, integrated search accelerators.

The IDT 75P42100 NSE is a high performance pipelined low-power, synchronous full-ternary 32K x 72 entry device. Each entry location in the NSE has both a Data entry and an associated Mask entry. The NSE devices integrate content addressable memory (CAM) technology with high-performance logic. The device can perform Lookup and Learn NSE operations plus Read, Write, Burst Write, and Dual Write maintenance operations.

The IDT 75P42100 NSE device has a bi-directional bus that is a multiplexed address and data bus that can support 100 million sustained searches per second. This device provides array segments which can be configured to enable multiple width lookups from 36 to 576 bits wide. The IDT 75P42100 requires a 1.8-volt V_{DD} supply, a user selectable 1.8 or 2.5-volt V_{DDQ} supply, and a 2.5-volt V_{BIAS} supply. This NSE device provides the user with flexibility and control in determining the device power. Only the array segments that will be used for a specific NSE operation are powered up while the unused segments are not.

The IDT 75P42100 NSE utilizes the latest high-performance 1.8V CMOS processing technology and is packaged in a JEDEC Standard, thermally enhanced, low profile Ball Grid Array. The options include a 304 BGA, satisfying smaller footprint requirements and a 372 BGA package that is compatible with the IDT 64K x 72 Entry (75P52100) and 128K x 72 Entry (75K62100) NSE devices.

Block Diagram

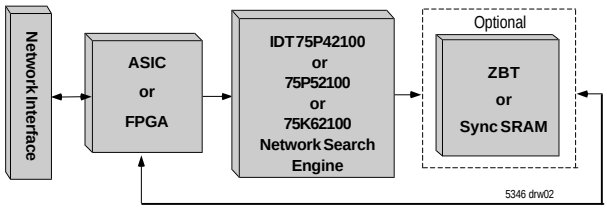


System Configurations

The IDT NSEs are designed to fulfill the needs of various types of networking systems. In solutions requiring data searching such as routers, a system configuration as shown in Figure 1.0 may be realized. Maximum flexibility is provided by allowing one board design to be populated today using either the IDT 75P42100 or 75P52100 NSEs and later upgraded to use IDT's 75K62100 NSE. Applications note AN-279 discusses how to accommodate one board design for any of these NSEs.

In this compatible configuration, the NSE interfaces directly to an ASIC/ FPGA for lookups and routes an Index to an associated SRAM device, which supplies the next hop address via an SRAM Data Bus to the ASIC. The NSE provides the required control signals to directly hookup to ZBT™ or Synchronous Pipeline Burst SRAM. Lookup results can also be fed directly back to the ASIC/ FPGA without the use of external SRAM. Control of the associated handshake signals is provided by all NSEs to adapt to either configuration.

Figure 1.0 ASIC / Compatible NSE / SRAM configuration



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Features

- Full Ternary 32K x 72 bit content addressable memory
- Upgradeable to 64K x 72 and 128K x 72 NSEs
- Power Management
- Global Mask Registers
- Segments individually configurable
- 36/72/144/288/576 multiple width lookups
- 100M sustained lookups per second at 72 and 144 width lookups
- Burst write for high speed table updates
- Multi-match
- Learn new entries
- Dual bus interface
- Cascadable to 8 devices with no glue logic or latency penalty
- Glueless interface to standard ZBT™ or Synchronous Pipelined Burst SRAMs
- Boundary Scan JTAG Interface (IEEE 1149.1compliant)
- 1.8V core power supply
- 2.5V V_{BIAS} power supply
- User selectable 2.5V or 1.8V I/O supply

Functional Highlights

Data and Mask Array

The NSE has Data cell entries and associated Mask cell entries as shown in Fig. 1.1. This combination of Data and Mask cell entries enables the NSE to store 0, 1 or X, making it a full ternary Network Search Engine. During a lookup operation, both arrays are used along with a Global Mask Register to find a match to a requested data word.

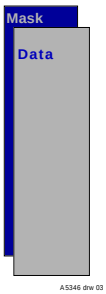

Figure 1.1

Bus Interface

The NSE utilizes a dual bus interface consisting of the NSE Request Bus and the NSE Response Bus.

The NSE Request Bus is comprised of the Command Bus and the Request Data Bus. The Command Bus handles the instruction to the NSE while the Request Data Bus is the main data path to the NSE.

The 72 bit bi-directional Request Data Bus functions as a multiplexed address and data bus, which performs the writing and reading of NSE entries, as well as presenting lookup data to the device.

The NSE Response Bus is comprised of an independent unidirectional Index Bus which drives the result of the lookup (or index) to either an SRAM device or an ASIC. In addition to driving the Index, the NSE Response Bus also drives the associated SRAM control signals ($\overline{CE}$/$\overline{OE}$, and $\overline{WE}$) for either ZBT™ or Synchronous Pipeline Burst SRAM devices.

Command Bus

The Command Bus loads the specific instructions into the NSE. These include:

■ Read or Write

A Read or Write instruction operates on a specified data entry, mask entry, or register.

■ SRAM No Wait Read

An SRAM No Wait Read is a Read instruction to an external SRAM that can be pipelined within a series of operations and does not require the user to wait for the Read to complete before loading the next instruction.

■ Dual Write

In addition to individual writes, the NSE has the ability to perform simultaneous writes to a Data entry and a respective external SRAM location.

■ Lookup

A lookup can be requested in 72-bit, 144-bit, 288-bit or 576-bit widths. A 36-bit lookup can be accomplished by using two Global Mask Registers.

■ Learn

The NSE implements a fully autonomous Learn Instruction, which provides a mechanism for the user to write a lookup entry into an unused location in the NSE and the associated data in external SRAM. This allows the user to update an entry into the NSE which had not previously been stored. The Learn writes the new entry, making it available for future lookups.

SRAM Interface

The NSE provides all required address and control signals for a glueless SRAM interface. The NSE provides a pipelined bypass path for reads or writes to the external SRAM. The ASIC/FPGA handles the pipelining of the data to and from the SRAM.

Registers

There are four basic types of registers supported:

■ Configuration Registers are used at initialization to define the segmentation of the entries, timing of outputs and the SRAM interface.

■ Global Mask Registers are provided to support Lookup instructions by masking individual bits during a search.

■ Comparand Registers assist in the Learn Instruction.

■ Result Registers are used to store the resulting index of a search from a Lookup or Learn operation.

Synchronous Burst Write

The burst write feature has no limit on the number of continuous write accesses and supports initialization of the NSE.

Width Segmentation Capability

The NSEs are capable of performing lookups for comparisons on data structures of 72 bits, 144 bits, 288 bits and 576 bits. These devices has can be configured to meet various system requirements.

- *Single Width Array*
- *Multiple Width Arrays within a Single Device*

Multi Match

The Multi-Match feature signals to the user that more than one match has resulted. The result of the lookup, which defines the highest priority match, is sent along with the Multi-Match signal.

Power Savings and Classification Features

See the full IDT75P42100 Datasheet for more information.

Signal Descriptions

Pin Function		I/O	Description
NSE Request Bus:			
Request Strobe		Input	This input signifies a valid input request and signals the start of an NSE operation cycle.
Command Bus	Instruction	Input	These two fields of the Command bus define the instruction to be performed by the NSE and the lookup type. The lookup type is selected only for operational type commands (Lookups, Learns) and is a "don't care" for maintenance type commands (all Reads and Writes).
	Lookup Type	Input	
	Global Mask Register Select	Input	This field is within the Command bus. During Lookup or Write operations, this field defines which of the Global Mask Register groups are being accessed. This field is a "don't care" for Read, SRAM No Wait Read, and Learn Operations.
	Comparand and Result Register Select	Input	This is a multiplexed field within the Command Bus that specifies both the Result Register to store the Index into, and the Comparand Register to use. This field is sampled every input clock cycle. The first cycle decodes the selected Comparand Register and the second decodes the selected Result Register.
Request Data Bus		Input/Output Three State	The Request Data Bus is a multiplexed address/data bus used to perform reads (and writes) from (to) the NSE, and to present search data for lookups.
NSE Response Bus:			
Index Bus	Address	Output Three State	This bus is used to drive the address of an external SRAM, or feedback Lookup result information directly to the NSE's ASIC/FPGA. The Index Bus contain the encoded location at which the compare was found, the address of the NSE which found the result and the Lookup type.
	Device ID		
	Lookup Type		
Chip Enable/ Output Enable		Output Three State	This signal is driven along with the Index Bus. It is connected to the $\overline{CE}$ input pin of a ZBT SRAM or to the $\overline{OE}$ pin of a PBSRAM.
Write Enable		Output Three State	This signal is driven along with the Index bus. It is used to assert the $\overline{WE}$ pin of an external SRAM. It is active for both SRAM write operations and the Learn command.
Read Acknowledge		Output	This signal is sent back when the data is read from the NSE on the Request Data Bus, or when the data being read from the associated external SRAM.
Match Acknowledge		Output	This is signal is sent with the Index. It will be driven low if there was no match, high if a match was found.
Valid Lookup Bit		Output	This signal is sent with the Index. It will be driven high upon the completion of a lookup, even if the lookup did not result in a hit.
Multi Match Output		Output (Open Drain)	This signal is sent with the Index. It shall go active when a) multiple hits occur in one segment; or, b) one or more hits occur in two (or more) segments; or, c) one or more hits occur in multiple devices that are depth cascaded.
Depth Expansion:			
Device Address		Input	These three DC pins are used to define the Device Address for each of the eight possible depth expanded NSE devices in an NSE system.
Match Input		Input	The Match Input signal is driven by all upstream Match Output signals. This indicates to all down stream NSEs that a hit in a higher priority NSE has occurred.
Match Output		Output	The Match Output signal signifies that a match has occurred in the NSE. The signal is fed into a Match Input line of all lower priority NSE(s).
Clock and Initialization:			
Clock Input		Input	All inputs and outputs are referenced to the positive edge of this clock.
Clock Phase Enable		Input	This signal is used to generate an internal clock at ½ the frequency of the input clock.
Reset		Input	This pin will force all outputs to a high impedence condition, as well as clearing the NSE enable bit.
Advance Burst Address		Input	This signal will advance an internal address counter to allow for burst writes when writing to the Data/Mask memory in the NSE. This provides a mechanism to conveniently initialize the NSE memory.
Last NSE		Input	This pin defines which NSE device will drive the ASIC Feedback signals to the ASIC/FPGA.
Last SRAM		Input	This pin defines which NSE device will drive the SRAM control signals $\overline{CE}$/$\overline{OE}$ and $\overline{WE}$. It also defaults this device to driving the Index Bus when there is no ongoing operation preventing the bus from floating.

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