

Microcontroller with Transponder Interface

The U9280M-H IC is a multi-chip module for remote control and contactless ID systems. It consists of the M44C092 microcontroller and U3280M transponder interface circuit with EEPROM. A coil connected to the transponder interface serves as wireless bidirectional communication interface as well as power supply for the μC and the interface. As transponder, the device is supplied by a magnetic RF field applied at the coil. For IR- or RF-transmitter applications, it can be supplied by a battery. The μC supports with its built-in timers a wide range of IR- and RF-transmission modes such as burst-modulation modes, PWM-, NRZ-, Manchester- and Biphase coding.

Features

- 4-bit HARVARD architecture
- 4 K \times 8-bit application ROM
- 256 \times 4-bit RAM
- 32 \times 16-bit EEPROM
- 10 bidirectional I/Os
- 4 external interrupt inputs (SSO20)
- 8 interrupt levels
- 2 \times 8-bit multifunction timer/counter
- Interval timer with watchdog
- Two-wire serial interface
- Voltage supervisor
- On-chip RC oscillator
- On-chip crystal oscillator

Benefits

- Contactless power supply and communication interface
- Power management for contactless- and battery-power supply
- Shift-register-supported modulator and demodulator stages
- Low power consumption
- Active mode $< 300 \mu\text{A}$ @ 2 V and 1 MHz system clock frequency (2 μs instruction cycle)
- Power-down mode $< 1 \mu\text{A}$
- Supply voltage 2.0 V to 6.5 V
- High-level language programming in qFORTH
- Operating speed: 1 – 10 μs instruction cycle (2 μs @ $V_{\text{DD}} = 2 \text{ V}$)

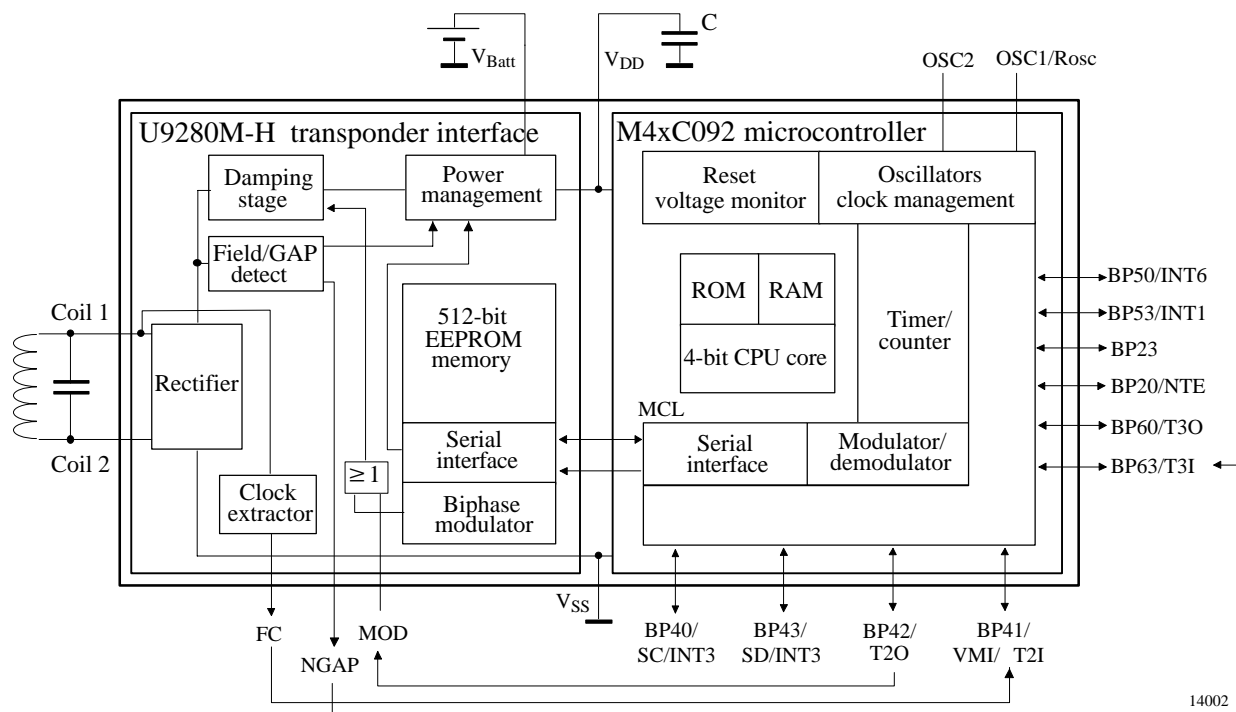


Figure 1. Block diagram

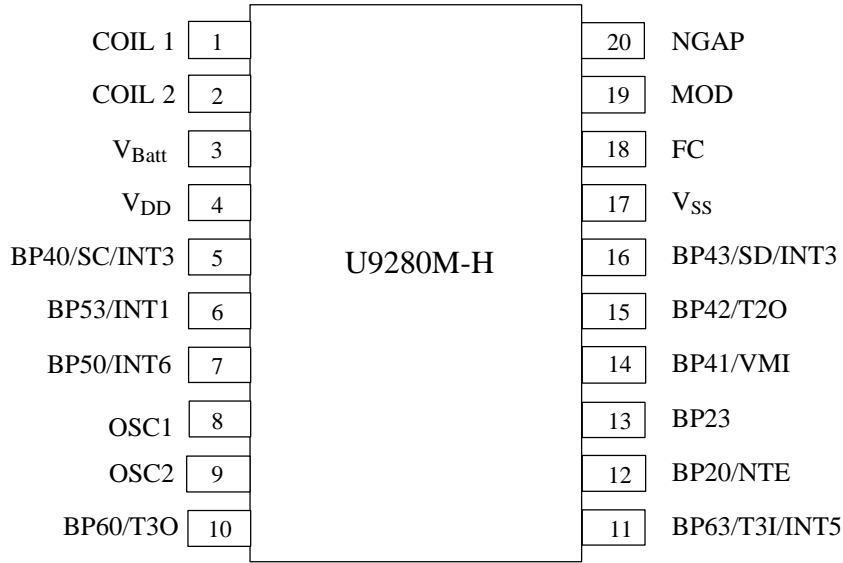


Figure 2. Pinning SSO20

Table 1. Pin Description (SSO20 Package)

Name	Pin	Function / Alternate Function
V _{SS}	17	Circuit ground
U _{Batt}	3	Power-supply voltage input to connect a battery
V _{DD}	4	Power-supply voltage for the μ C and EEPROM. At this pin a capacitor (0.5 to 10 μ F) must be connected to buffer the voltage during field supply and to block the V _{DD} of the μ C.
Coil1	1	Coil input 1. Pin to connect a LC antenna for communication and field supply
Coil2	2	Coil input 2 see above
NGAP	20	Gap detect output – front end. Must be connected to the demodulator input Pin T3I.
MOD	19	Modulation input – front end. Must be connected to the modulator output Pin T2O.
FC	18	Field clock output of the clock extractor
BP60/T3O	10	Bidirectional I/O-line / Timer 3 output/ modulator output
BP63/T3I/INT5	11	I/O-port line / INT5 interrupt input / Timer 3 input / demodulator input
BP50/INT6	7	I/O-port line / INT6 interrupt input (falling or rising edge sensitive)
BP53/INT3	6	I/O-port line / INT3 interrupt input (falling or rising edge sensitive)
BP40/SC/INT3	5	I/O-port line / serial clock line / INT3 input (falling edge sensitive)
BP41/VMI	14	I/O-port line / Voltage monitor input / Timer 2 input
BP42/T2O	15	I/O-port line / Timer 2 output / modulator output
BP43/SD/INT3	16	I/O-port line / serial data line / INT3 input (falling edge sensitive)
BP20/NTE	12	BP20-I/O-port line / test mode input. This input is used to control the test modes. During POR it must not be connected with a low impedance to V _{DD} .
BP23	13	I/O-port line
OSC1/Rosc	8	Oscillator- or external system-clock input / input for RC-oscillator resistor
OSC2	9	Oscillator output

Table of Contents

1	Functional Description	4
1.1	M44C092	4
1.2	The U3280M Transponder Interface	5
1.3	Modulation	5
1.4	Field Clock	5
1.5	Gap Detect	5
1.6	Wake-up Signal	5
1.7	U3280M Signals and Timing	6
1.8	Power Supply	6
1.8.1	Automatic Power Management	6
1.8.2	Controlling the Power Management via the Serial Interface	7
1.8.3	Buffer Capacitor CB	7
1.9	Serial Interface	7
1.9.1	Serial Protocol	7
1.10	EEPROM	8
1.10.1	EEPROM – Operating Modes	8
1.10.2	Write Operations	8
1.10.3	Read Operations	9
1.10.4	Initialization after a Reset Condition	10
1.10.5	Special Modes	10
1.11	Power-on Reset	11
2	Electrical Characteristics	12
2.1	Common Features U9280M-H	12
2.2	Absolute Maximum Ratings	12
2.3	Thermal Resistance	12
2.4	Common DC Characteristics	13
2.5	DC Characteristics – Microcontroller M44C092	13
2.6	AC Characteristics	14
2.7	DC Characteristics – Transponder Interface U3280M	16
2.8	AC Characteristics – Transponder Interface U3280M	17
3	Package Information	18
4	Ordering Information	18
4.1	Order Number	18

1 Functional Description

The U9280M-H multi-chip module contains a microcontroller and a transponder IC mounted in a single package. Everything necessary for remote control and wireless identification systems is integrated: inputs to connect keys, outputs to control an IR- or RF transmitter and to drive indicator LEDs, an EEPROM to store key code and identifiers, and an interface for contactless communication and power supply.

The U3280M is a transponder interface consisting of an analog front end for contactless data communication and power supply, and a serial 512-bit EEPROM. In addition, it includes power management to switch the battery or magnetic-field power supply. For modulation and demodulation of the magnetic field, the device has input and output pins to connect the microcontroller. The MOD, NGAP and FC Pins can be connected externally to the modulator, demodulator and timer I/O pins of the microcontroller. Access to the EEPROM is possible via a two-wire serial interface. The M44C092 microcontrollers are equipped with compatible two-wire serial interface to communicate with the U3280M. In the U9280M-H the serial interfaces of the transponder interface and the microcontroller are linked internally.

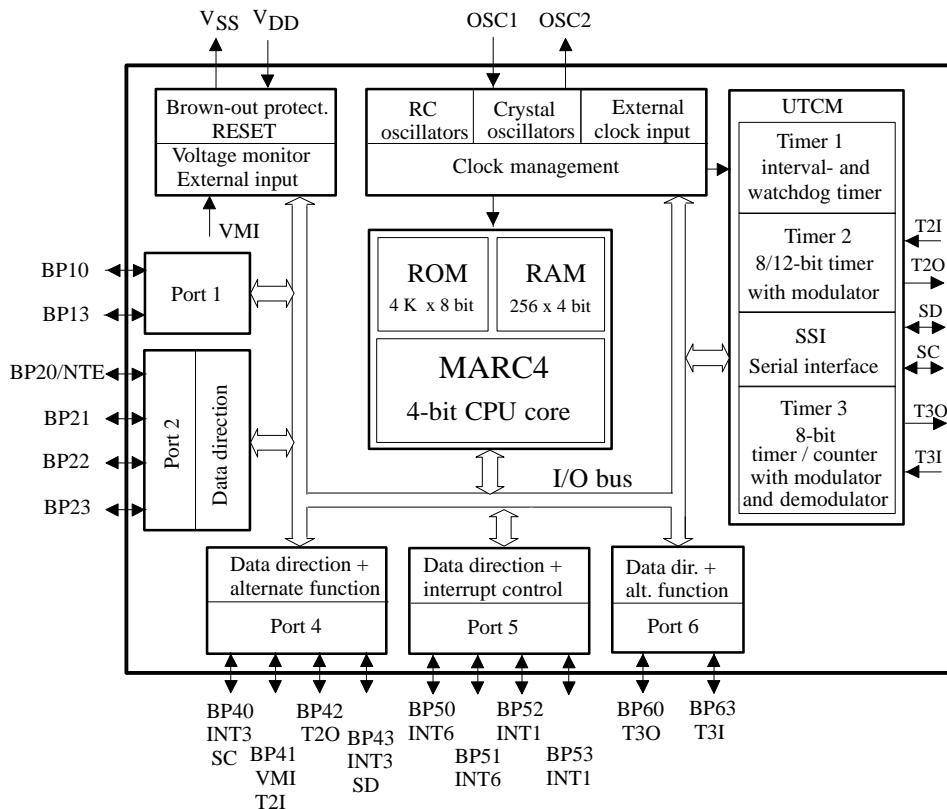
1.1 M44C092

The M44C092 microcontroller is a member of the TEMIC 4-bit single-chip microcontroller family. It is especially designed for remoted-control applications. It consists of an advanced stack-based 4-bit CPU core with 4 K ROM, 256 nibble of RAM and on-chip peripherals. The CPU is based on the HARVARD architecture and contains an interrupt controller with 8 prioritized interrupt levels.

The peripherals include parallel I/O ports, two 8-bit programmable multifunction timer/counters, a two-wire serial interface, an interval timer with watchdog function and a voltage supervisor. The serial interface supports, together with the timers, a modulator and demodulator stage for Manchester, Biphase and pulse-width modulation and demodulation. The integrated clock generator contains a RC-, a 32-kHz crystal, a 4-MHz crystal oscillator and a programmable input to use an external clock.

Note: In the U9280M-H not all I/O pins of the M44C092 are available (see 'Pin Description').

The microcontroller is fully described in the MARC4 M44C092 data sheet.



13361

Figure 3. Block diagram M44C092

1.2 The U3280M Transponder Interface

The transponder interface contains a rectifier stage to rectify the AC from the coil inputs and to supply itself and an additional microcontroller device with power from a LC-resonant circuit at the coil inputs. It is also possible to supply the device via the V_{Batt} -input with DC from a battery. The built-in power management switches automatically between battery supply (V_{Batt} pin) and coil supply. It switches to coil supply if a field is applied at the coil and switches back to battery if the field is removed.

The voltage from the coil or the V_{Batt} pin is output at the V_{DD} pin to supply the microcontroller device. At the V_{DD} pin a capacitor must be connected to smooth and buffer the supply voltage for the transponder interface and the microcontroller. This capacitor is also used to buffer the supply voltage during communication (damping and gaps in the field).

For communication, a damping-stage and a gap-detect circuitry is on the chip. By means of the damping stage the coil voltage can be modulated to transmit data via the field. It can be controlled with the modulator input (MOD pin) via the microcontroller. The gap detection circuitry detects gaps in the field and output the gap/field signal at the gap detect output (NGAP pin). It can be used to receive data via a modulated field and to check if a field is applied at the coil.

For the storage of data such as key codes, identifiers and configuration bits, a 512-bit EEPROM is available on the chip. It can be read and written by the microcontroller via an I²C-compatible two-wire serial interface. The serial interface, the EEPROM and the microcontroller are supplied with the voltage at the V_{DD} pin. That means the microcontroller can read and write the EEPROM if the supply voltage is in the operating range.

The U3280M contains additional operating modes to support a wide range of applications. These modes can be controlled via the serial interface. The power management can be switched off by software to disable the automatic switching between battery and field. This supports applications with battery supply only.

There is an on-chip Biphase and Manchester modulator. It can be selected and controlled via the serial interface with a special mode control byte. If this modulator is used the external connection to the modulator input is not necessary.

1.3 Modulation

The transponder interface can modulate the magnetic field by a modulator to transmit data to a base station. It modulates the coil voltage by varying the coil's load. The

modulator can be controlled via the MOD pin. A high level "1" increases the current into the coil inputs and damps the coil voltage. A low level "0" decreases the current and increases the coil voltage. The modulator generates a voltage stroke of about $2 V_{pp}$ at the coil. A high level at the MOD input makes the maximum of the field energy available at V_{DD} . During a reset a high level at the MOD input causes the optimum conditions for starting the device and charging the capacitor at V_{DD} after the field is applied at the coil.

Digital Input to Control the Damping Stage (MOD)

MOD=0: coil undamped

$$V_{COIL_peak} = V_{DD} \times \sqrt{2} + V_{CMS} = V_{CU}$$

MOD=1: coil damped

$$V_{COIL_peak} = V_{DD} \times \sqrt{2} = V_{CD}$$

$V_{CMS} = V_{CID}$: modulation voltage stroke @ coil inputs

Note: If the automatically power management is disabled the internal front end V_{DD} is limited at V_{DDC} . In this case the value V_{DDC} must be used in the formula above.

1.4 Field Clock

The field clock extractor of the interface makes the field clock available for the microcontroller. It can be used to supply timer inputs to synchronize modulation and demodulation with the field clock.

1.5 Gap Detect

The transponder interface can also receive data. The base station modulates the data with short gaps in the field. The gap-detection circuit detects these gaps in the magnetic field and outputs the gap/field signal at the NGAP pin. A high level indicates that a field is applied at the coil and a low level indicates a gap or that the field is off. The microcontroller must demodulate the incoming data stream at one of its inputs.

Digital Output of the Gap Detection Stage (NGAP)

NGAP=0: gap detected / no field

$$V_{COIL_peak} = V_{FDOFF}$$

NGAP=1: field detected

$$V_{COIL_peak} = V_{FDON}$$

Note: No amplifier is used in the gap detection stage. A digital Schmitt trigger evaluates the rectified and smoothed coil voltage.

1.6 Wake-up Signal

If a field is applied at the coil of the transponder interface the microcontroller can be woken up with the wake signal at the NGAP pin. For that purpose the NGAP pin must be

connected to an interrupt input of the microcontroller. A high level at the NGAP output indicates an applied field and can be used as wake signal for the microcontroller via an interrupt. If no battery voltage is available at V_{Batt} the controller starts with a power-on-reset after the voltage of the buffer capacitor at V_{DD} is loaded by the field above the power-on-reset level.

The wake signal is generated if the power management switches to field supply. The field detection stage of the power management has low-pass characteristics to avoid the generation of wake signals and unnecessary switching between battery and field supply in case of interferences at the coil inputs.

1.7 U3280M Signals and Timing

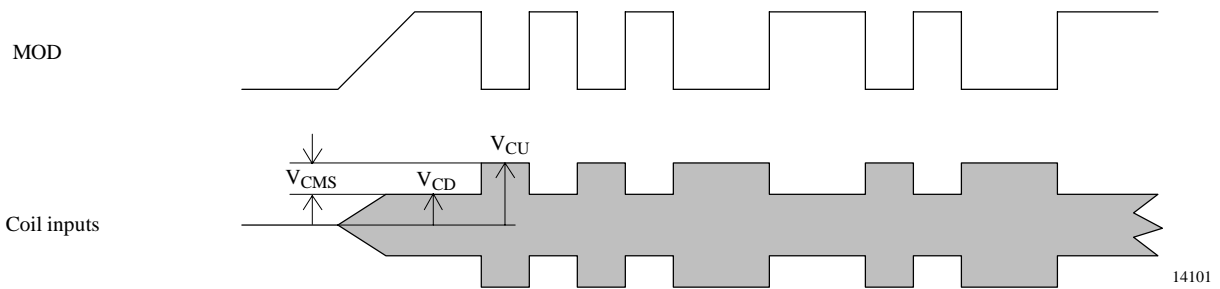


Figure 4. Modulation

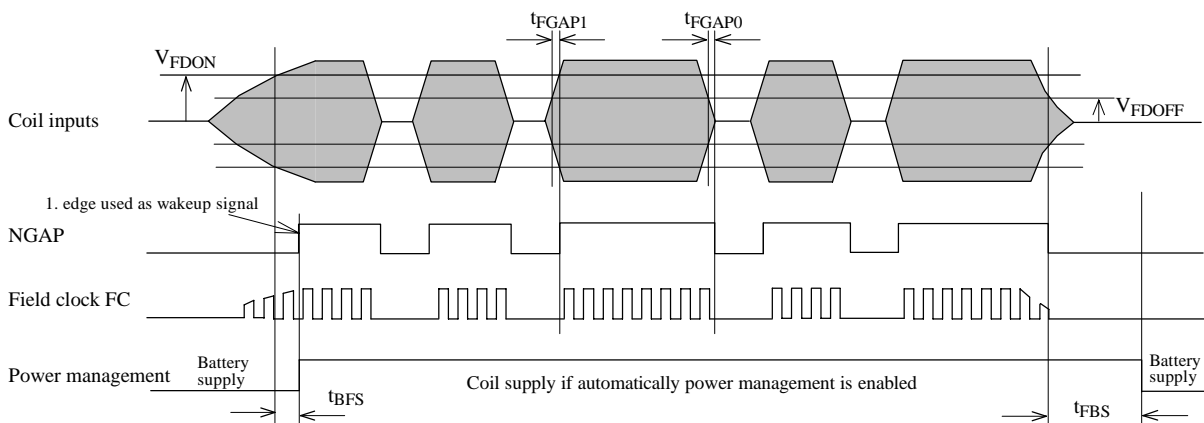


Figure 5. Gap detection and battery to field switching

1.8 Power Supply

The U3280 has a power management that handles two power-supply sources. Normally, the IC is supplied by a battery at the V_{Batt} pin. If a magnetic field is applied at the LC-resonant circuit of the device the field detection circuit switches from V_{Batt} to field supply. During field supply the V_{DD} voltage is limited at 3 V.

The V_{DD} pin is used to connect a capacitor to smooth the voltage from the rectifier and to buffer the power when

the field is modulated by gaps and damping. The EEPROM and the microcontroller always operate with the voltage at the V_{DD} pin.

1.8.1 Automatical Power Management

There are different conditions to switch from the battery to field and vice versa.

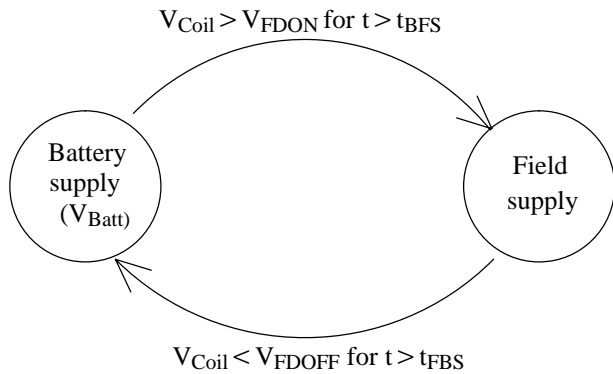


Figure 6. Switch conditions for the power management

The power management switches automatically from battery to field if the rectified voltage (V_{coil}) from the coil inputs becomes higher than field-on-detection voltage (V_{FDON}) even if no battery voltage is available ($0 < V_{Batt} < 1.8\text{ V}$). It switches back to battery if the coil voltage becomes lower than the field-off-detection voltage (V_{FDOFF}).

The field-detection stage of the power management has low-pass characteristics to suppress noise. An applied field needs a time delay t_{BFS} (battery-to-field switch delay) to change the power supply. If the field is removed from the coil the power management will generate a reset for the microcontroller.

1.8.2 Controlling the Power Management via the Serial Interface

The automatic mode of the power management can be switched off and on by a command from the microcontroller. If the automatic mode is switched off the IC is always supplied by the battery up to the next power-on reset or to a switch-on command. The power management-on and -off command must be transferred via the serial interface.

If the power management is switched off and the device is supplied from the battery it can communicate via the field without load the field. This mode can be used to realize applications with battery supply if the available field is too weak to supply the IC with power.

1.8.3 Buffer Capacitor CB

The buffer capacitor connected at V_{DD} is used to buffer the supply voltage for the microcontroller and the EEPROM during field supply. It smooths the rectified AC from the coil and buffers the supply voltage during modulation and gaps in the field. The size of this capacitor depends on the application. It must be of a dimension so that during modulation and gaps the ripple on the supply

voltage is in the range of 100 – 300 mV. During gaps and damping the capacitor is used to supply the device, that means the size of the capacitor depends on the length of the gaps and damping cycles.

Example:

For a supply current 350 μA , 200 mV ripple @ V_{DD}

No Field Supply During	Necessary CB
250 μs	470 nF
500 μs	1000 nF

1.9 Serial Interface

The transponder interface has an I²C-like serial interface to the microcontroller for read and write accesses to the EEPROM. In a special mode the serial interface can also be used to control the Biphase/Manchester modulator or the power management of the U3280M.

The serial interface of the U3280M device must be controlled by a master device (normally the M4xC09x microcontroller) which generates the serial clock and controls the access via the SCL- and SDA-line. SCL is used to clock the data in and out of the device. SDA is a bidirectional line used to transfer data into and out of the device. The following protocol is used for the data transfers.

1.9.1 Serial Protocol

- Data states on the SDA line changing only while SCL is low.
- Changes in the SDA line while SCL is high will be interpreted as START or STOP condition.
- A START condition is defined as high-to-low transition on the SDA-line while the SCL-line is high.
- A STOP condition is defined as low-to-high transition on the SDA-line while the SCL-line is high.
- Each data transfer must be initialized with a START condition and terminated with a STOP condition. The START condition wakes the device from standby mode and the STOP condition returns the device to stand-by mode.
- A receiving device generates an acknowledge (A) after the reception of each byte. For that the master device must generate an extra clock pulse. If the reception was successful the receiving master or slave device pulls down the SDA-line during that clock cycle. If in transmit mode an acknowledge is not detected (N) by the interface, it will terminate further data transmissions and will go into receive mode. A master device must finish its read operation by a not acknowledge and then issue a stop condition to place the device into a known state.

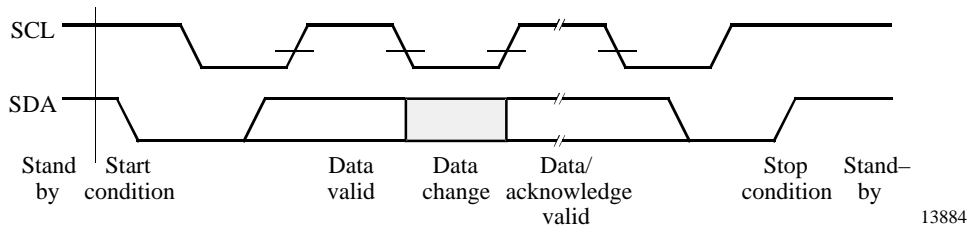


Figure 7. Serial protocol

13884

Control Byte Format

	EEPROM address					Mode control bits		Read/NWrite	
Start	A4	A3	A2	A1	A0	C1	C0	R/NW	Ackn

The control byte follows the start condition and consists of the 5-bit row address, 2 mode control bits and the read/not write-bit.

Data Transfer Sequence

Start	Control byte	Ackn	Data byte	Ackn	Data byte	Ackn	Stop
-------	--------------	------	-----------	------	-----------	------	------

- Before the START condition and after the STOP condition the device is in standby mode and the SDA-line is switched as input with pull-up resistor.
- The START condition follows a control byte that determines the following operation. Bit 0 of the control byte is used to control the following transfer direction. A "0" defines a write access and a "1" a read access.

1.10 EEPROM

The EEPROM has a size of 512 bits and is organized as a 32 x 16-bit matrix. To read and write data to and from the EEPROM the serial interface must be used. The interface supports one and two byte write accesses and one to n-byte read accesses to the EEPROM.

1.10.1 EEPROM – Operating Modes

The operating modes of the EEPROM are defined via the control byte. The control byte contains the row address, the mode control bits and the read/not-write bit that is used to control the direction of the following transfer. A "0" defines a write access and a "1" a read access. The five address bits select one of the 32 rows of the EEPROM memory to be accessed. For all accesses the complete 16-bit word of the selected row is loaded into a buffer. The buffer must be read or overwritten via the serial interface. The two mode control bits C1 and C2 define in which order the accesses to the buffer are performed: High byte – low byte or low byte – high byte. The EEPROM also supports autoincrement and autodecrement read operations. After sending the start address with the corresponding mode, consecutive memory cells can be read row by row without transmission of the row addresses.

Two special control bytes enable the complete initialization of EEPROM with "0" or with "1".

1.10.2 Write Operations

The EEPROM permits 8-bit and 16-bit write operations. A write access starts with the START condition followed by a write control byte and one or two data bytes from the master. It is completed via the STOP condition from the master after the acknowledge cycle.

If the EEPROM receives the control byte, it loads the content of the addressed memory cell into a 16-bit read/write buffer. After the first data byte has been received the EEPROM starts the internal programming cycle. It consists of an erase cycle (write "zeros") and the write cycle (write "ones"). Each cycle takes about 10 ms. The write cycle is started after the stop condition and the complete buffer is stored back automatically to the EEPROM. That means for two-byte write operations, the second byte must be transferred within the erase cycle otherwise only the first byte will be stored in the EEPROM and the second byte will be ignored.

Acknowledge Polling

If the EEPROM is busy with an internal write cycle, all inputs are disabled and the EEPROM will not acknowledge until the write cycle is finished. This can be used to detect the end of the write cycle. The master must perform acknowledge polling by sending a start condition followed by the control byte. If the device is still busy with the write cycle, it will not return an acknowledge and the master has to generate a stop condition or perform further acknowledge polling sequences. If the cycle is complete, it returns an acknowledge and the master can proceed with the next read or write cycle.

Write One Data Byte

Start	Control byte	A	Data byte 1	A	Stop
-------	--------------	---	-------------	---	------

Write Two Data Bytes

Start	Control byte	A	Data byte 1	A	Data byte 2	A	Stop
-------	--------------	---	-------------	---	-------------	---	------

Write Control Byte Only

Start	Control byte	A	Stop
-------	--------------	---	------

A → acknowledge

Write Control Bytes

Write low byte first

MSB					LSB		
A4	A3	A2	A1	A0	C1	C0	R/NW
Row address					0	1	0

Byte order

LB(R)	HB(R)
-------	-------

Write high byte first

MSB					LSB		
A4	A3	A2	A1	A0	C1	C0	R/NW
Row address					1	0	0

Byte order

HB(R)	LB(R)
-------	-------

HB: high byte; LB: low byte; R: row address

1.10.3 Read Operations

The EEPROM allows byte-, word- and current address read operations. The read operations are initiated in the same way as write operations. Every read access is initiated by sending the START condition followed by the control byte which contains the address and the read mode. After the device receives a read command it returns an acknowledge, loads the addressed word into the read/write buffer and sends the selected data byte to the master. The master has to acknowledge the received byte

if it wants to proceed the read operation. If two bytes are read out from the buffer the device increments respectively decrements the word address automatically and loads the buffer with the next word. The read mode bits determines if the low or high byte is read first from the buffer and if the word address is incremented or decremented for the next read access. If the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The master can terminate the read operation after every byte by not responding with an acknowledge (N) and by issuing a stop condition.

Read One Data Byte

Start	Control byte	A	Data byte 1	N	Stop
-------	--------------	---	-------------	---	------

Read Two Data Bytes

Start	Control byte	A	Data byte 1	A	Data byte 2	N	Stop
-------	--------------	---	-------------	---	-------------	---	------

Read n Data Bytes

Start	Control byte	A	Data byte 1	A	Data byte 2	A	-----	Data byte n	N	Stop
-------	--------------	---	-------------	---	-------------	---	-------	-------------	---	------

A -> acknowledge, N -> no acknowledge

Read Control Bytes

Read low byte first, address increment	MSB					LSB		
	A4	A3	A2	A1	A0	C1	C0	R/NW
	Row address					0	1	1

Byte order	LB(R)	HB(R)	LB(R+1)	HB(R+1)	---	LB(R+n)	HB(R+n)
------------	-------	-------	---------	---------	-----	---------	---------

Read high byte first, addr. decrement	MSB					LSB		
	A4	A3	A2	A1	A0	C1	C0	R/NW
	Row address					1	0	1

Byte order	HB(R)	LB(R)	HB(R-1)	LB(R-1)	---	HB(R-n)	LB(R-n)
------------	-------	-------	---------	---------	-----	---------	---------

HB: high byte; LB: low byte, R: row address

1.10.4 Initialization after a Reset Condition

The EEPROM with the serial interface has its own reset circuitry. In systems with microcontrollers that have their own reset circuitry for power on reset, watchdog reset or brown-out reset, it may be necessary to bring the U505M into a known state independent of its internal reset. This is performed by reading one byte without acknowledging and then generating a stop condition.

1.10.5 Special Modes

With special control bytes the serial interface can be used to control the modulator stage or the power management. The EEPROM access and the serial interface are disabled in these modes until the next STOP condition. If no START or STOP condition is generated the SCL and SDA line can be used for the modulator stage. SCL is used for the modulator clock and SDA is used for the data. In that mode the same conditions for clock and data changing as normal are valid. The SCL and SDA line can be used for continuous bit transfers, an acknowledge cycle after 8 bits must not be generated.

Table 2. Special modes

Control Byte	Description
1100x111b	Biphase modulation
1101x111b	Manchester modulation (not yet available !!!!)
11xx0111b	Switch power management off -> disables switching from battery to field supply
11xx1111b	Switch power management on -> enables automatically switching between battery and field supply
xxxxx110b	Reserved

Data Transfer Sequence for Biphase and Manchester Modulation:

Start	Control byte	Ackn	Bit 1	Bit 2	Bit 3	Bit n	Stop
-------	--------------	------	-------	-------	-------	-------	-------	------

Note: After a reset of the microcontroller it is not known whether the transponder interface has been a reset too. It could be still in a receive or transmit cycle. To place the serial interface of the device into a known state, the microcontroller should read one byte from the device without acknowledge and generate a stop condition.

1.11 Power-on Reset

The analog front end starts working with the applied field. The EEPROM with the serial interface has its own reset circuitry. (The reset level of the front end is below the reset level of the M44C092)

The microcontroller has a power-on reset circuitry with a brown-out detection. One of two reset voltage levels [1.8 V / 2.0 V] can be selected via the software (see

M44C092 data sheet). If a fast instruction cycle ($< 2 \mu\text{s}$) is used the higher reset level should be selected.

After a watchdog or brown-out detection reset, the serial interface and the EEPROM should be reset by reading one byte from the transponder interface device without acknowledging and generation of a STOP condition. That places the serial interface and EEPROM into a known state.

2 Electrical Characteristics

2.1 Common Features U9280M-H

- Operating temperature range: -40°C to $+85^{\circ}\text{C}$
- Operating voltage range (V_{Batt}): 2.0 V to 6.5 V
- Low power consumption:
 - 600 μA @ 6.5 V in operating mode (with 2 μs instruction cycle)
 - 200 μA @ 2.0 V in operating mode (with 2 μs instruction cycle)
 - 1 μA @ 2.0 V in stop mode
- Power supply : Contactless (coil 125 kHz) and battery supply

2.2 Absolute Maximum Ratings

Voltages are given relative to V_{SS} .

Parameters	Symbol	Value	Unit
Supply voltage	$V_{\text{Batt}}, V_{\text{DD}}$	0 to +7.0 with reverse protection	V
Max. current out of V_{SS} -pin		15	mA
Max. current into V_{Batt} -pin		15	mA
Input voltage (on any pin)	V_{IN}	$V_{\text{SS}}-0.6 < V_{\text{IN}} < V_{\text{DD}}+0.6$	V
Input/output clamp current ($V_{\text{SS}} > V_i/V_o > V_{\text{DD}}$)	$I_{\text{IK}} / I_{\text{OK}}$	+/- 15	mA
Min. ESD protection (100 pF through 1.5 k Ω)		+/-2	kV
Min. ESD protection Coil 1 and Coil 2 inputs (100 pF through 1.5 k Ω)		+/-1	kV
Operating temperature range	T_{amb}	- 40 to + 85	$^{\circ}\text{C}$
Storage temperature range	T_{stg}	- 40 to + 125	$^{\circ}\text{C}$
Soldering temperature ($t \leq 10$ sec)	T_{sd}	260	$^{\circ}\text{C}$

Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any condition above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating condition for an extended period may affect device reliability. All inputs

and outputs are protected against high electrostatic voltages or electric fields. However, precautions to minimize the build-up of electrostatic charges during handling are recommended. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g. V_{DD}).

2.3 Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SSO20	R_{thJA}	140	K/W

2.4 Common DC Characteristics

$V_{SS} = 0\text{ V}$, $T_{amb} = -40\text{ to }85^{\circ}\text{C}$ unless otherwise specified.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Power supply						
Operating voltage at V_{Batt}		V_{Batt}	2.0		6.5	V
Operating voltage at V_{DD}		V_{DD}	V_{POR}		6.5	V
Active current CPU active	$f_{SYSCL} = 1\text{ MHz}$ $V_{DD} = 2.0\text{ V}$ $V_{DD} = 3.0\text{ V}$ $V_{DD} = 6.5\text{ V}$	I_{DD}		200 300 600	250 800	μA μA μA
Power down current (CPU sleep, RC oscillator active, 4-MHz quartz-osc. active)	$f_{SYSCL} = 1\text{ MHz}$ $V_{DD} = 2.0\text{ V}$ $V_{DD} = 3.0\text{ V}$ $V_{DD} = 6.5\text{ V}$	I_{PD}		40 100 250	70 400	μA μA μA
Sleep current (CPU sleep, 32-kHz quartz-osc. inactive 4-MHz quartz-osc. inactive)	$V_{DD} = 6.5\text{ V}$	I_{Sleep}		1.0	2.0	μA
Reset current	$V_{DD} < V_{POR}$	I_{Reset}		150		μA

2.5 DC Characteristics – Microcontroller M44C092

$V_{SS} = 0\text{ V}$, $T_{amb} = -40\text{ to }85^{\circ}\text{C}$ unless otherwise specified.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Brown-out protection reset threshold voltage						
Reset threshold voltage	$BOT = 1$	V_{POR}	155	1.7	1.85	V
Reset threshold voltage	$BOT = 0$	V_{POR}	1.85	2.0	2.2	V
Reset hysteresis		V_{POR}		50		mV
Voltage monitor threshold voltage						
VM high threshold voltage	$V_{DD} > VM$, $VMS = 1$	V_{MThh}		3.0	3.25	V
VM high threshold voltage	$V_{DD} < VM$, $VMS = 0$	V_{MThh}	2.8	3.0		V
VM middle thresh. voltage	$V_{DD} > VM$, $VMS = 1$	V_{MThm}		2.6	2.8	V
VM middle thresh. voltage	$V_{DD} < VM$, $VMS = 0$	V_{MThm}	2.4	2.6		V
VM low threshold voltage	$V_{DD} > VM$, $VMS = 1$	V_{MThl}		2.2	2.4	V
VM low threshold voltage	$V_{DD} < VM$, $VMS = 0$	V_{MThl}	2.0	2.2		V
External input voltage						
VMI rising edge threshold	$VMS = 1$, $V_{DD} = 3\text{ V}$	V_{VMI}		1.3	1.4	V
VMI falling edge threshold	$VMS = 0$, $V_{DD} = 3\text{ V}$	V_{VMI}	1.2	1.3		V

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit	
All Bidirectional Ports							
Input voltage LOW	$V_{DD} = 1.8$ to 6.5 V	V_{IL}	V_{SS}		$0.2 \cdot V_{DD}$	V	
Input voltage HIGH	$V_{DD} = 1.8$ to 6.5 V	V_{IH}	$0.8 \cdot V_{DD}$		V_{DD}	V	
Input LOW current (pull-up)	$V_{DD} = 2.0$ V,	I_{IL}	-2.0	-4.0	-12	μ A	
	$V_{DD} = 3.0$ V, $V_{IL} = V_{SS}$			-20			
	$V_{DD} = 6.5$ V		-50	-100	-200		
Input HIGH current (pull-down)	$V_{DD} = 2.0$ V,	I_{IH}	2.0	4.0	12	μ A	
	$V_{DD} = 3.0$ V, $V_{IH} = V_{DD}$			20			
	$V_{DD} = 6.5$ V		50	100	200		
Input LOW current (strong pull-up)	$V_{DD} = 2.0$ V, $V_{IL} = V_{SS}$	I_{IL}	-20	-50	-100	μ A	
	$V_{DD} = 6.5$ V		-300	-600	-1200		
Input LOW current (strong pull-down)	$V_{DD} = 2.0$ V, $V_{IH} = V_{DD}$	I_{IH}	20	50	100	μ A	
	$V_{DD} = 6.5$ V		300	600	1200		
Input leakage current	$V_{IL} = V_{SS}$	I_{IL}			100	nA	
Input leakage current	$V_{IH} = V_{DD}$	I_{IH}			100	nA	
Output LOW current	$V_{OL} = 0.2 \cdot V_{DD}$ $V_{DD} = 2.0$ V $V_{DD} = 3.0$ V, $V_{DD} = 6.5$ V	I_{OL}	0.6	1.2	2.5	mA	
					5		
			8	15	22		
Output HIGH current	$V_{OH} = 0.8 \cdot V_{DD}$ $V_{DD} = 2.0$ V $V_{DD} = 3.0$ V, $V_{DD} = 6.5$ V	I_{OH}	-0.6	-1.2	-2.5	mA	
					-5		
			-8	-16	-24		

Note: The Pin BP20/NTE has a strong pull-up resistor during the reset-phase of the microcontroller

2.6 AC Characteristics

Operation Cycle Time

$V_{SS} = 0$ V

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
System clock cycle	$V_{DD} = 1.8$ to 6.5 V $T_{amb} = -40$ to 85° C	t_{SYSCL}	500		2000	ns
	$V_{DD} = 2.4$ to 6.5 V $T_{amb} = -40$ to 85° C	t_{SYSCL}	250		2000	ns

Supply voltage $V_{DD} = 1.8$ to 6.5 V, $V_{SS} = 0$ V, $T_{amb} = -40$ to 85° C unless otherwise specified.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Timer 2 input timing Pin T2I						
Timer 2 input clock		f_{T2I}			5	MHz
Timer 2 input LOW time		t_{T2IL}	100			ns
Timer 2 input HIGH time		t_{T2IH}	100			ns
Timer 3 input timing Pin T3I						
Timer 3 input clock		f_{T3I}			$SYSCL/2$	
Timer 3 input LOW time		t_{T3IL}	$2 \times t_{SYSCL}$			ns
Timer 3 input HIGH time		t_{T3IH}	$2 \times t_{SYSCL}$			ns

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Interrupt request input timing						
Int. request LOW time		t _{IRL}	100			ns
Int. request HIGH time		t _{IRH}	100			ns
External system clock						
EXSCL at OSC1	ECM = EN Rise / fall time < 10 ns	f _{EXSCL}	0.5		4	MHz
EXSCL at OSC1	ECM = DI Rise / fall time < 10 ns	f _{EXSCL}	0.02		4	MHz
Input HIGH time	Rise / fall time < 10 ns	t _{IH}	0.1			μs
Reset timing						
Power-on reset time	V _{DD} > V _{POR}	t _{POR}		1.5	5	ms
RC oscillator 1						
Frequency		f _{RcOut1}		3.8		MHz
Stability	V _{DD} = 2.0 to 6.5 V	Δf/f			± 50	%
Temperature coefficient		Δf/f/°C		0.15		%
RC oscillator 2 – external resistor						
Frequency	R _{ext} = 170 kΩ R _{ext} = 720 kΩ	f _{RcOut2} f _{RcOut2}		4 1		MHz
Stability	V _{DD} = 2.0 to 6.5 V	Δf/f			± 15	%
Stabilization time		t _S			10	μs
4-MHz crystal oscillator (operating range 2.2 V to 6.5 V)						
Frequency		f _X		4		MHz
Start-up time		t _{SQ}		5		ms
Stability		Δf/f	-10		10	ppm
Integrated input / output capacitances (mask programmable)	C _{IN} / C _{OUT} programmable in steps of 2 pF	C _{IN}	0		20	pF
		C _{OUT}	0		20	pF
32-kHz crystal oscillator (operating range 2.0 V to 6.5 V)						
Frequency		f _X		32.768		kHz
Start-up time		t _{SQ}		0.5		s
Stability		Δf/f	-10		10	ppm
Integrated input / output capacitances (mask programmable)	C _{IN} / C _{OUT} programmable in steps of 2 pF	C _{IN}	0		20	pF
		C _{OUT}	0		20	pF
External 32-kHz crystal parameters						
Crystal frequency		f _X		32.768		kHz
Serial resistance		R _S		30	50	kΩ
Static capacitance		C ₀		1.5		pF
Dynamic capacitance		C ₁		3		fF

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
External 4 MHz crystal parameters						
Crystal frequency		f_X		4.0		MHz
Serial resistance		RS		40	150	Ω
Static capacitance		C0		1.4	3	pF
Dynamic capacitance		C1		3		fF

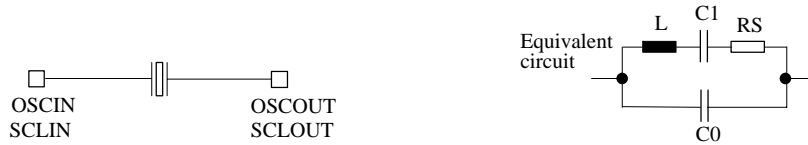


Figure 8. Crystal equivalent circuit

2.7 DC Characteristics – Transponder Interface U3280M

Supply voltage $V_{DD} = 1.8$ to 6.3 V, $V_{SS} = 0$ V, $T_{amb} = -40$ to 85°C unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Power supply						
Operating voltage at V_{Batt}		V_{Batt}	2.0		6.5	V
Operating voltage at V_{DD} during battery supply		V_{DDB}		$V_{Batt} - V_{SD}$		V
V_{DD} -limiter voltage during coil supply		V_{DDC}	2.4	2.9	3.2	V
Power management						
Field on detection voltage	$V_{DD} > 1.8$ V	V_{FDon}	2.2	2.5	2.9	V
Field off detection voltage	$V_{DD} > 1.8$ V	V_{FDOff}		0.8		V
Voltage drop at power-supply switch	$I_S = 1$ mA, $V_{Batt} = 2$ V	V_{SD}			300	mV
Coil input Coil 1, Coil 2						
Coil input current		I_{CI}			20	mA
Coil voltage stroke during modulation	$V_{CU} > 5$ V	V_{CMS}	1.8		4.0	V
Input capacitance		C_{IN}		30		pF
MOD pin						
Input LOW Voltage		V_{IL}	V_{SS}		$0.2 \times V_{DD}$	V
Input HIGH Voltage		V_{IH}	$0.8 \times V_{DD}$		V_{DD}	V
Input leakage current		I_{Ileak}		10		nA
NGAP/ FC pin						
Output LOW current	$V_{DD} = 2.0$ V $V_{OL} = 0.2 \times V_{DD}$	I_{OL}	0.08	0.2	0.3	mA
Output HIGH current	$V_{DD} = 2.0$ V $V_{OH} = 0.8 \times V_{DD}$	I_{OH}	-0.06	-0.15	-0.25	mA
EEPROM						
Operating current during erase/write cycle	$V_{DD} = 2$ V	I_{WR}			450	μA

2.8 AC Characteristics – Transponder Interface U3280M

Supply voltage $V_{DD} = 1.8$ to 6.5 V, $V_{SS} = 0$ V, $T_{amb} = -40$ to 85° C unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Serial interface timing (internal)						
SCL clock frequency (int.)		f_{SC}			500	kHz
Serial timing (if SCL and SDA available extern)						
SCL clock frequency (ext.)		f_{SCL}	0		100	kHz
Clock low time		t_{LOW}	4.7			μ s
Clock high time		t_{HIGH}	4.0			μ s
SDA and SCL rise time		t_R			1000	ns
SDA and SCL fall time		t_F			300	ns
Start condition setup time		t_{SUSTA}	4.7			μ s
Start condition hold time		t_{HDSTA}	4.0			μ s
Data input setup time		t_{SUDAT}	250			ns
Data input hold time		t_{HDDAT}	0			ns
Stop condition setup time		t_{SUSTO}	4.7			μ s
Bus free time		t_{BUF}	4.7			μ s
Input filter time		t_I			100	ns
Data output hold time		t_{DH}	300		1000	ns

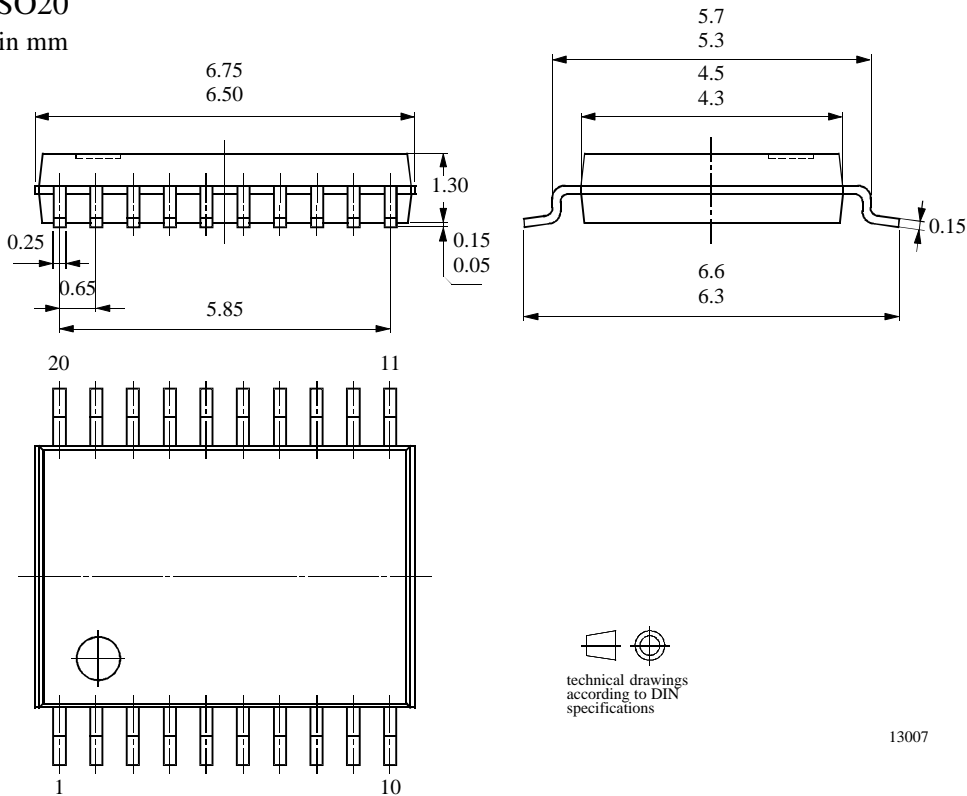
Supply voltage $V_{DD} = 1.8$ to 6.5 V, $V_{SS} = 0$ V, $T_{amb} = 25^{\circ}$ C unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Coil inputs						
Coil frequency		f_{COIL}		125		kHz
Gap detection						
Delay field off to gap = 0	$V_{CoilGap} < 0.7 V_{DC}$	t_{FGAP0}	10		50	μ s
Delay field on to gap = 1	$V_{CoilField} > 3 V_{DC}$	t_{FGAP1}	1		10	μ s
Power management						
Battery to field switch delay		t_{BFS}	160		650	μ s
Field to battery switch delay		t_{FBS}		10	60	ms
EEPROM						
Endurance	Erase/write-cycles	ED	500,000	1,000,000		E/W-cycles
Data erase/write cycle time	for 16 bits access	t_{DEW}		9	12	ms
Data erase time		t_{DE}	2		$1/2 \times t_{DEW}$	ms
Data retention time	$T_{amb} = 25^{\circ}$ C	t_{DR}	10			years
Power-up to read operation		t_{PUR}			0.2	ms
Power-up to write operation		t_{PUW}			0.2	ms

3 Package Information

Package SSO20

Dimensions in mm



4 Ordering Information

4.1 Order Number

Extended Type Number	Package	Remarks
U9280M-H-xxxz-FSG3	SSO20	> 200 kpcs p.a. taped and reeled

Remarks:

Customer ROM mask (10,000 US\$)

- to be defined by the customer
- lead time: 18 weeks after ROM mask programming and order received

Flash Version

As flash version of the U9280M-H the MARC4 M48C892 is used (available from stock).

Please select the option setting from the list below and insert ROM CRC.

Port 1

- BP10 CMOS Pull-up
 Open drain [N] Pull-down
 Open drain [P] Pull-up strong
 Pull-down strong
- BP13 CMOS Pull-up
 Open drain [N] Pull-down
 Open drain [P] Pull-up strong
 Pull-down strong

Port 2

- BP20 CMOS Pull-up
 Open drain [N] Pull-down
 Open drain [P] Pull-up strong
- BP21 CMOS Pull-up
 Open drain [N] Pull-down
 Open drain [P] Pull-up strong
 Pull-down strong
- BP22 CMOS Pull-up
 Open drain [N] Pull-down
 Open drain [P] Pull-up strong
 Pull-down strong
- BP23 CMOS Pull-up
 Open drain [N] Pull-down
 Open drain [P] Pull-up strong
 Pull-down strong

Port 4

- BP40 CMOS Pull-up
 Open drain [N] Pull-down
 Open drain [P] Pull-up strong
 Pull-down strong
- BP41 CMOS Pull-up
 Open drain [N] Pull-down
 Open drain [P] Pull-up strong
 Pull-down strong
- BP42 CMOS Pull-up
 Open drain [N] Pull-down
 Open drain [P] Pull-up strong
 Pull-down strong
- BP43 CMOS Pull-up
 Open drain [N] Pull-down

- Open drain [P] Pull-up strong
 Pull-down strong

Port 5

- BP50 CMOS Pull-up
 Open drain [N] Pull-down
 Open drain [P] Pull-up strong
 Pull-down strong
- BP51 CMOS Pull-up
 Open drain [N] Pull-down
 Open drain [P] Pull-up strong
 Pull-down strong
- BP52 CMOS Pull-up
 Open drain [N] Pull-down
 Open drain [P] Pull-up strong
 Pull-down strong
- BP53 CMOS Pull-up
 Open drain [N] Pull-down
 Open drain [P] Pull-up strong
 Pull-down strong

Port 6

- BP60 CMOS Pull-up
 Open drain [N] Pull-down
 Open drain [P] Pull-up strong
 Pull-down strong
- BP63 CMOS Pull-up
 Open drain [N] Pull-down
 Open drain [P] Pull-up strong
 Pull-down strong

OSC1

- No integrated capacitance
 Internal capacitance (___ pF)

OSC2

- No integrated capacitance
 Internal capacitance (___ pF)

ECM (Ext. clock monitor)

- Enable
 Disable

File: _____ . HEX

CRC: _____ HEX

Approval Date: ____-____-____ Signature: _____

Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design and may do so without further notice.

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use TEMIC Semiconductors products for any unintended or unauthorized application, the buyer shall indemnify TEMIC Semiconductors against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

Data sheets can also be retrieved from the Internet: <http://www.temic-semi.com>

TEMIC Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2594, Fax number: 49 (0)7131 67 2423