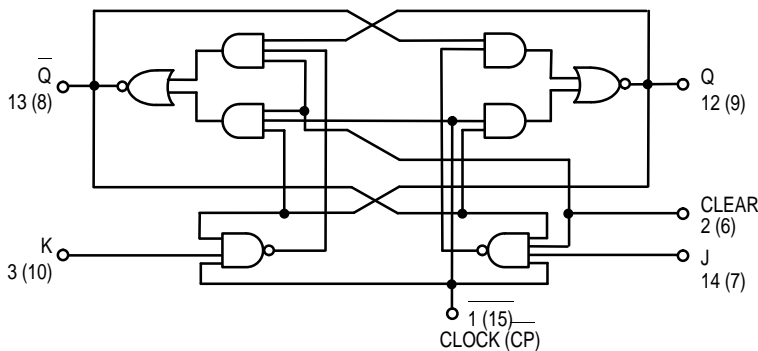




# DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

The SN54LS/74LS73A offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

**LOGIC DIAGRAM (Each Flip-Flop)**



**MODE SELECT — TRUTH TABLE**

OPERATING MODE	INPUTS			OUTPUTS	
	C <sub>D</sub>	J	K	Q	Q̄
Reset (Clear)	L	X	X	<u>L</u>	H
Toggle	H	h	h	q	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	<u>L</u>
Hold	H	l	l	q	q

H, h = HIGH Voltage Level

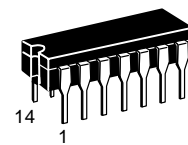
L, l = LOW Voltage Level

X = Don't Care

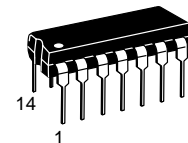
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

## SN54/74LS73A

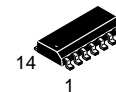
**DUAL JK NEGATIVE  
EDGE-TRIGGERED FLIP-FLOP**  
**LOW POWER SCHOTTKY**



**J SUFFIX**  
CERAMIC  
CASE 632-08



**N SUFFIX**  
PLASTIC  
CASE 646-06

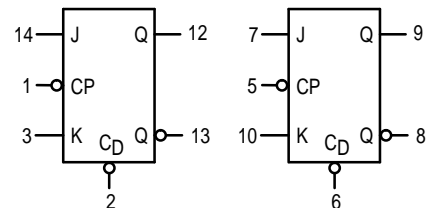


**D SUFFIX**  
SOIC  
CASE 751A-02

**ORDERING INFORMATION**

SN54LSXXJ Ceramic  
SN74LSXXN Plastic  
SN74LSXXD SOIC

**LOGIC SYMBOL**



V<sub>CC</sub> = PIN 4  
GND = PIN 11

# SN54/74LS73A

## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I <sub>OH</sub>	Output Current — High	54, 74			-0.4	mA
I <sub>OL</sub>	Output Current — Low	54 74			4.0 8.0	mA

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage	54	2.5	3.5	V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table	
		74	2.7	3.5	V		
V <sub>OL</sub>	Output LOW Voltage	54, 74		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA I <sub>OL</sub> = 8.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
		74		0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current	J, K Clear Clock			20 60 80	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
		J, K Clear Clock			0.1 0.3 0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current	J, K Clear, Clock			-0.4 -0.8	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)		-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current				6.0	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

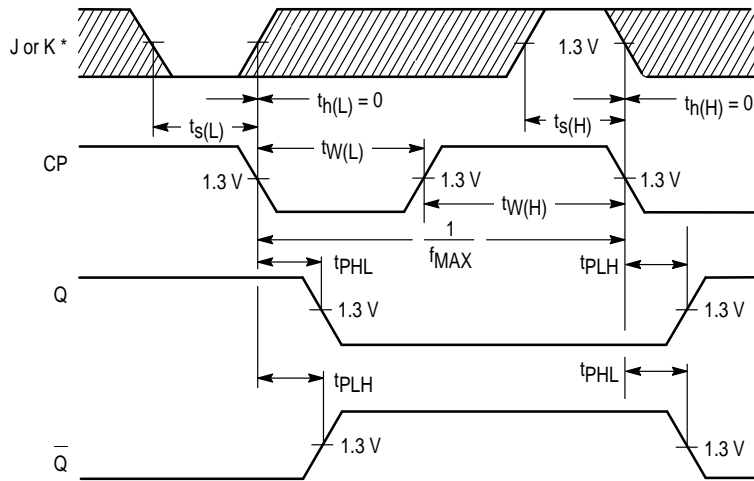
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Clock Frequency	30	45		MHz	Figure 1
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Clock to Output		15	20	ns	Figure 1
			15	20	ns	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>W</sub>	Clock Pulse Width High	20			ns	Figure 1
t <sub>W</sub>	Clear Pulse Width	25			ns	Figure 2
t <sub>s</sub>	Setup Time	20			ns	Figure 1 V <sub>CC</sub> = 5.0 V
t <sub>h</sub>	Hold Time	0			ns	

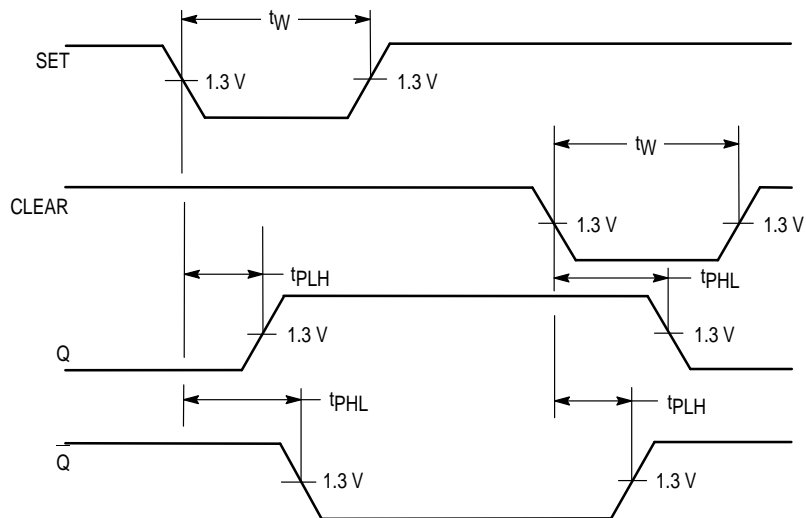
# SN54/74LS73A

## AC WAVEFORMS



\*The shaded areas indicate when the input is permitted to change for predictable output performance.

**Figure 1. Clock to Output Delays, Data Set-Up and Hold Times, Clock Pulse Width**



**Figure 2. Set and Clear to Output Delays, Set and Clear Pulse Widths**