

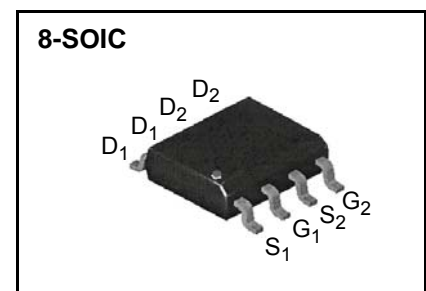
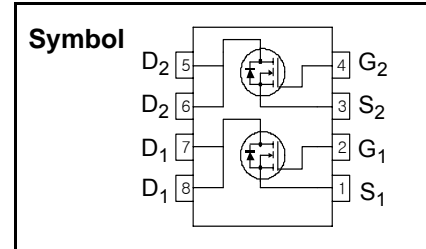
## Dual N-Channel MOSFET

### Features

- Low  $R_{DS(on)}$  ( $0.030\Omega$ )@ $V_{GS}=4.5V$   
Low  $R_{DS(on)}$  ( $0.043\Omega$ )@ $V_{GS}=2.5V$
- Gate Charge (Typical 14nC)
- Improved dv/dt Capability
- Maximum Junction Temperature Range ( $150^{\circ}C$ )
- Available in Tape and Reel

### General Description

This Power MOSFET is produced using SemiWell's advanced planar stripe, DMOS technology. This latest technology has been especially designed to minimize on-state resistance, have a low gate charge with superior switching performance, and rugged avalanche characteristics. This Power MOSFET is well suited for Battery protection circuit, Load switch and other power management application.



### Absolute Maximum Ratings

Symbol	Parameter	Value	Units
$V_{DSS}$	Drain to Source Voltage	20	V
$I_D$	Continuous Drain Current(@ $T_A = 25^{\circ}C$ )	6.5	A
$I_{DM}$	Drain Current Pulsed (Note 1)	30	A
$V_{GS}$	Gate to Source Voltage	$\pm 12$	V
$P_D$	Total Power Dissipation Single Operation ( $T_A=25^{\circ}C$ )	2.0	W
	Total Power Dissipation Single Operation ( $T_A=70^{\circ}C$ )	1.28	W
$T_{STG}, T_J$	Operating Junction Temperature & Storage Temperature	- 55 ~ 150	$^{\circ}C$
$T_L$	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.	300	$^{\circ}C$

### Thermal Characteristics

Symbol	Parameter	Value			Units
		Min.	Typ.	Max.	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 4)	-	-	62.5	$^{\circ}C/W$

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## Electrical Characteristics ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted )

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	20	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature coefficient	$I_D = 250\mu A$ , referenced to $25\text{ }^\circ\text{C}$	-	24	-	mV/°C
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS} = 16V, V_{GS} = 0V$	-	-	1	$\mu A$
$I_{GSS}$	Gate-Source Leakage, Forward	$V_{GS} = 12V, V_{DS} = 0V$	-	-	100	nA
	Gate-Source Leakage, Reverse	$V_{GS} = -12V, V_{DS} = 0V$	-	-	-100	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.5	-	1.5	V
$R_{DS(ON)}$	Static Drain-Source On-state Resistance	$V_{GS} = 4.5V, I_D = 6.5A$ $V_{GS} = 2.5V, I_D = 5.4A$	-	0.025 0.036	0.030 0.043	$\Omega$
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0V, V_{DS} = 10V, f = 1MHz$	-	645	-	pF
$C_{oss}$	Output Capacitance		-	350	-	
$C_{rss}$	Reverse Transfer Capacitance		-	115	-	
<b>Dynamic Characteristics</b>						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 10V, I_D = 1A, R_G = 50\ \Omega$ $V_{GS} = 4.5V$ (Note 2,3)	-	9	28	ns
$t_r$	Rise Time		-	45	100	
$t_{d(off)}$	Turn-off Delay Time		-	95	200	
$t_f$	Fall Time		-	60	130	
$Q_g$	Total Gate Charge	$V_{DS} = 10V, V_{GS} = 4.5V, I_D = 4.5A$ (Note 2,3)	-	14	18	nC
$Q_{gs}$	Gate-Source Charge		-	2.5	-	
$Q_{gd}$	Gate-Drain Charge(Miller Charge)		-	5	-	

## Source-Drain Diode Ratings and Characteristics

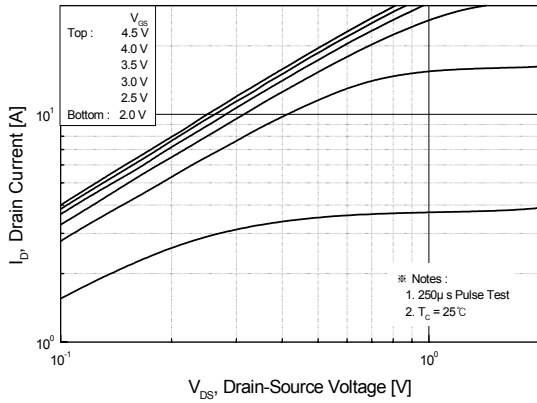
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
$I_S$	Maximum Continuous Diode Forward Current		-	-	1.3	A
$V_{SD}$	Diode Forward Voltage	$I_S = 1.3A, V_{GS} = 0V$ (Note 2)	-	-	1.2	V

### ※ NOTES

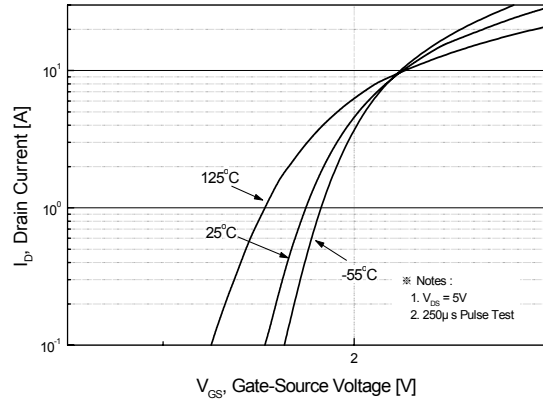
1. Repeatability rating : pulse width limited by junction temperature
2. Pulse Test : Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$
3. Essentially independent of operating temperature.
4. Surface mounted on 1 inch<sup>2</sup> Cu board.



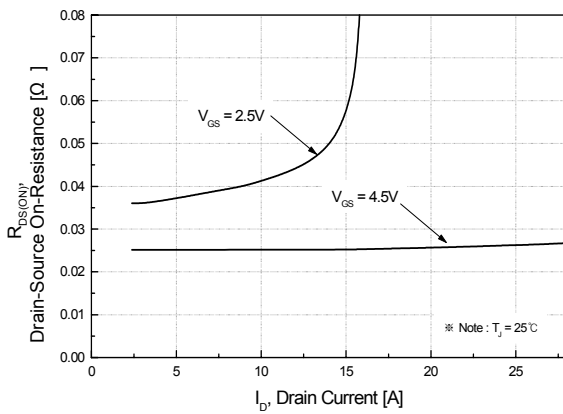
**Fig 1. On-State Characteristics**



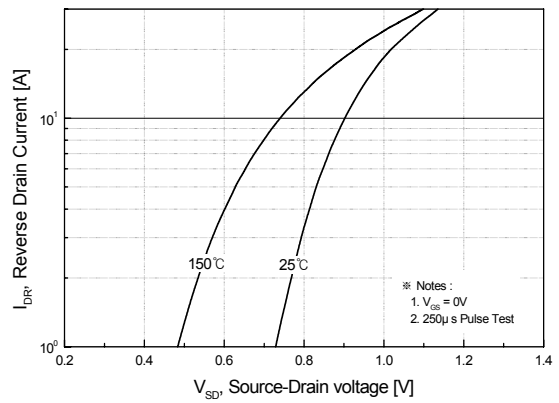
**Fig 2. Transfer Characteristics**



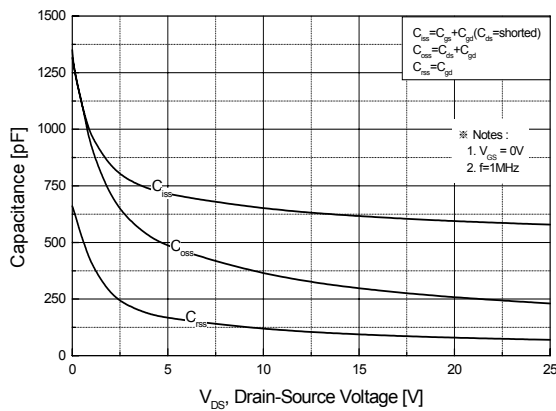
**Fig 3. On Resistance Variation vs. Drain Current and Gate Voltage**



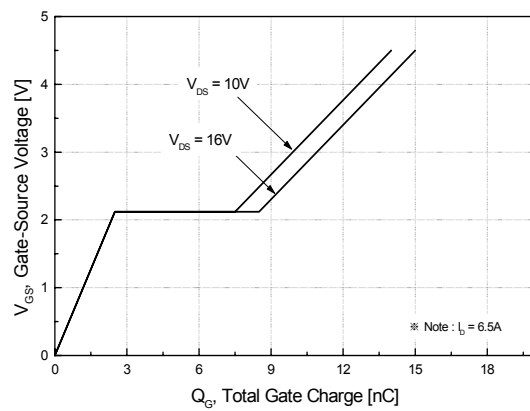
**Fig 4. On State Current vs. Allowable Case Temperature**



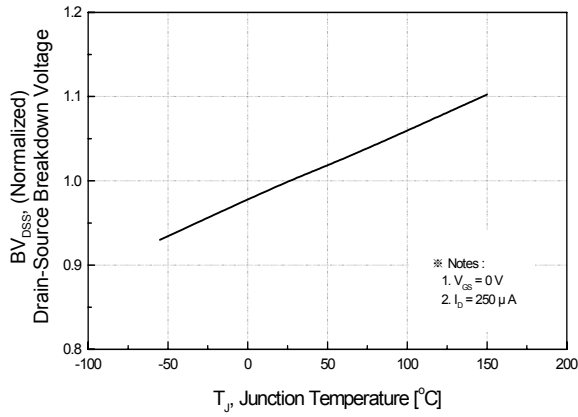
**Fig 5. Capacitance Characteristics**



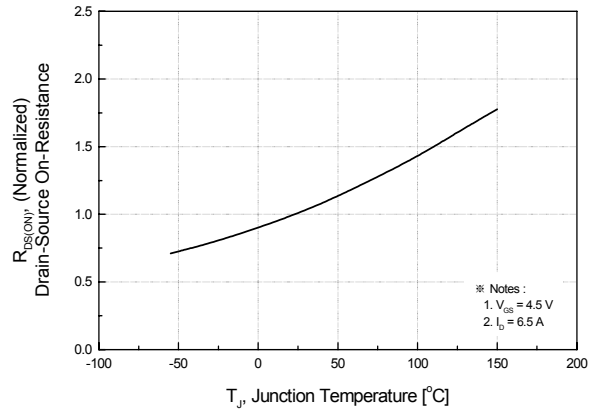
**Fig 6. Gate Charge Characteristics**



**Fig 7. Breakdown Voltage Variation vs. Junction Temperature**



**Fig 8. On-Resistance Variation vs. Junction Temperature**



**Fig 9. Normalized Transient Thermal Response Curve**

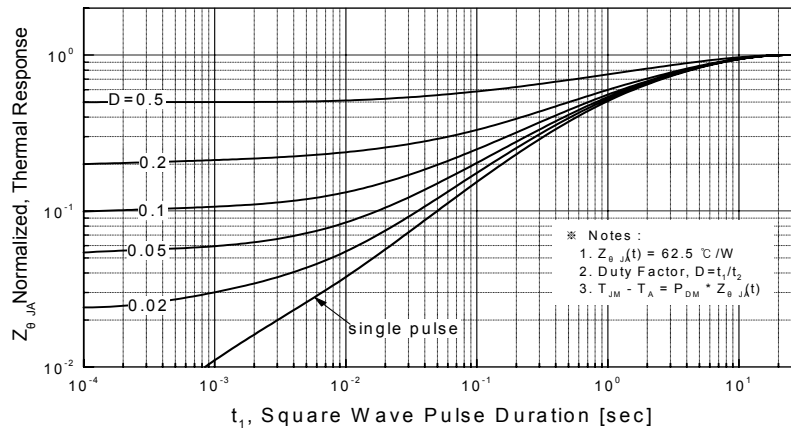


Fig. 10. Gate Charge Test Circuit & Waveforms

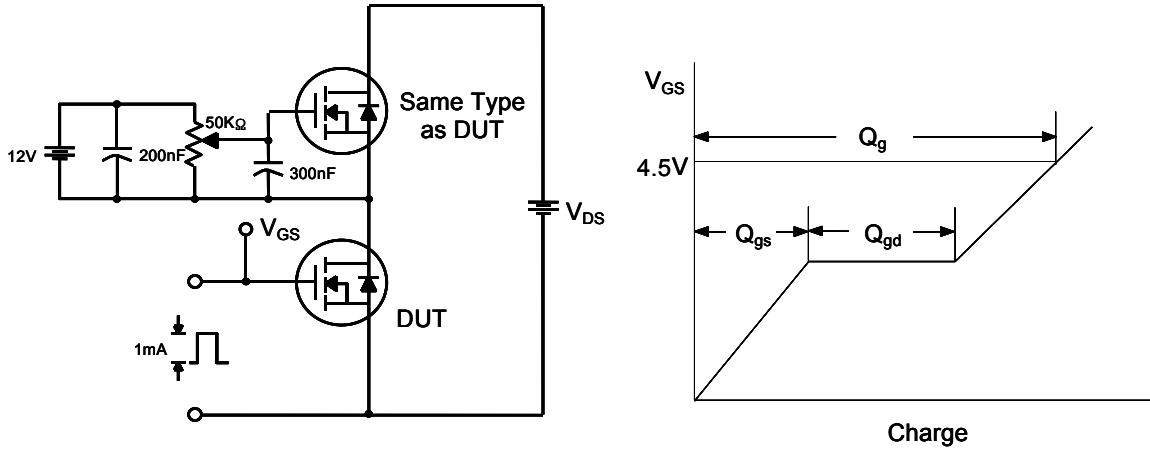
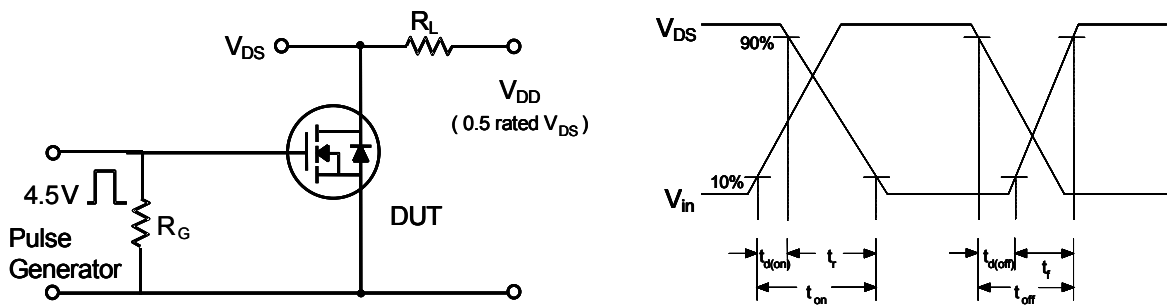


Fig. 11. Switching Time Test Circuit & Waveforms



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## 8-SOIC Package Dimension

Dim.	mm			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35	1.55	1.75	0.053	0.061	0.069
B	0.1	0.175	0.25	0.004	0.007	0.010
C	0.38	0.445	0.510	0.015	0.018	0.020
D	0.19	0.22	0.25	0.007	0.009	0.010
E	4.8	4.9	5	0.189	0.193	0.197
F	3.8	3.9	4	0.150	0.154	0.157
G	1.27 BSC					
H	5.8	6	6.2	0.228	0.236	0.244
I	0.5	0.715	0.93	0.020	0.028	0.037
J	0'	4'	8'	0'	4'	8'
K	0.250	0.375	0.05	0.010	0.015	0.020

