

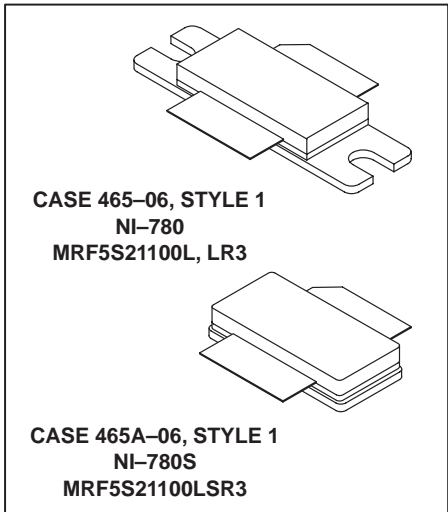
The RF MOSFET Line  
**RF Power Field Effect Transistors**  
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

- Typical 2-carrier W-CDMA Performance for  $V_{DD} = 28$  Volts,  $I_{DQ} = 1050$  mA,  $f_1 = 2135$  MHz,  $f_2 = 2145$  MHz, Channel Bandwidth = 3.84 MHz, Adjacent Channels Measured over 3.84 MHz BW @  $f_1 - 5$  MHz and  $f_2 + 5$  MHz, Distortion Products Measured over a 3.84 MHz BW @  $f_1 - 10$  MHz and  $f_2 + 10$  MHz, Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.
  - Output Power — 23 Watts Avg.
  - Power Gain — 13.5 dB
  - Efficiency — 26%
  - IM3 — -37 dBc
  - ACPR — -40 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2140 MHz, 100 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Qualified Up to a Maximum of 32  $V_{DD}$  Operation
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.
- Low Gold Plating Thickness on Leads. L Suffix Indicates 40 $\mu$ m Nominal.

**MRF5S21100L**  
**MRF5S21100LR3**  
**MRF5S21100LSR3**

**2170 MHz, 23 W AVG.,**  
**2 x W-CDMA, 28 V**  
**LATERAL N-CHANNEL**  
**RF POWER MOSFETs**



**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	65	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	$P_D$	250 1.43	Watts W/°C
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Operating Junction Temperature	$T_J$	200	°C

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 100 W CW Case Temperature 80°C, 23 W CW	$R_{\theta JC}$	0.70 0.76	°C/W

**ESD PROTECTION CHARACTERISTICS**

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)
Charge Device Model	C7 (Minimum)

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate–Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	0.5	$\mu\text{Adc}$

**ON CHARACTERISTICS (DC)**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 250\ \mu\text{Adc}$ )	$V_{GS(th)}$	2.5	2.8	3.5	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_D = 1050\text{ mA}$ )	$V_{GS(Q)}$	—	3.8	—	Vdc
Drain–Source On–Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 2.5\text{ Adc}$ )	$V_{DS(on)}$	—	0.24	0.3	Vdc
Forward Transconductance ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 2.5\text{ Adc}$ )	$g_{fs}$	—	6	—	S

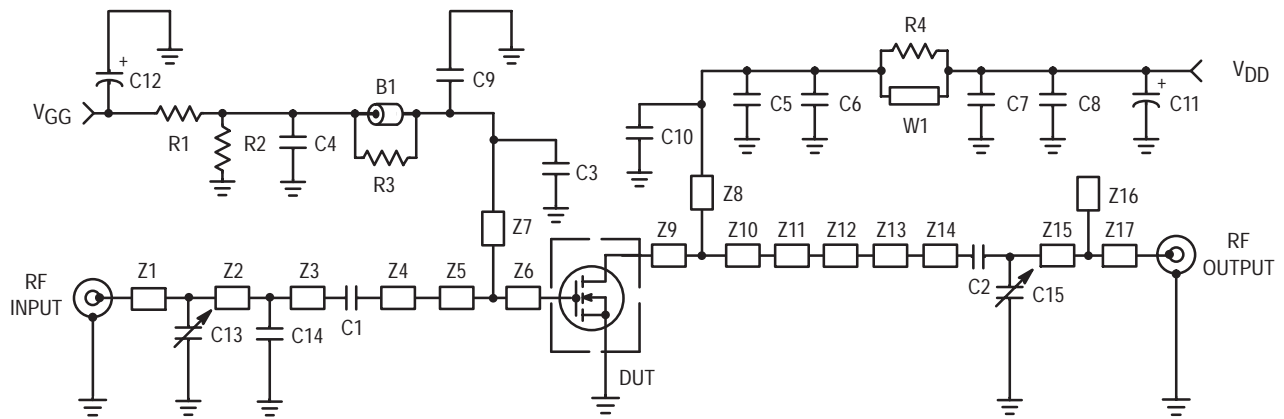
**DYNAMIC CHARACTERISTICS (1)**

Reverse Transfer Capacitance ( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{rss}$	—	2.14	—	pF
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**FUNCTIONAL TESTS** (In Motorola Test Fixture, 50 ohm system) 2–carrier W–CDMA, 3.84 MHz Channel Bandwidth Carriers, ACPR and IM3 measured in 3.84 MHz Bandwidth. Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.

Common–Source Amplifier Power Gain ( $V_{DD} = 28\text{ Vdc}$ , $P_{out} = 23\text{ W Avg.}$ , $I_{DQ} = 1050\text{ mA}$ , $f_1 = 2112.5\text{ MHz}$ , $f_2 = 2122.5\text{ MHz}$ and $f_1 = 2157.5\text{ MHz}$ , $f_2 = 2167.5\text{ MHz}$ )	$G_{ps}$	12.5	13.5	—	dB
Drain Efficiency ( $V_{DD} = 28\text{ Vdc}$ , $P_{out} = 23\text{ W Avg.}$ , $I_{DQ} = 1050\text{ mA}$ , $f_1 = 2112.5\text{ MHz}$ , $f_2 = 2122.5\text{ MHz}$ and $f_1 = 2157.5\text{ MHz}$ , $f_2 = 2167.5\text{ MHz}$ )	$\eta$	24	26	—	%
Third Order Intermodulation Distortion ( $V_{DD} = 28\text{ Vdc}$ , $P_{out} = 23\text{ W Avg.}$ , $I_{DQ} = 1050\text{ mA}$ , $f_1 = 2112.5\text{ MHz}$ , $f_2 = 2122.5\text{ MHz}$ and $f_1 = 2157.5\text{ MHz}$ , $f_2 = 2167.5\text{ MHz}$ ; IM3 measured over 3.84 MHz BW at $f_1 -10\text{ MHz}$ and $f_2 +10\text{ MHz}$ referenced to carrier channel power.)	IM3	—	–37	–35	dBc
Adjacent Channel Power Ratio ( $V_{DD} = 28\text{ Vdc}$ , $P_{out} = 23\text{ W Avg.}$ , $I_{DQ} = 1050\text{ mA}$ , $f_1 = 2112.5\text{ MHz}$ , $f_2 = 2122.5\text{ MHz}$ and $f_1 = 2157.5\text{ MHz}$ , $f_2 = 2167.5\text{ MHz}$ ; ACPR measured over 3.84 MHz at $f_1 -5\text{ MHz}$ and $f_2 +5\text{ MHz}$ .)	ACPR	—	–40	–38	dBc
Input Return Loss ( $V_{DD} = 28\text{ Vdc}$ , $P_{out} = 23\text{ W Avg.}$ , $I_{DQ} = 1050\text{ mA}$ , $f_1 = 2112.5\text{ MHz}$ , $f_2 = 2122.5\text{ MHz}$ and $f_1 = 2157.5\text{ MHz}$ , $f_2 = 2167.5\text{ MHz}$ )	IRL	—	–16	–9	dB

(1) Part is internally matched both on input and output.



Z1	0.674" x 0.080" Microstrip	Z10	0.368" x 1.136" Microstrip
Z2	0.421" x 0.080" Microstrip	Z11	0.151" x 0.393" Microstrip
Z3	0.140" x 0.080" Microstrip	Z12	0.280" x 0.220" Microstrip
Z4	1.031" x 0.080" Microstrip	Z13	0.481" x 0.142" Microstrip
Z5	0.380" x 0.643" Microstrip	Z14	0.138" x 0.080" Microstrip
Z6	0.080" x 0.643" Microstrip	Z15	0.344" x 0.080" Microstrip
Z7	0.927" x 0.048" Microstrip	Z16	0.147" x 0.099" Microstrip
Z8	0.620" x 0.048" Microstrip	Z17	0.859" x 0.080" Microstrip
Z9	0.079" x 1.136" Microstrip	PCB	Arlon GX-0300-SS-22, 30 mil, $\epsilon_r = 2.55$

Figure 1. MRF5S21100L Test Circuit Schematic

Table 1. MRF5S21100L Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
B1	Short RF Bead	95F786	Newark
C1, C2	8.2 pF Chip Capacitors, B Case	100B8R2CP500X	ATC
C3	5.6 pF Chip Capacitor, B Case	100B5R6CP500X	ATC
C4	0.1 $\mu$ F Chip Capacitor, B Case	CDR33BX104AKWS	Kemet
C5, C7	7.5 pF Chip Capacitors, B Case	100B7R5JP500X	ATC
C6	1.2 pF Chip Capacitor, B Case	100B1R2BP500X	ATC
C8	1K pF Chip Capacitor, B Case	100B102JP500X	ATC
C9, C10	0.56 $\mu$ F Chip Capacitors, B Case	700A561MP150X	Kemet
C11	470 $\mu$ F, 63 V Electrolytic Capacitor	95F4579	Newark
C12	100 $\mu$ F, 50 V Electrolytic Capacitor	51F2913	Newark
C13	0.6–4.5 pF Gigatrim Variable Capacitor	44F3358	Newark
C14	2.7 pF Chip Capacitor, B Case	100B2R7CP500X	ATC
C15	0.4–2.5 pF Gigatrim Variable Capacitor	44F3367	Newark
R1	1 k $\Omega$ Chip Resistor	D5534M07B1K00R	Newark
R2	560 k $\Omega$ Chip Resistor	CR1206564JT	Newark
R3, R4	12 $\Omega$ Chip Resistors	RM73B2B120JT	Garrett Electronics
W1	Wire Strap	14 Gauge Jumper Wire	

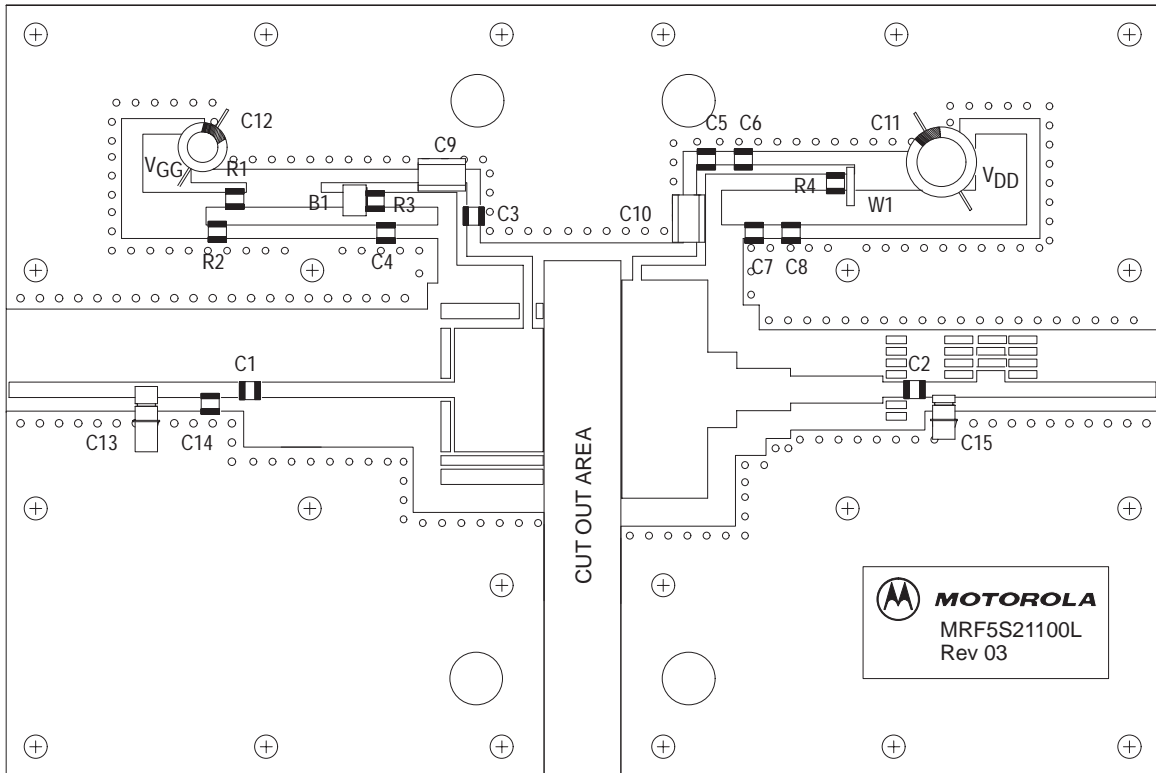
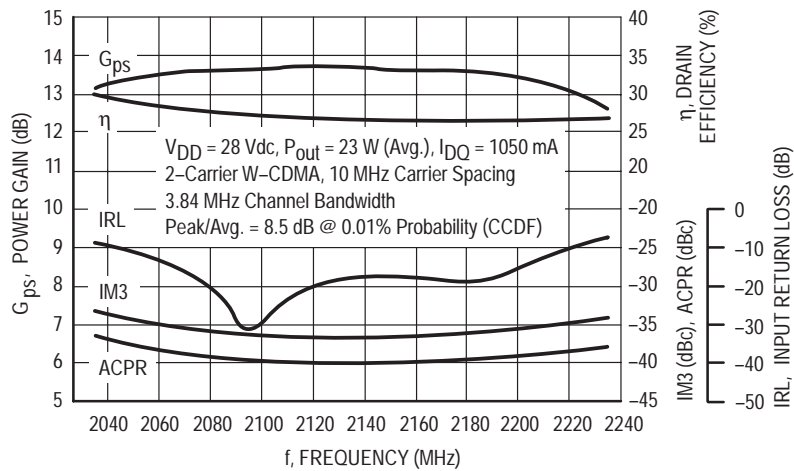
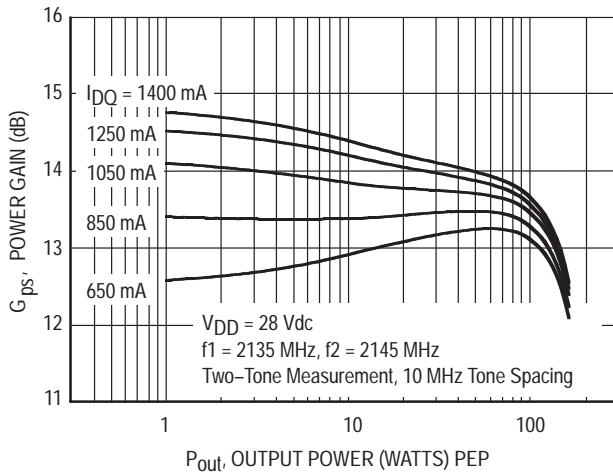


Figure 2. MRF5S21100L Test Circuit Component Layout

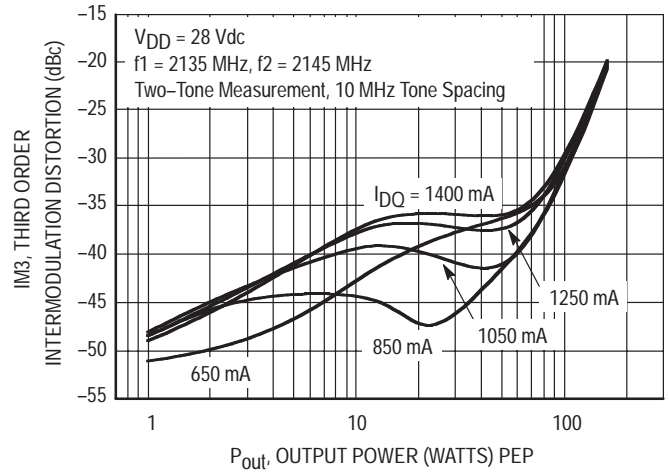
## TYPICAL CHARACTERISTICS



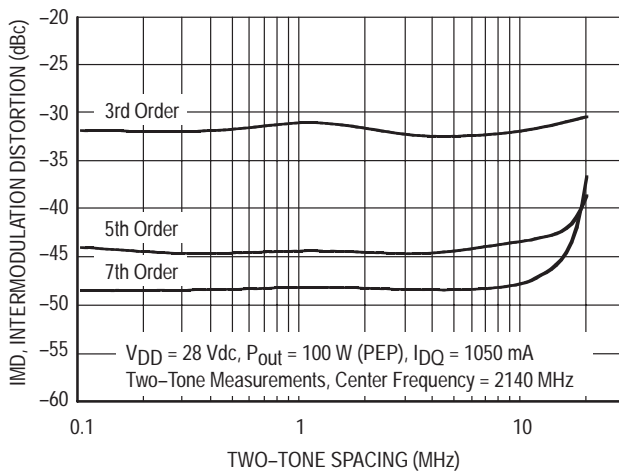
**Figure 3. 2-Carrier W-DCMA Broadband Performance**



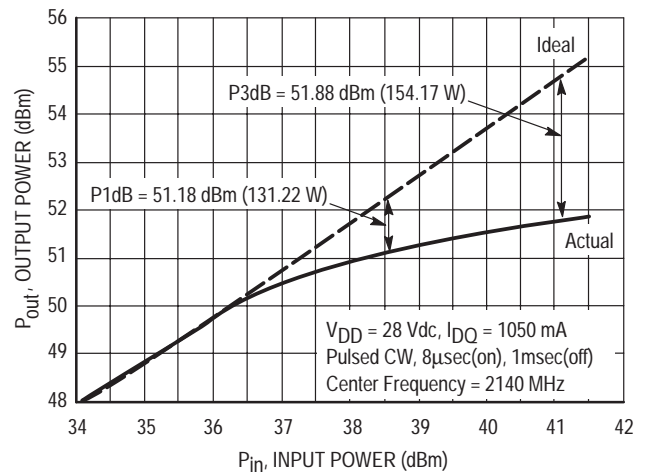
**Figure 4. Two-Tone Power Gain versus Output Power**



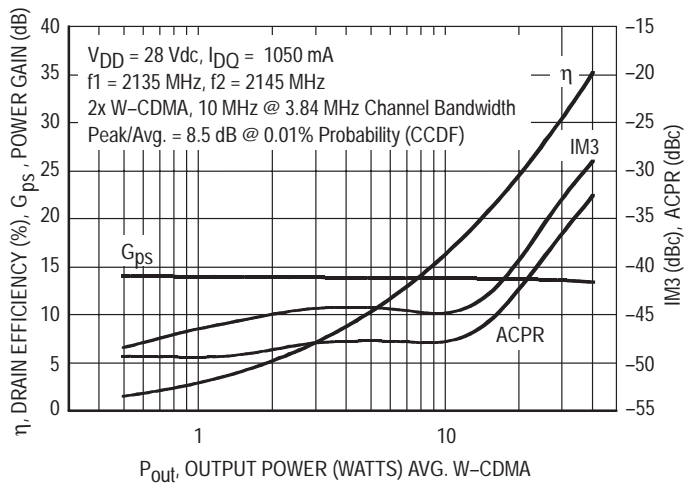
**Figure 5. Third Order Intermodulation Distortion versus Output Power**



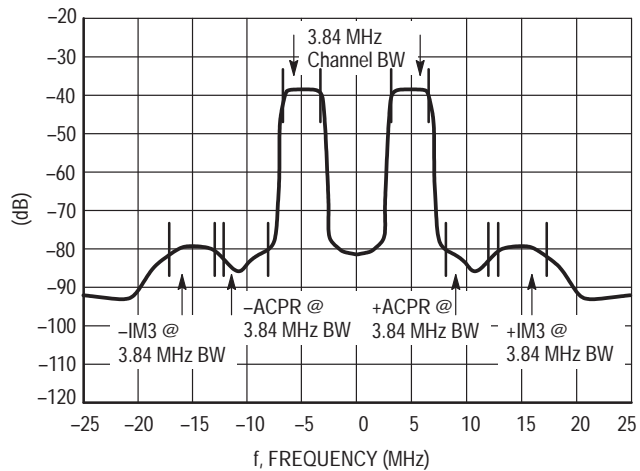
**Figure 6. Intermodulation Distortion Products versus Tone Spacing**



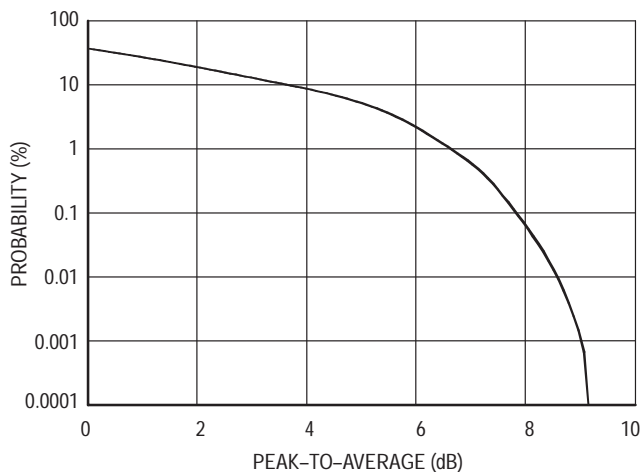
**Figure 7. Pulse CW Output Power versus Input Power**



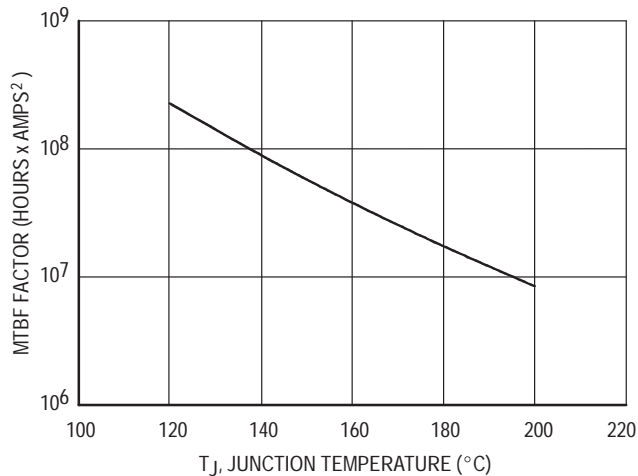
**Figure 8. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power**



**Figure 9. 2-Carrier W-CDMA Spectrum**

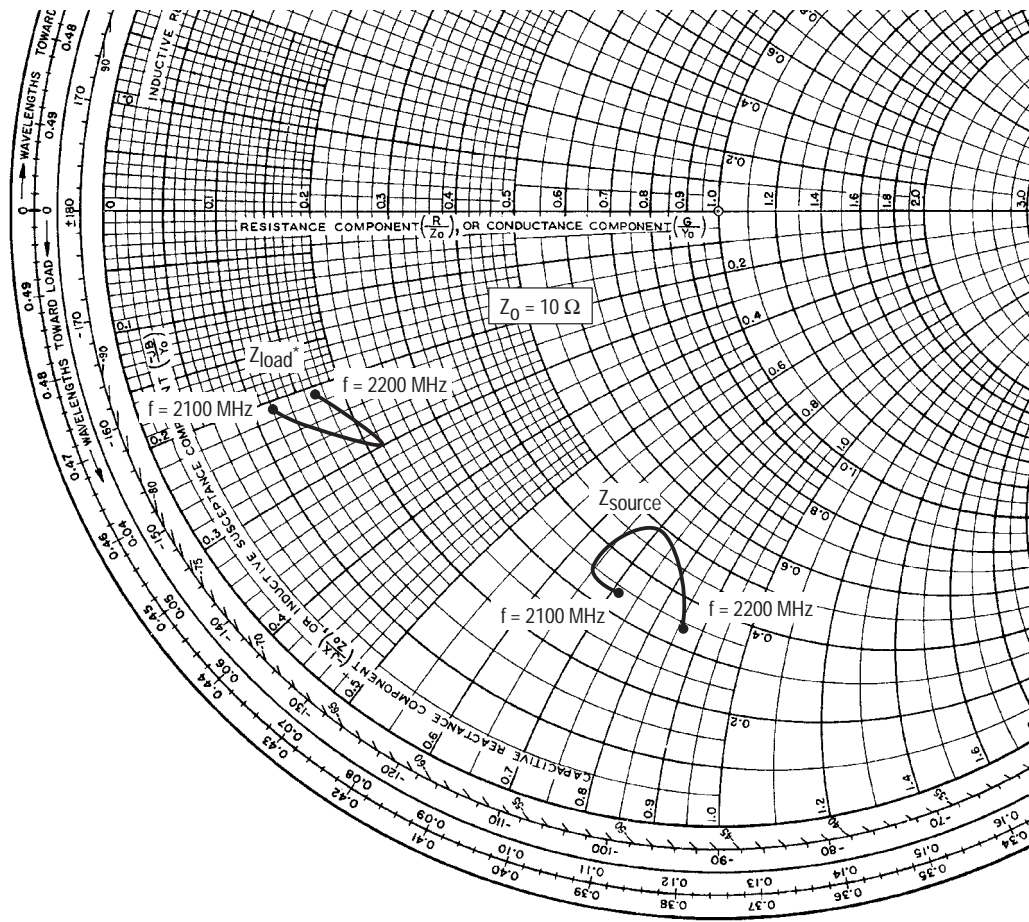


**Figure 10. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 67% Clipping, Single Carrier Test Signal**



This above graph displays calculated MTBF in hours x ampere<sup>2</sup> drain current. Life tests at elevated temperatures have correlated to better than  $\pm 10\%$  of the theoretical prediction for metal failure. Divide MTBF factor by  $I_D^2$  for MTBF in a particular application.

**Figure 11. MTBF Factor versus Junction Temperature**



$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 1050 \text{ mA}$ ,  $P_{out} = 23 \text{ W Avg.}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
2100	$3.4 - j7.2$	$1.2 - j2.1$
2120	$3.4 - j6.5$	$1.4 - j2.3$
2160	$4.9 - j7.0$	$2.2 - j3.0$
2200	$3.4 - j8.6$	$1.7 - j2.1$

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

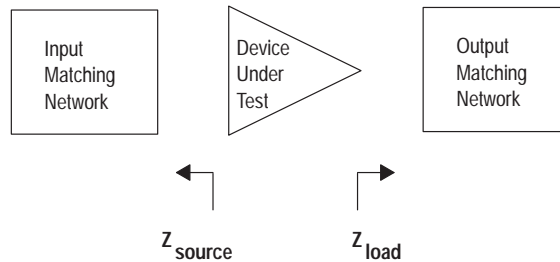


Figure 12. Series Equivalent Input and Output Impedance

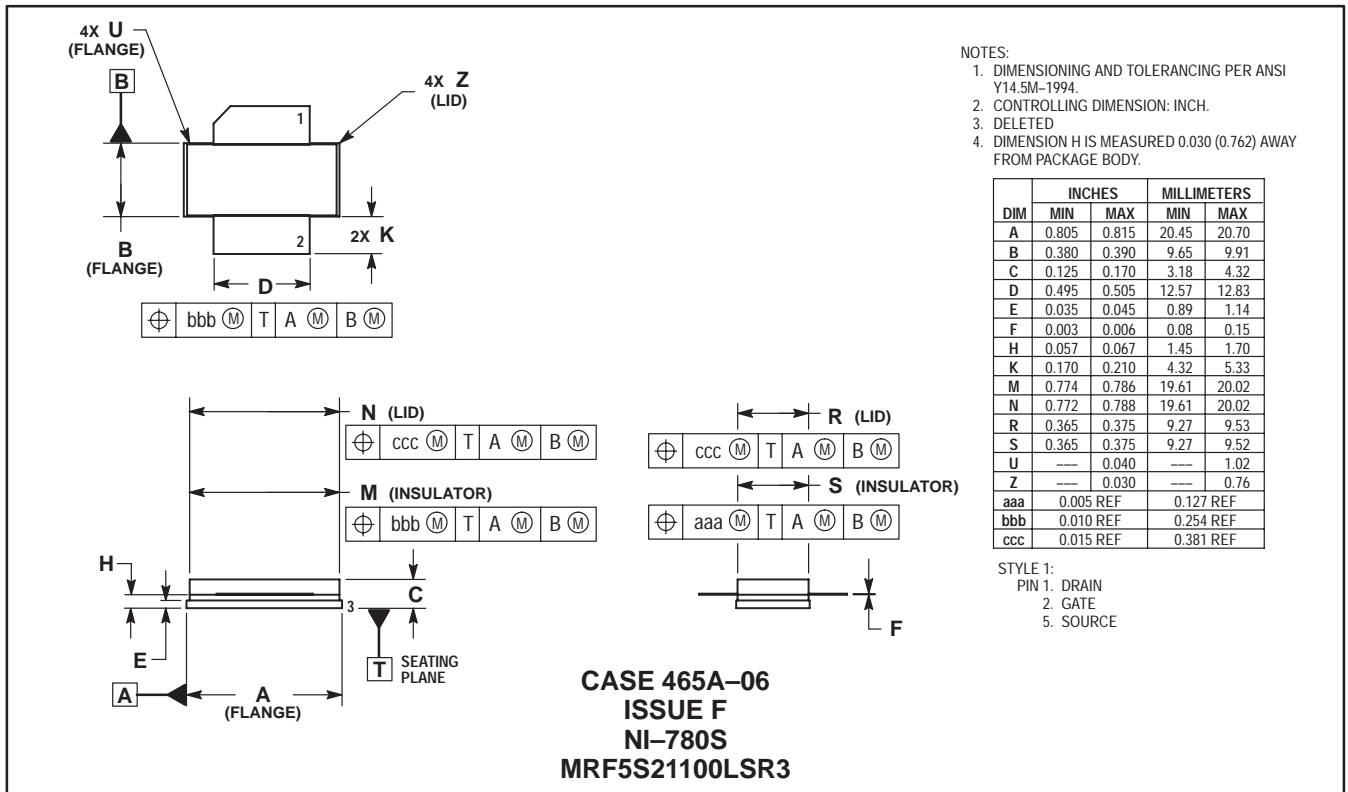
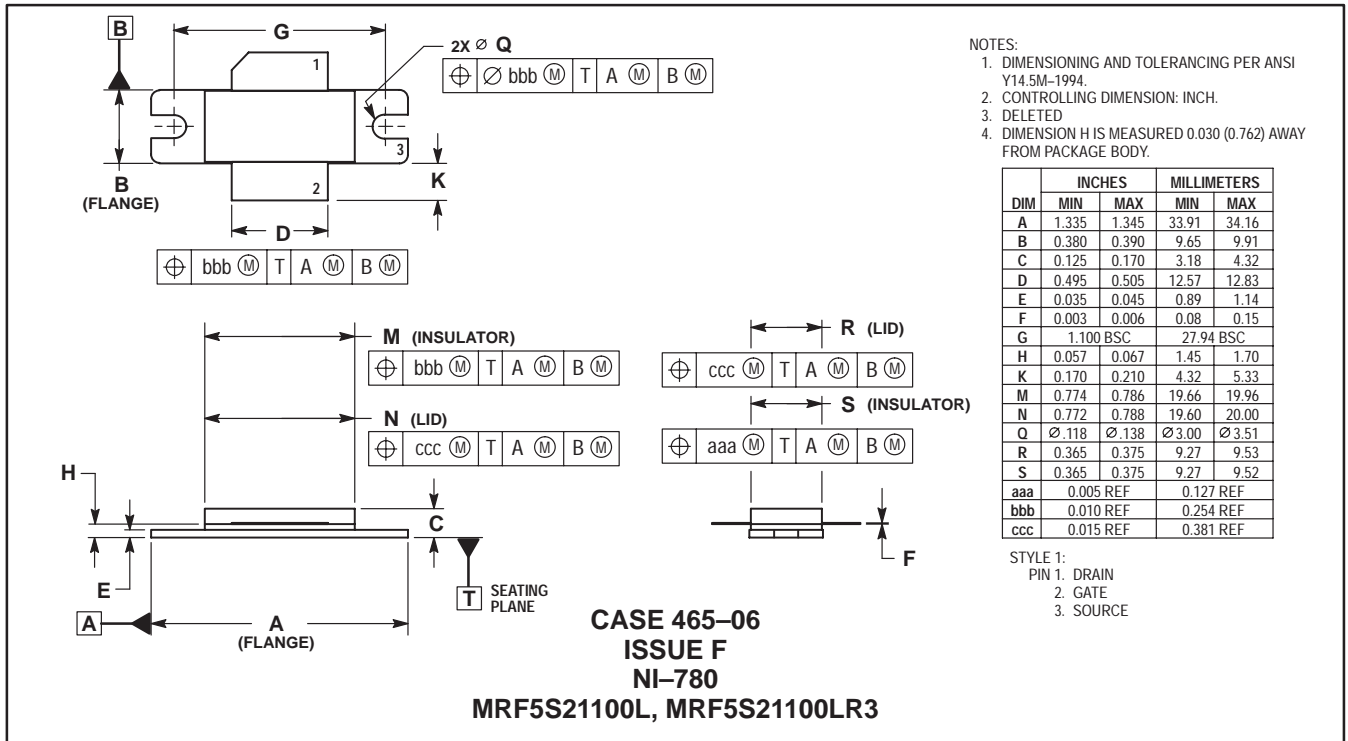
# NOTES



# NOTES

# NOTES

## PACKAGE DIMENSIONS



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