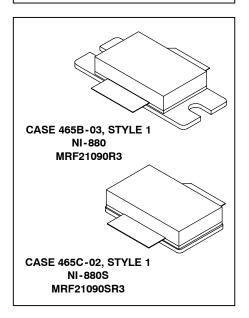
# The RF Sub-Micron MOSFET Line **RF Power Field Effect Transistors**N-Channel Enhancement-Mode Lateral MOSFETs

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications.

- Typical W-CDMA Performance for 2140 MHz, 28 Volts
   4.096 MHz BW @ 5 MHz offset, 1 PERCH 15 DTCH:
   Output Power 11.5 Watts
   Efficiency 16%
   Gain 12.2 dB
   ACPR -45 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2110 MHz, 90 Watts CW Output Power
- · Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

## MRF21090R3 MRF21090SR3

2170 MHz, 90 W, 28 V LATERAL N-CHANNEL RF POWER MOSFETs



#### **MAXIMUM RATINGS**

Rating		Value	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	65	Vdc	
Gate-Source Voltage	V <sub>GS</sub>	+15, -0.5	Vdc	
Total Device Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	270 1.54	Watts W/°C	
Storage Temperature Range	T <sub>stg</sub>	- 65 to +150	°C	
Operating Junction Temperature	TJ	200	°C	

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

NOTE - <u>CAUTION</u> - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.





#### **ESD PROTECTION CHARACTERISTICS**

Test Conditions		Class	
Human Body Model	MRF21090R3 MRF21090SR3	2 (Minimum) 1 (Minimum)	
Machine Model	MRF21090R3 MRF21090SR3	M3 (Minimum) M4 (Minimum)	

ELECTRICAL CHARACTERISTICS (T <sub>C</sub> = 25°C unless otherwise noted)					
Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage $(V_{GS} = 0 \text{ Vdc}, I_D = 100 \mu\text{Adc})$	V <sub>(BR)DSS</sub>	65	_		Vdc
Gate-Source Leakage Current (V <sub>GS</sub> = 5 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	_	_	1	μAdc
Zero Gate Voltage Drain Leakage Current $(V_{DS} = 28 \text{ Vdc}, V_{GS} = 0 \text{ Vdc})$	I <sub>DSS</sub>	_	_	10	μAdc
ON CHARACTERISTICS					
Forward Transconductance (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 3 Adc)	9fs	_	7.2	_	S
Gate Threshold Voltage ( $V_{DS}$ = 10 V, $I_{D}$ = 300 $\mu$ A)	V <sub>GS(th)</sub>	2	3	4	Vdc
Gate Quiescent Voltage (V <sub>DS</sub> = 28 V, I <sub>D</sub> = 750 mA)	V <sub>GS(Q)</sub>	3	3.8	5	Vdc
Drain-Source On-Voltage (V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1 A)	V <sub>DS(on)</sub>	_	0.1	0.6	Vdc
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V <sub>DS</sub> = 28 Vdc, V <sub>GS</sub> = 0, f = 1 MHz)	C <sub>rss</sub>	_	4.2	_	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)	FUNCTIONAL TESTS (In Motorola Test Fixture)				
Common-Source Amplifier Power Gain $(V_{DD}=28\ Vdc,\ P_{out}=90\ W\ PEP,\ I_{DQ}=750\ mA,\ f1=2110.0\ MHz,\ f2=2110.1\ MHz\ and\ f1=2170.0\ MHz,\ f2=2170.1\ MHz)$	G <sub>ps</sub>	10	11.7	_	dB
Drain Efficiency $(V_{DD}=28\ Vdc,\ P_{out}=90\ W\ PEP,\ I_{DQ}=750\ mA,\ f1=2110.0\ MHz,\ f2=2110.1\ MHz\ and\ f1=2170.0\ MHz,\ f2=2170.1\ MHz)$	η	30	33	_	%
Intermodulation Distortion ( $V_{DD}$ = 28 Vdc, $P_{out}$ = 90 W PEP, $I_{DQ}$ = 750 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz and f1 = 2170.0 MHz, f2 = 2170.1 MHz)	IMD	=	-30	-27.5	dBc
Input Return Loss $(V_{DD}=28\ Vdc,\ P_{out}=90\ W\ PEP,\ I_{DQ}=750\ mA,\ f1=2110.0\ MHz,\ f2=2110.1\ MHz\ and\ f1=2170.0\ MHz,\ f2=2170.1\ MHz)$	IRL	=	-12	-9.0	dB
Common-Source Amplifier Power Gain (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 75 W CW, I <sub>DQ</sub> = 750 mA, f = 2170 MHz)	G <sub>ps</sub>	_	11.7	_	dB
Drain Efficiency (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 75 W CW, I <sub>DQ</sub> = 750 mA, f = 2170 MHz)	η	_	41	_	%
Output Mismatch Stress $(V_{DD}=28\ Vdc,\ P_{out}=90\ W\ CW,\ I_{DQ}=750\ mA,\ f=2110\ MHz,\ VSWR=10:1,\ All\ Phase\ Angles\ at\ Frequency\ of\ Tests)$	Ψ	No	Degradation Before and	In Output Po	wer

<sup>(1)</sup> Part is internally matched both on input and output.

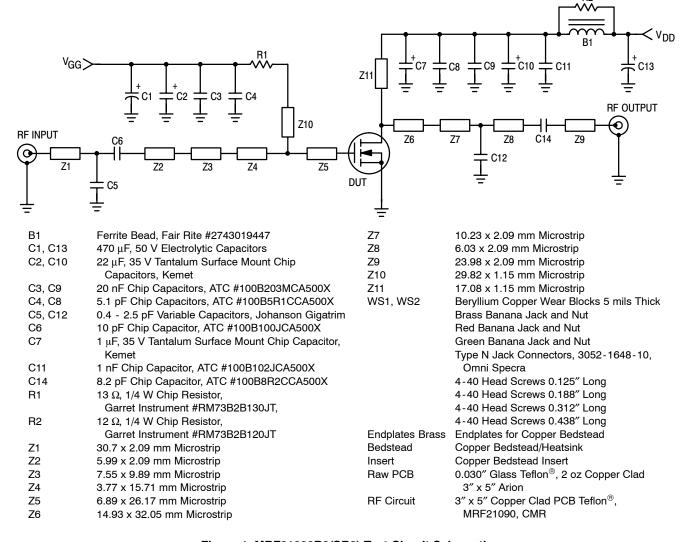


Figure 1. MRF21090R3(SR3) Test Circuit Schematic

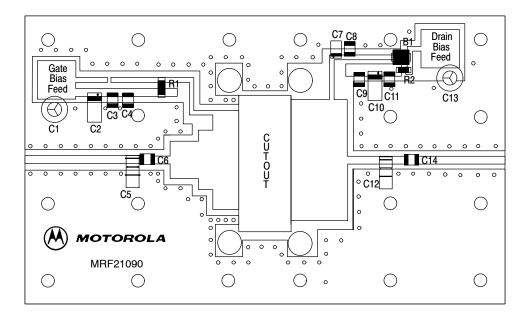


Figure 2. MRF21090R3(SR3) Test Circuit Component Layout

#### TYPICAL PERFORMANCE (IN MOTOROLA TEST FIXTURE)

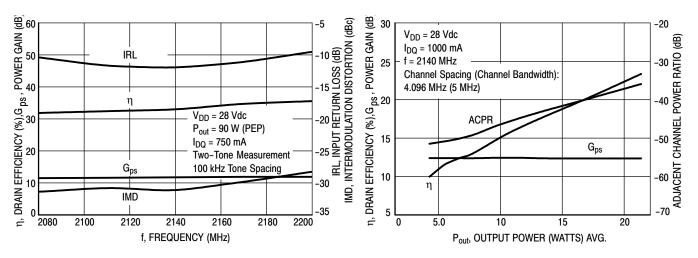


Figure 3. Class AB Broadband Circuit Performance

Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

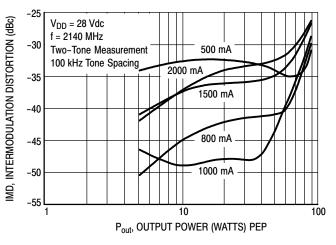


Figure 5. Intermodulation Distortion versus
Output Power

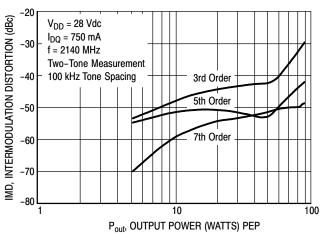


Figure 6. Intermodulation Distortion Products versus Output Power

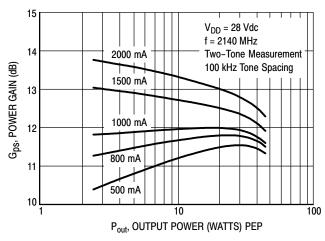


Figure 7. Power Gain versus Output Power

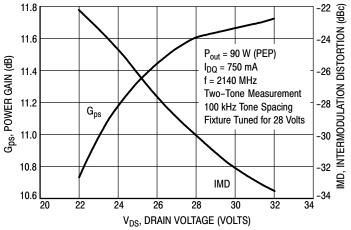
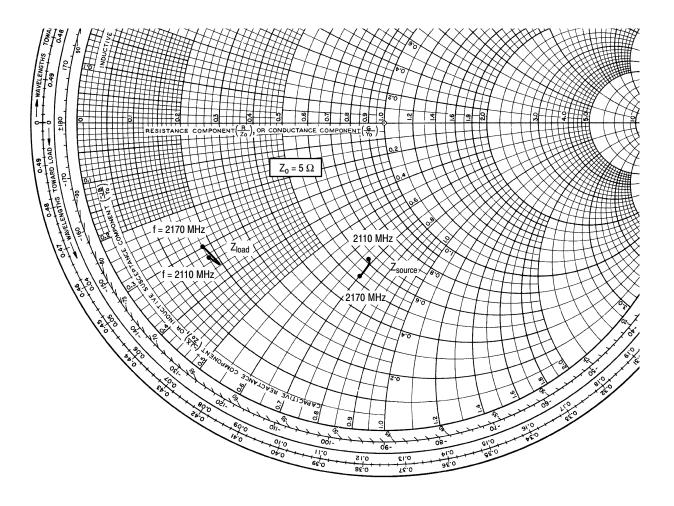


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



 $V_{DD} = 28 \text{ V}, I_{DQ} = 750 \text{ mA}, P_{out} = 90 \text{ W} \text{ (PEP)}$ 

f MHz	$\mathbf{Z_{source}}_{\Omega}$	$\mathbf{Z_{load}}_{\Omega}$
2110	3.03 - j3.40	0.92 - j1.67
2140	3.02 - j3.46	0.97 - j1.80
2170	2.60 - j3.50	0.90 - j1.52

Z<sub>source</sub> = Test circuit impedance as measured from gate to ground.

Z<sub>load</sub> = Test circuit impedance as measured from drain to ground.

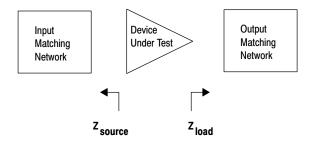
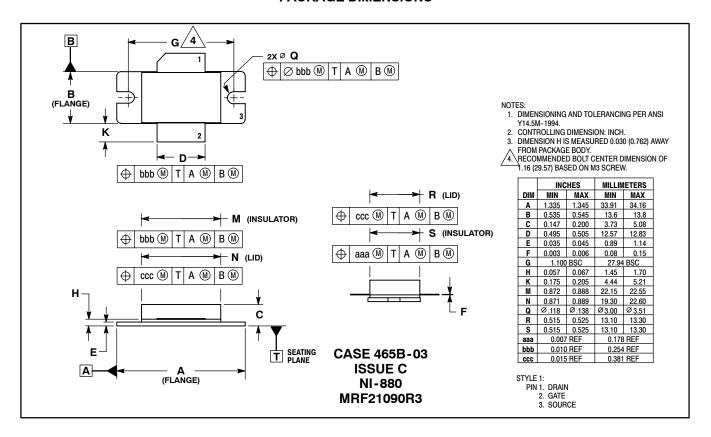
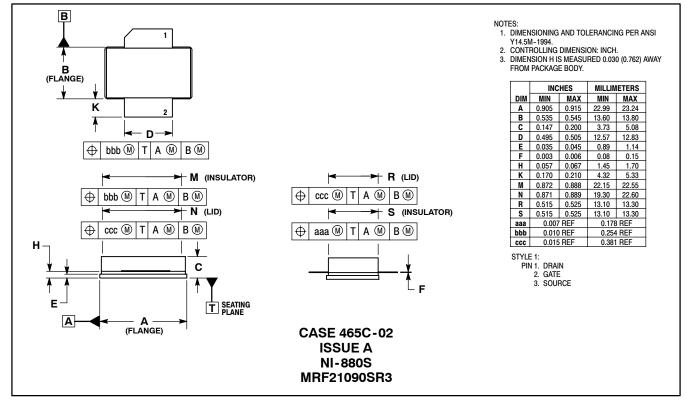


Figure 9. Series Equivalent Source and Load Impedance

#### **PACKAGE DIMENSIONS**





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