☐ MN103004K , MN103016K

Type	MN103004K	MN103016K
Command ROM (×64-bit)	256 K-byte	256 K-byte
Data RAM (×32-bit)	10 K-byte	10 K-byte
Package **(Old Package)**	QFP208-P-2828F *Pb free , FLGA239-C-1313 (QFP208-P-2828A)	FLGA239-C-1313
Minimum Instruction Execution Time	25 ns (at 2.7 V to 3.6 V, 40 MHz)	
Interrupts	• RESET • IRQ × 8 • NMI • Timer × 22 • Input capture × 14 • PWM × 4 • SIF × 16 • DMAC × 4 • WDT • A/D • System error	

Timer Counter

Timer counter 0 to 3: 32-bit × 1 (interval timer, event count, toggle output, interrupt, A/D conversion trigger)
  Clock source ····················· IOCLK; IOCLK/8; IOCLK/32; external clock input; underflow of timer counter
  Interrupt source ············· underflow of timer counter 0, 1, 2, 3

Timer counter 4 to 7: 32-bit × 1
 (interval timer, event count, toggle output, interrupt, clock source for serial I/F, generation of timer synchronous output timing)
  Clock source ····················· IOCLK; IOCLK/8; IOCLK/32; external clock input; underflow of timer counter
  Interrupt source ············· underflow of timer counter 4, 5, 6, 7

Timer counter 8 to B: 32-bit × 1
 (interval timer, event count, toggle output, interrupt, clock source for serial I/F, generation of timer synchronous output timing)
  Clock source ····················· IOCLK; IOCLK/8; IOCLK/32; external clock input; underflow of timer counter
  Interrupt source ············· underflow of timer counter 8, 9, A, B

*: each of timer counters 0 to 3, 4 to 7, and 8 to B can be changed to an 8-, 16-, or 24-bit timer counter.

Timer counter 10 to 13: 16-bit × 4 (interval timer, event count, toggle output, interrupt, DMA start)
  Clock source ····················· IOCLK; IOCLK/8; IOCLK/32; external clock input;
             underflow of timer counter 0, 1, 2
  Interrupt source ············· underflow of timer counter 10, 11, 12, 13

Timer counter 14, 15: 16-bit × 2
 (interval timer, event count, toggle output, PMW output, interrupt, input capture (2 lines), one-shot output,
 external trigger start, generation of timer synchronous output timing, DMA start)
  Clock source ····················· IOCLK; IOCLK/8; external clock input (2 lines);
             underflow of timer counter 0, 1; 2-phase encode
  Interrupt source ············· overflow of timer 14, 15; underflow of timer 14, 15; coincidence of compare
             register with binary counter or at capture

Watchdog timer: 16- to 25-bit × 1

DMA Controller

Number of channels: 2
Unit of transfer: 8/16/32 bits
Max. Transfer cycles: 65535
Staring factor: external interrupt, timer factor, PNM factor, serial transmission/reception factor,
       A/D conversion finish, software factor
Transfer method: 2-bus cycle transfer
Adressing modes: fixed, increment, decrement
Transfer modes: word transfer, burst transfer, intermittent transfer

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■ **Serial Interface**

Serial 0, 1: 7-, 8-bit × 2 (clock synchronous mode, start-stop synchronous mode, I²C mode)

Serial 2: 7-, 8-bit × 1 (start-stop synchronous mode)

Serial 3 to 7: 7-, 8-bit × 5 (clock synchronous mode)

Clock source ···················· (clock synchronous mode, start-stop synchronous mode)

IOCLK; underflow of timer counter; external clock

(I²C mode)

IOCLK; underflow of timer counter

■ **I/O Pins**	**I/O**	155	• Common use : 137
	Input	16	• Common use : 16

■ **A/D Inputs**   10-bit × 16-ch.

■ **PWM**   12-, 14-bit resolution × 4-ch. (dedicated), 16-bit resolution × 2-ch. (common with timer)

■ **ICR**   28-bit × 13-ch. + 16-bit × 4-ch. (common with timer)

■ **OCR**   16-bit × 4-ch. (common with timer)

■ **Timer Synchronous Output**   4-bit (synchronous output) × 2-ch.

■ **Electrical Characteristics**

Supply current

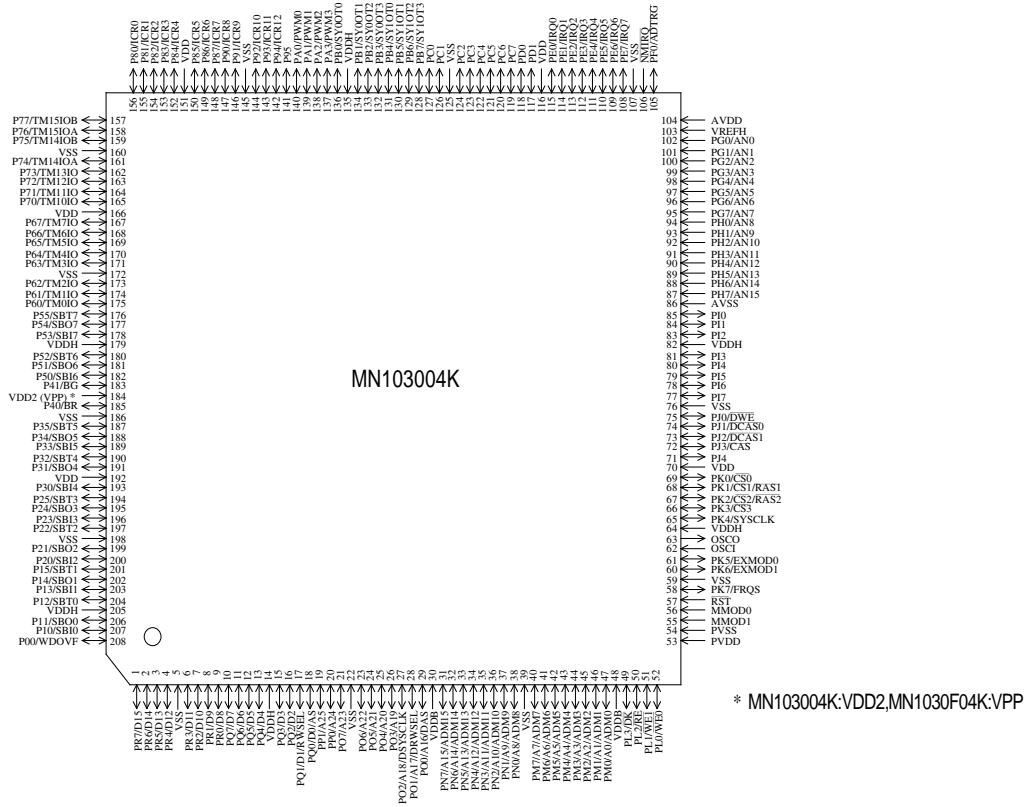| Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	VDDH, VDDB, VDD, PVDD, AVDD = 3.0 V VI = VDDH (VDDB) or VSS At internal = 40 MHz Output open			150	mA
Supply current at stopping	IDD4	VDDH, VDDB, VDD, PVDD, AVDD = 3.6 V VI = VDDH (VDDB) or VSS fosc = oscillation stopped Output open			150*	μA

(Ta = −20°C to +85°C)
*FLGA239-C-1313

A/D conversion performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Resolution					10	Bits
A/D conversion absolute error		VREF+ = 3.0 V A/D conversion clock = 5 MHz			± 7	LSB
A/D conversion relative error					± 5	LSB
A/D conversion time			2.8			μ s

(Ta = −20°C to +85°C, AVDD = 3.0 V, AVSS = 0 V)

See the next page for pin assignment and support tool.

MN103004K

QFP208-P-2828F *Pb free

(QFP208-P-2828A)

* MN103004K:VDD2,MN1030F04K:VPP

Left side pins (157–208):
P77/TM15IOB 157
P76/TM15IOA 158
P75/TM14IOB 159
VSS 160
P74/TM14IOA 161
P73/TM13IO 162
P72/TM12IO 163
P71/TM11IO 164
P70/TM10IO 165
VDD 166
P67/TM7IO 167
P66/TM6IO 168
P65/TM5IO 169
P64/TM4IO 170
P63/TM3IO 171
VSS 172
P62/TM2IO 173
P61/TM1IO 174
P60/TM0IO 175
P55/SBT7 176
P54/SBO7 177
P53/SBI7 178
VDDH 179
P52/SBT6 180
P51/SBO6 181
P50/SBI6 182
P41/BG 183
VDD2 (VPP) * 184
P40/BR 185
VSS 186
P35/SBT5 187
P34/SBO5 188
P33/SBI5 189
P32/SBT4 190
P31/SBO4 191
VSS 192
P30/SBI4 193
P25/SBT3 194
P24/SBO3 195
P23/SBI3 196
P22/SBT2 197
VSS 198
P21/SBO2 199
P20/SBI2 200
P15/SBT1 201
P14/SBO1 202
P13/SBI1 203
P12/SBT0 204
VDDH 205
P11/SBO0 206
P10/SBI0 207
P00/WDOVF 208

Right side pins (104–53):
AVDD 104
VREFH 103
PG0/AN0 102
PG1/AN1 101
PG2/AN2 100
PG3/AN3 99
PG4/AN4 98
PG5/AN5 97
PG6/AN6 96
PG7/AN7 95
PH0/AN8 94
PH1/AN9 93
PH2/AN10 92
PH3/AN11 91
PH4/AN12 90
PH5/AN13 89
PH6/AN14 88
PH7/AN15 87
AVSS 86
PI0 85
PI1 84
PI2 83
VDDH 82
PI3 81
PI4 80
PI5 79
PI6 78
PI7 77
VSS 76
PJ0/DWE 75
PJ1/DCAS0 74
PJ2/DCAS1 73
PJ3/CAS 72
PJ4 71
VDD 70
PK0/CS0 69
PK1/CS1/RAS1 68
PK2/CS2/RAS2 67
PK3/CS3 66
PK4/SYSCLK 65
VDDH 64
OSCO 63
OSCI 62
PK5/EXMOD0 61
PK6/EXMOD1 60
VSS 59
PK7/FRQS 58
RST 57
MMOD0 56
MMOD1 55
PVSS 54
PVDD 53

Top side pins:
P80/ICR0, P81/ICR1, P82/ICR2, P83/ICR3, P84/ICR4, VDD, P85/ICR5, P86/ICR6, P87/ICR7, P90/ICR8, P91/ICR9, P92/ICR10, P93/ICR11, P94/ICR12, P95, PA0/PWM0, PA1/PWM1, PA2/PWM2, PA3/PWM3, PB0/SYO0T0, VDDH, PB1/SYO0T1, PB2/SYO0T2, PB3/SYO0T3, PB4/SYO1T0, PB5/SYO1T1, PB6/SYO1T2, PB7/SYO1T3, PC0, PC1, VSS, PC2, PC3, PC4, PC5, PC6, PC7, PD0, PD1, VDD, PE0/IRQ0, PE1/IRQ1, PE2/IRQ2, PE3/IRQ3, PE4/IRQ4, PE5/IRQ5, PE6/IRQ6, PE7/IRQ7, VSS, NMIRQ, PF0/ADTRG
(pins 156–105)

Bottom side pins (1–52):
PR7/D15, PR6/D14, PR5/D13, PR4/D12, VSS, PR3/D11, PR2/D10, PR1/D9, PR0/D8, PQ7/D7, PQ6/D6, PQ5/D5, PQ4/D4, VDDH, PQ3/D3, PQ2/D2, PQ1/D1/RWEH, PQ0/D0/AS, PP1/A23, PP0/A24, PO7/A25, VSS, PO6/A22, PO5/A21, PO4/A20, PO3/A19, PO2/A18/DSYSCLK, PO1/A17/DRWSEL, PO0/A16/DAS, VDDB, PN7/A15/ADM15, PN6/A14/ADM14, PN5/A13/ADM13, PN4/A12/ADM12, PN3/A11/ADM11, PN2/A10/ADM10, PN1/A9/ADM9, PN0/A8/ADM8, VDD, PM7/A7/ADM7, PM6/A6/ADM6, PM5/A5/ADM5, PM4/A4/ADM4, PM3/A3/ADM3, PM2/A2/ADM2, PM1/A1/ADM1, PM0/A0/ADM0, VDDB, PL3/DK, PL2/RE, PL1/WEL, PL0/WEH

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Pin Assignment (Continue)

Perspective

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
T	N.D.	N.D.	PE7, IRQ7	$\overline{NMIRQ}$	PE1, IRQ1	PD0	PC4	PC1	PB1, SY0OT1	PA2, PWM2	P94, ICR12	P91, ICR9	P84, ICR4	P80, ICR0	N.D.	N.D.
R	N.D.	N.D.	N.D.	PE5, IRQ5	PE3, IRQ3	VDD	PC2	PB7, SY1OT3	PB3, SY0OT3	PA0, PWM0	P92, ICR10	P85, ICR5	P82, ICR2	N.D.	N.D.	N.D.
P	AVDD	N.D.	PF0, $\overline{ADTRG}$	VSS	PE4, IRQ4	PC6	PC5	VSS	PB5, SY1OT1	PB0, SY0OT0	VSS	VDD	P87, ICR7	P77, TM15IOB	N.D.	P76, TM15IOA
N	PG2, AN2	PG0, AN0	VREFH	PE6, IRQ6	PE2, IRQ2	PD1	PC3	PB6, SY1OT2	VDDH	PA1, PWM1	P90, ICR8	P83, ICR3	P74, TM14IOA	P75, TM14IOB	P73, TM13IO	VSS
M	PG3, AN3	PG5, AN5	PG1, AN1	PG4, AN4	PE0, IRQ0	PC7	PC0	PB2, SY0OT2	PA3, PWM3	P95	P86, ICR6	P81, ICR1	P70, TM10IO	P72, TM12IO	VDD	P71, TM11IO
L	PG7, AN7	PH1, AN9	PH2, AN10	PG6, AN6	PH3, AN11	PH0, AN8	PB4, SY1OT0	N.D.	N.D.	P93, ICR11	P67, TM7IO	P63, TM3IO	P65, TM5IO	VSS	P66, TM6IO	P64, TM4IO
K	PH7, AN15	PH5, AN13	PH6, AN14	AVSS	PI0	PH4, AN12	N.D.	N.D.	N.D.	N.D.	P60, TM0IO	P54, SBO7	P62, TM2IO	P55, SBT7	P61, TM1IO	P53, SBI7
J	PI2	PI3	PI4	VDDH	PI1	N.D.	N.D.	N.D.	N.D.	N.D.	P41, $\overline{BG}$	VDDH	P51, SBO6	P52, SBT6	P50, SBI6	
H	PJ0, $\overline{DWE}$	PI7	VSS	PI5	PI6	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	P35, SBT5	P34, SBO5	P40, $\overline{BR}$	VDD2 (VPP)	VSS
G	PK2, $\overline{CS2}$, $\overline{RAS2}$	PK0, $\overline{CS0}$	PK1, $\overline{CS1}$, $\overline{RAS1}$	VDD	PJ4	PJ2, $\overline{DCAS1}$	N.D.	N.D.	N.D.	N.D.	P31, SBO4	P33, SBI5	P30, SBI4	P32, SBT4	VDD	P25, SBT3
F	OSCO	PK4, SYSCLK	VDDH	PK3, $\overline{CS3}$	PJ3, $\overline{CAS}$	PJ1, $\overline{DCAS0}$	PN5, A13, ADM13	N.D.	N.D.	PO5, A21	P24, SBO3	P21, SBO2	P22, SBT2	P15, SBT1	P23, SBI3	VSS
E	OSCI	VSS	PK7, FRQS	PK6, EXMOD1	PK5, EXMOD0	PN1, A9, ADM9	PN3, A11, ADM11	PO0, A16, DAS	PO2, A18, DSYSCLK	PP0, A24	PQ2, D2	PR1, D9	P13, SBI1	P20, SBI2	P14, SBO1	P12, SBT0
D	MMOD1	$\overline{RST}$	MMOD0	PVSS	PM4, A4, ADM4	PN0, A8, ADM8	PN4, A12, ADM12	PO7, A23	PO3, A19	PQ0, D0, AS	PQ5, D5	PQ7, D7	P10, SBI0	VDDH	P11, SBO0	P00, WDOVF
C	PVDD	N.D.	PL1, $\overline{WE1}$	PL3, $\overline{DK}$	PM2, A2, ADM2	PM6, A6, ADM6	VSS	PN7, A15, ADM15	VSS	PQ3, D3	VDDH	PR3, D11	PR4, D12	PR6, D14	N.D.	
B	N.D.	N.D.	PL2, $\overline{RE}$	PM0, A0, ADM0	PM1, A1, ADM1	PM5, A5, ADM5	PN6, A14, ADM14	VDDB	PO6, A22	PP1, A25	PQ6, D6	PR0, D8	PR5, D13		N.D.	N.D.
A	N.D.	N.D.	PL0, $\overline{WE0}$	VDDB	PM3, A3, ADM3	PM7, A7, ADM7	PN2, A10, ADM10	PO1, A17, DRWSEL	PO4, A20	PQ1, D1, RWSEL	PQ4, D4	PR2, D10	VSS	PR7, D15	N.D.	N.D.

FLGA239-C-1313

* C1 has no electrode (pin).

* N.D. has an electrode (pin) but N.C. is not guaranteed. Please design so as not to cause short circuit with other wiring on the user board.

* Each of VDD, VDDB, VDDH and VSS has multiple electrodes (pins). Pins having the same name are internally shorted.

*H2: MN103004K (VDD2), MN103016K (VDD2), MN1030F04K (VPP)

Support Tool

In-circuit Emulator	PX-ICE103004-QFP208-P-2828A	Not applicable to FLGA239-C-1313.
On-board Development Tools	PX-ODB103S-O CSIDE-MN10300 (Computex Co., Ltd, product)	

Flash Memory Built-in Type

Type	MN1030F04K
Command ROM ($\times$ 64-bit)	256 K-byte
Data RAM ($\times$ 32-bit)	12 K-byte
Minimum instruction execution time	25 ns (at 3.0 V to 3.6 V, 40 MHz)
Package	QFP208-P-2828F [*Pb free], FLGA239-C-1313
(Old Package)	(QFP208-P-2828A)