Bipolar Power Transistors

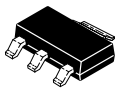
NPN Silicon

- Collector –Emitter Sustaining Voltage — $V_{CEO(sus)}$
  = 30 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain — h_{FE}
  = 85 (Min) @ I_C = 0.8 Adc
  = 60 (Min) @ I_C = 3.0 Adc
- Low Collector –Emitter Saturation Voltage — $V_{CE(sat)}$
  = 0.2 Vdc (Max) @ I_C = 1.2 Adc
  = 0.45 Vdc (Max) @ I_C = 3.0 Adc
- SOT–223 Surface Mount Packaging

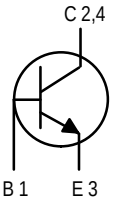
MMJT9410

Motorola Preferred Device

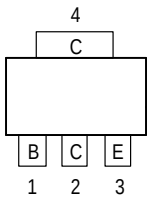
POWER BJT
I_C = 3.0 AMPERES
BV_{CEO} = 30 VOLTS
$V_{CE(sat)}$ = 0.2 VOLTS



CASE 318E–04, Style 1



Schematic



Top View Pinout

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CB}	45	Vdc
Emitter–Base Voltage	V_{EB}	± 6.0	Vdc
Base Current — Continuous	I_B	1.0	Adc
Collector Current — Continuous — Peak	I_C	3.0 5.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total P_D @ T_A = 25°C mounted on 1” sq. (645 sq. mm) Collector pad on FR–4 bd material Total P_D @ T_A = 25°C mounted on 0.012” sq. (7.6 sq. mm) Collector pad on FR–4 bd material	P_D	3.0 24 1.7 0.75	Watts mW/°C Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction to Case – Junction to Ambient on 1” sq. (645 sq. mm) Collector pad on FR–4 bd material – Junction to Ambient on 0.012” sq. (7.6 sq. mm) Collector pad on FR–4 bd material	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	42 75 165	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8” from case for 5 seconds	T_L	260	°C

This document contains information on a new product. Specifications and information are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0 Adc)	$V_{CEO(sus)}$	30	—	—	Vdc
Emitter–Base Voltage (I_E = 50 μAdc, I_C = 0 Adc)	V_{EBO}	6.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 25 Vdc, R_{BE} = 200 Ω)	I_{CER}	—	—	20	μAdc
(V_{CE} = 25 Vdc, R_{BE} = 200 Ω, T_J = 125°C)		—	—	200	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc)	I_{EBO}	—	—	10	μAdc
ON CHARACTERISTICS(1)					
Collector–Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 20 mAdc)	$V_{CE(sat)}$	—	0.105	0.150	Vdc
(I_C = 1.2 Adc, I_B = 20 mAdc)		—	0.150	0.200	
(I_C = 3.0 Adc, I_B = 0.3 Adc)		—	—	0.450	
Base–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{BE(sat)}$	—	—	1.25	Vdc
Base–Emitter On Voltage (I_C = 1.2 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	—	1.10	Vdc
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	85	200	—	—
(I_C = 1.2 Adc, V_{CE} = 1.0 Vdc)		80	—	—	
(I_C = 3.0 Adc, V_{CE} = 1.0 Vdc)		60	—	—	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0 Adc, f = 1.0 MHz)	C_{ob}	—	85	135	pF
Input Capacitance (V_{EB} = 8.0 Vdc)	C_{ib}	—	200	—	pF
Current–Gain — Bandwidth Product(2) (I_C = 500 mA, V_{CE} = 10 Vdc, F_{test} = 1.0 MHz)	f_T	—	72	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) $f_T = |h_{FE}| \cdot f_{test}$

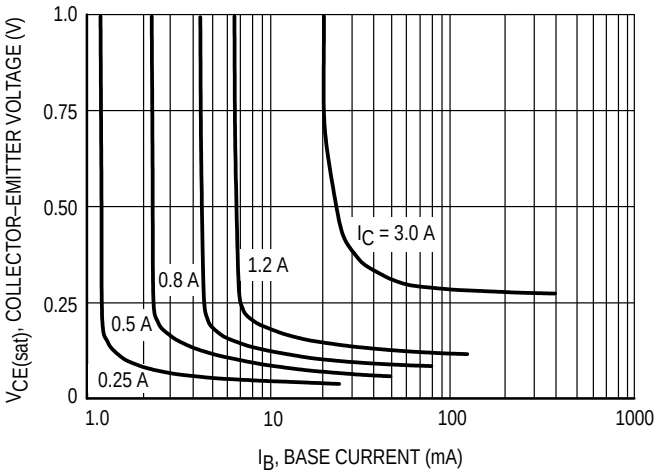


Figure 1. Collector Saturation Region

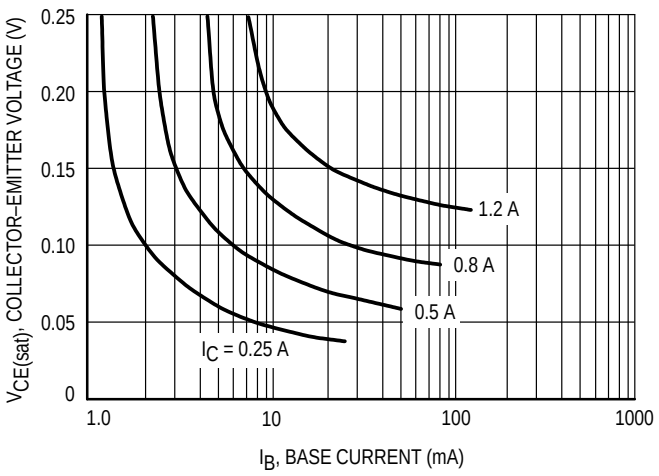


Figure 2. Collector Saturation Region

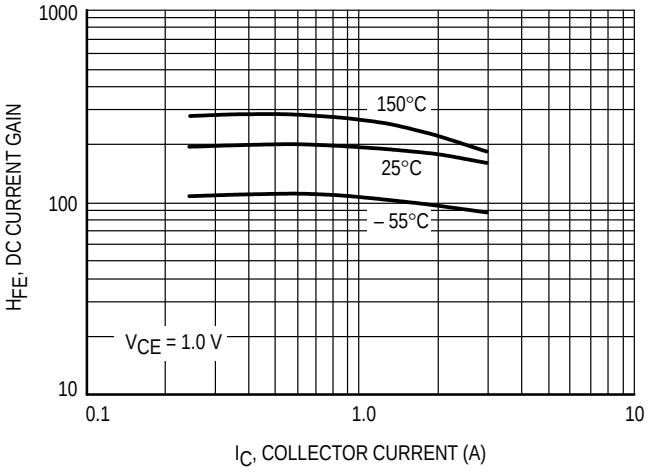


Figure 3. DC Current Gain

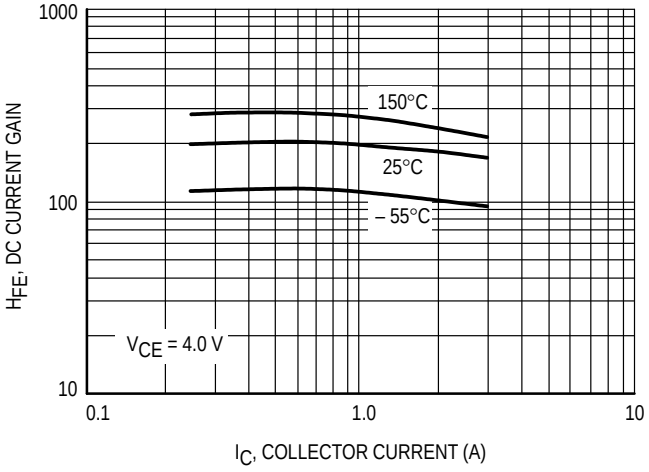


Figure 4. DC Current Gain

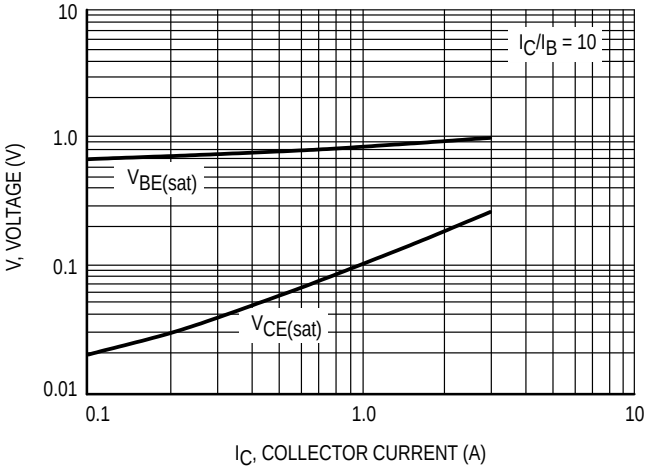


Figure 5. “On” Voltages

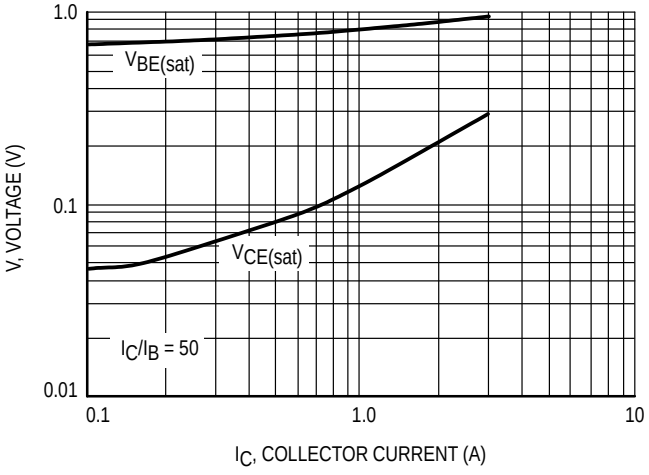


Figure 6. “On” Voltages

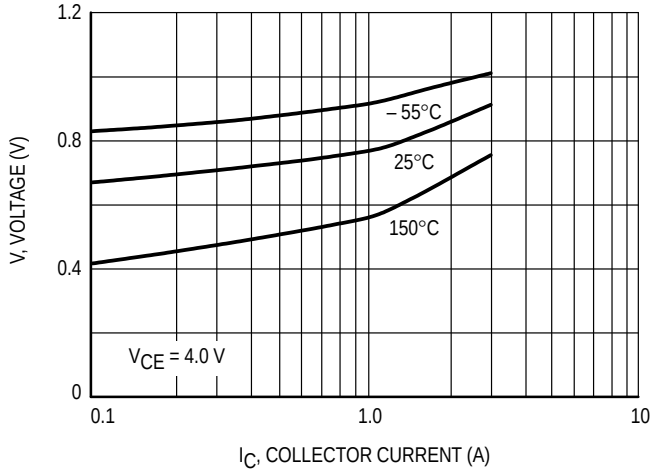


Figure 7. $V_{BE(on)}$ Voltage

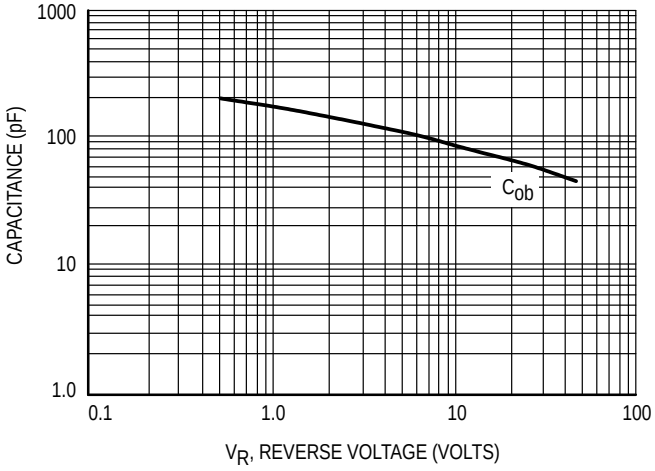


Figure 8. Capacitance

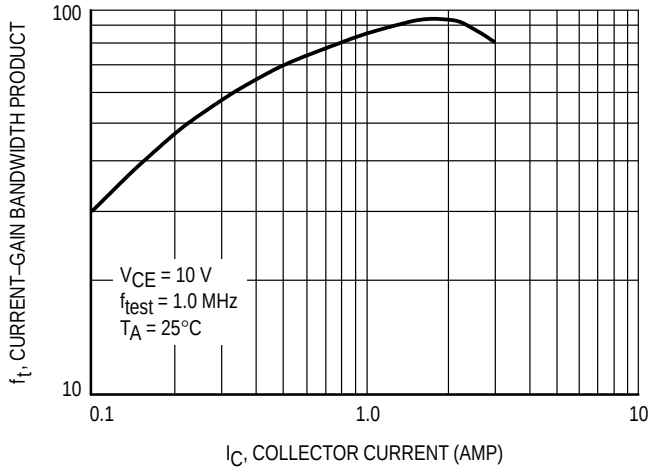


Figure 9. Current–Gain Bandwidth Product

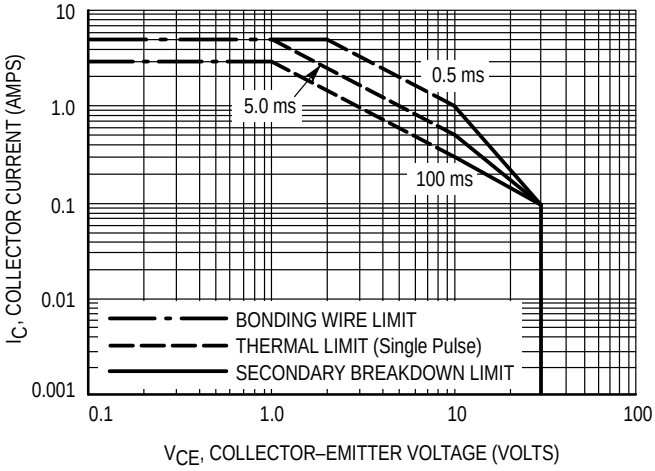


Figure 10. Active Region Safe Operating Area

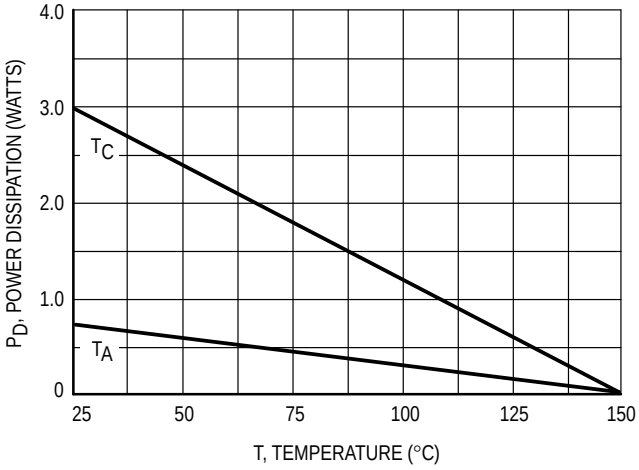


Figure 11. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

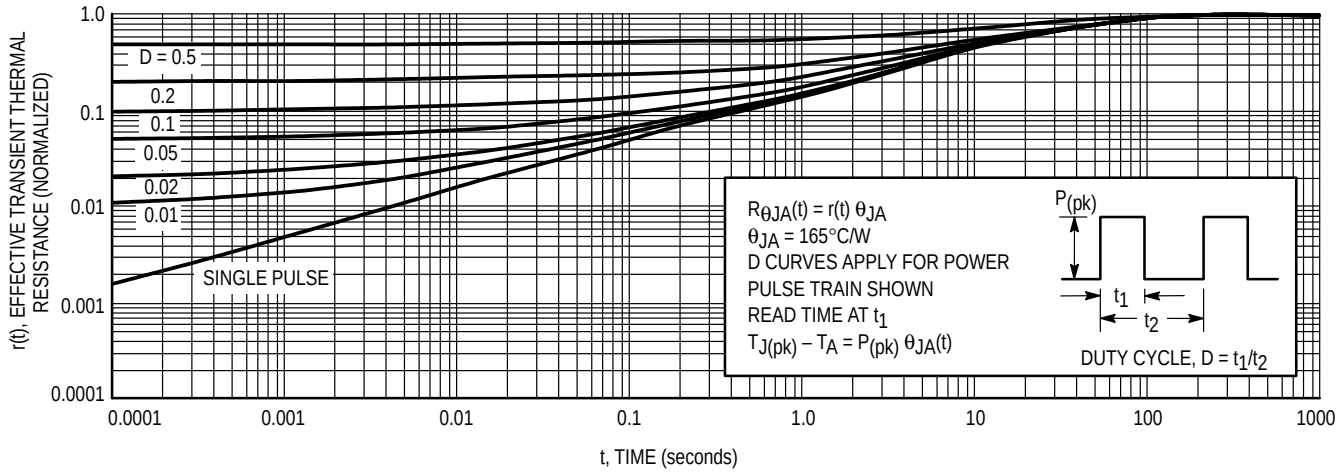
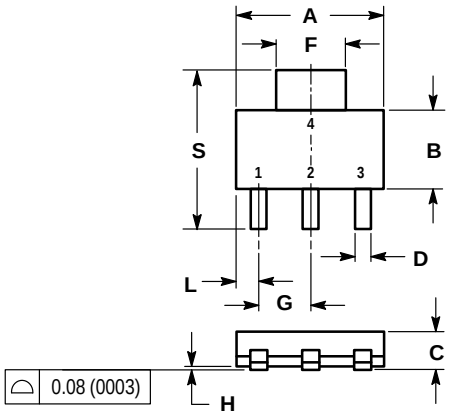
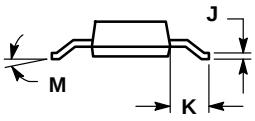


Figure 12. Thermal Response

PACKAGE DIMENSIONS



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0 °	10 °	0 °	10 °
S	0.264	0.287	6.70	7.30

CASE 318E–04
ISSUE H

How to reach us:
USA / EUROPE / Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 303–675–2140 or 1–800–441–2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
– US & Canada ONLY 1–800–774–1848

INTERNET: http://www.mot.com/SPS/

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 81–3–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298