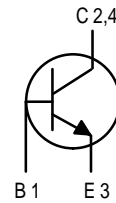


Bipolar Power Transistors

NPN Silicon

- Collector–Emitter Sustaining Voltage — $V_{CEO(sus)}$
= 30 Vdc (Min) @ $I_C = 10$ mAdc
- High DC Current Gain — h_{FE}
= 85 (Min) @ $I_C = 0.8$ Adc
= 60 (Min) @ $I_C = 3.0$ Adc
- Low Collector–Emitter Saturation Voltage — $V_{CE(sat)}$
= 0.2 Vdc (Max) @ $I_C = 1.2$ Adc
= 0.45 Vdc (Max) @ $I_C = 3.0$ Adc
- SOT–223 Surface Mount Packaging

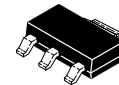


Schematic

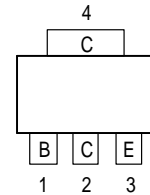
MMJT9410

Motorola Preferred Device

POWER BJT
 $I_C = 3.0$ AMPERES
 $V_{CEO} = 30$ VOLTS
 $V_{CE(sat)} = 0.2$ VOLTS



CASE 318E–04, Style 1



Top View Pinout

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CB}	45	Vdc
Emitter–Base Voltage	V_{EB}	± 6.0	Vdc
Base Current — Continuous	I_B	1.0	Adc
Collector Current — Continuous — Peak	I_C	3.0 5.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C Total P_D @ $T_A = 25^\circ\text{C}$ mounted on 1" sq. (645 sq. mm) Collector pad on FR–4 bd material Total P_D @ $T_A = 25^\circ\text{C}$ mounted on 0.012" sq. (7.6 sq. mm) Collector pad on FR–4 bd material	P_D	3.0 24 1.7 0.75	Watts mW/ $^\circ\text{C}$ Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to $+150$	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction to Case – Junction to Ambient on 1" sq. (645 sq. mm) Collector pad on FR–4 bd material – Junction to Ambient on 0.012" sq. (7.6 sq. mm) Collector pad on FR–4 bd material	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	42 75 165	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	260	$^\circ\text{C}$

This document contains information on a new product. Specifications and information are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I _C = 10 mA _{dc} , I _B = 0 A _{dc})	V _{CEO(sus)}	30	—	—	V _{dc}
Emitter–Base Voltage (I _E = 50 μA _{dc} , I _C = 0 A _{dc})	V _{EBO}	6.0	—	—	V _{dc}
Collector Cutoff Current (V _{CE} = 25 V _{dc} , R _{BE} = 200 Ω) (V _{CE} = 25 V _{dc} , R _{BE} = 200 Ω, T _J = 125°C)	I _{CER}	—	—	20 200	μA _{dc}
Emitter Cutoff Current (V _{BE} = 5.0 V _{dc})	I _{EBO}	—	—	10	μA _{dc}

ON CHARACTERISTICS(1)

Collector–Emitter Saturation Voltage (I _C = 0.8 A _{dc} , I _B = 20 mA _{dc}) (I _C = 1.2 A _{dc} , I _B = 20 mA _{dc}) (I _C = 3.0 A _{dc} , I _B = 0.3 A _{dc})	V _{CE(sat)}	—	0.105 0.150 —	0.150 0.200 0.450	V _{dc}
Base–Emitter Saturation Voltage (I _C = 3.0 A _{dc} , I _B = 0.3 A _{dc})	V _{BE(sat)}	—	—	1.25	V _{dc}
Base–Emitter On Voltage (I _C = 1.2 A _{dc} , V _{CE} = 4.0 V _{dc})	V _{BE(on)}	—	—	1.10	V _{dc}
DC Current Gain (I _C = 0.8 A _{dc} , V _{CE} = 1.0 V _{dc}) (I _C = 1.2 A _{dc} , V _{CE} = 1.0 V _{dc}) (I _C = 3.0 A _{dc} , V _{CE} = 1.0 V _{dc})	h _{FE}	85 80 60	200 — —	— — —	—

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 V _{dc} , I _E = 0 A _{dc} , f = 1.0 MHz)	C _{ob}	—	85	135	pF
Input Capacitance (V _{EB} = 8.0 V _{dc})	C _{ib}	—	200	—	pF
Current–Gain — Bandwidth Product(2) (I _C = 500 mA, V _{CE} = 10 V _{dc} , F _{test} = 1.0 MHz)	f _T	—	72	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) f_T = |h_{FE}| • f_{test}

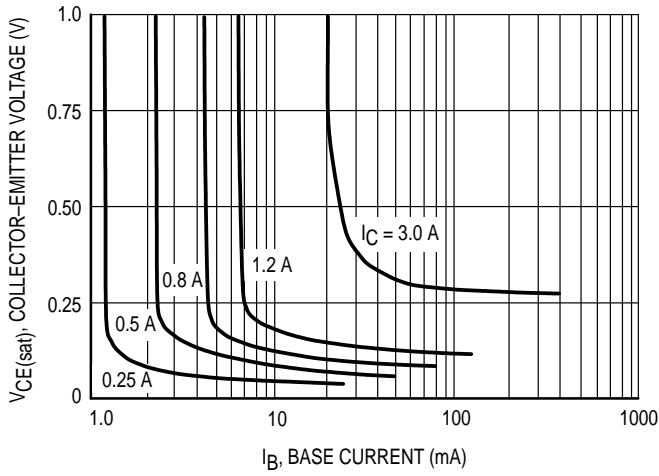


Figure 1. Collector Saturation Region

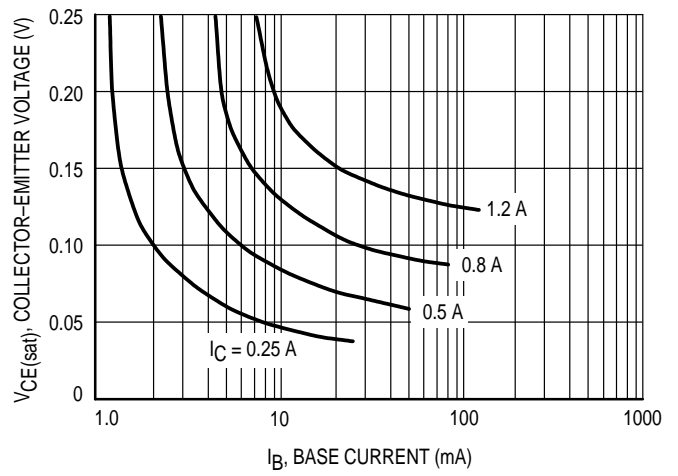


Figure 2. Collector Saturation Region

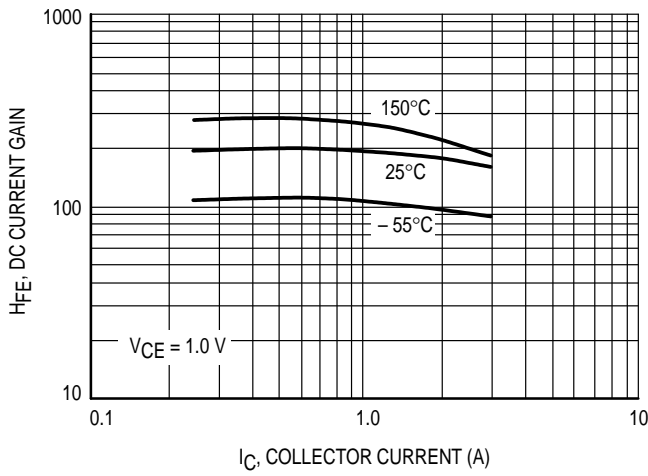


Figure 3. DC Current Gain

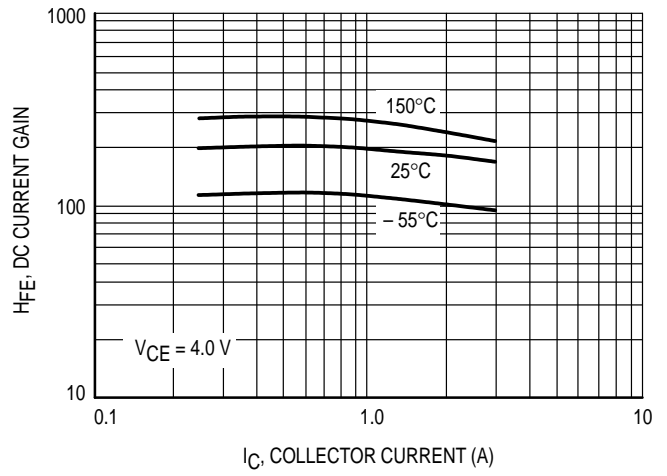


Figure 4. DC Current Gain

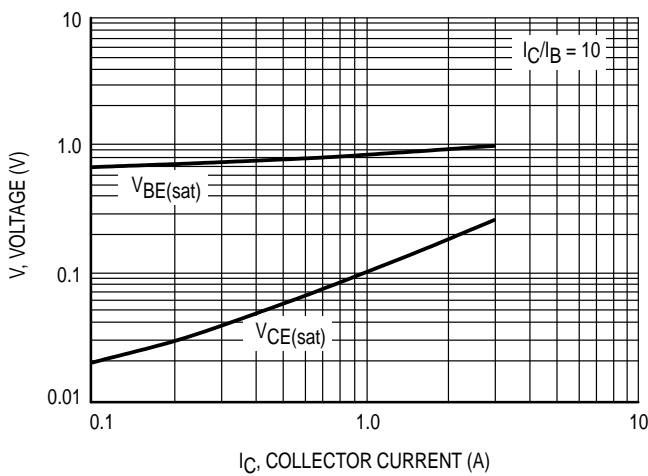


Figure 5. "On" Voltages

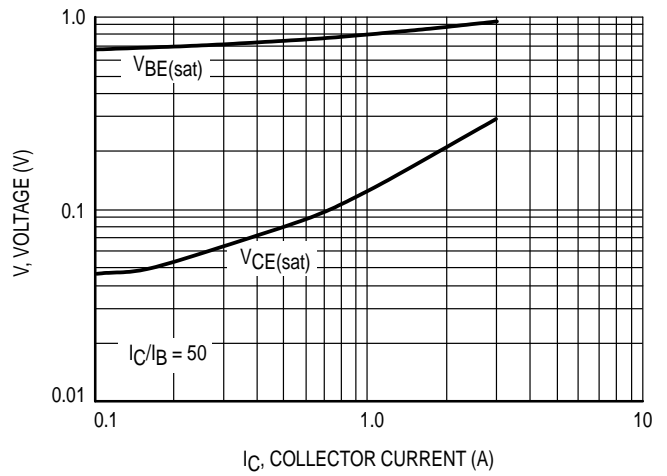


Figure 6. "On" Voltages

MMJT9410

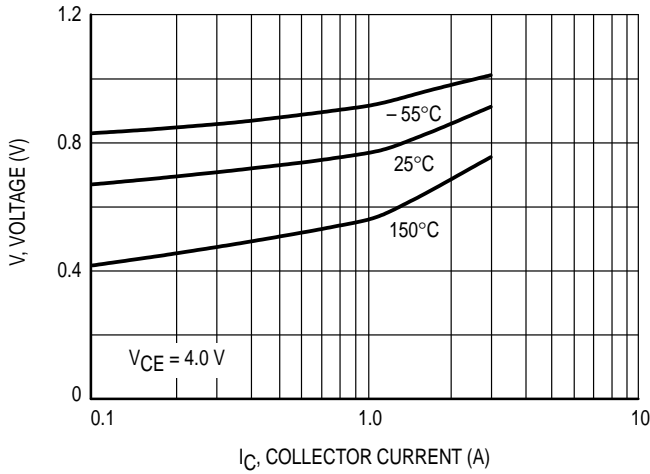


Figure 7. $V_{BE(on)}$ Voltage

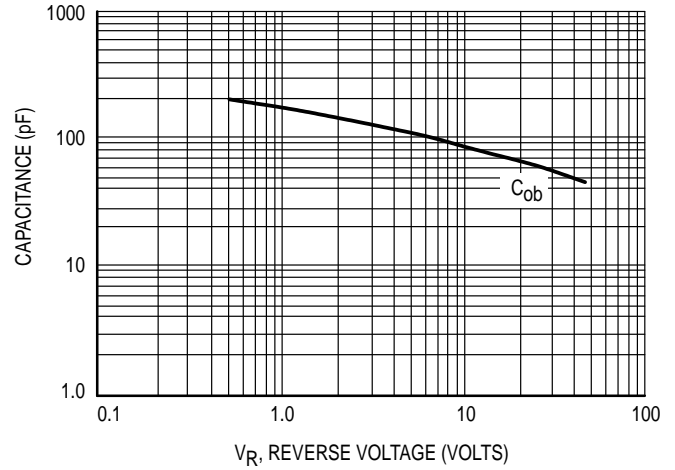


Figure 8. Capacitance

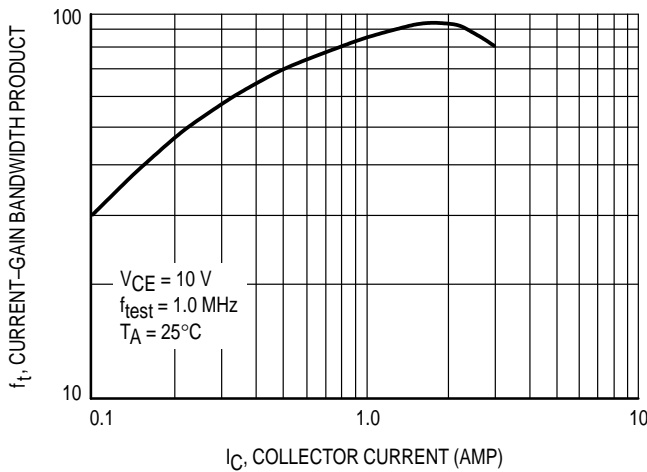


Figure 9. Current-Gain Bandwidth Product

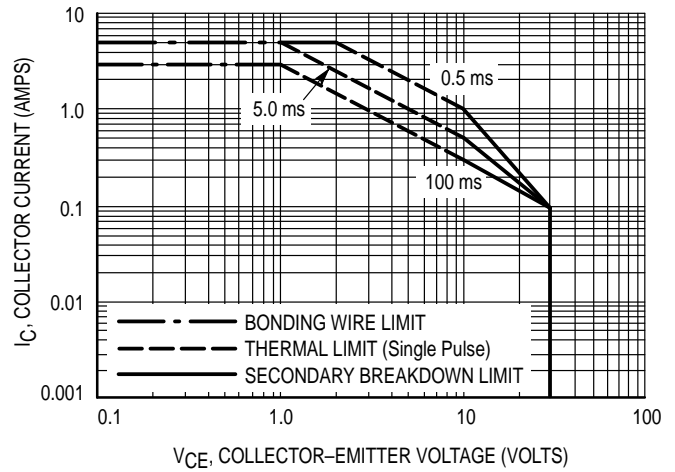


Figure 10. Active Region Safe Operating Area

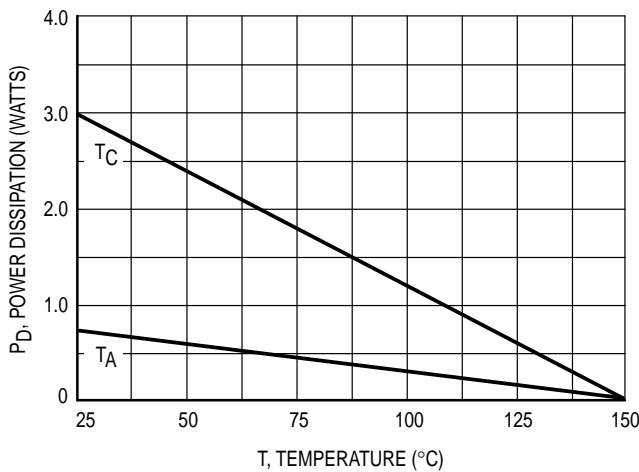


Figure 11. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

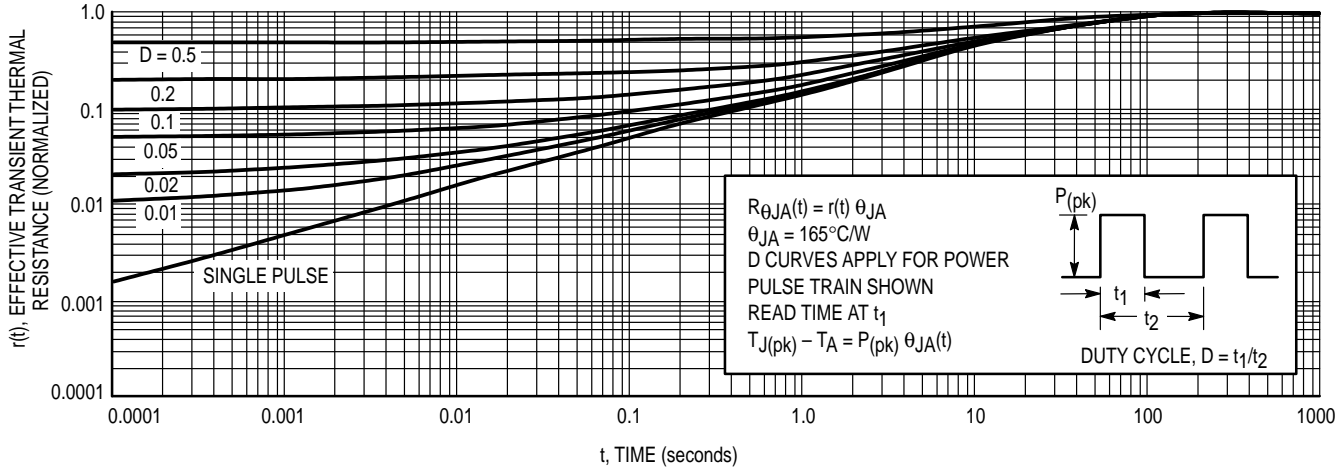
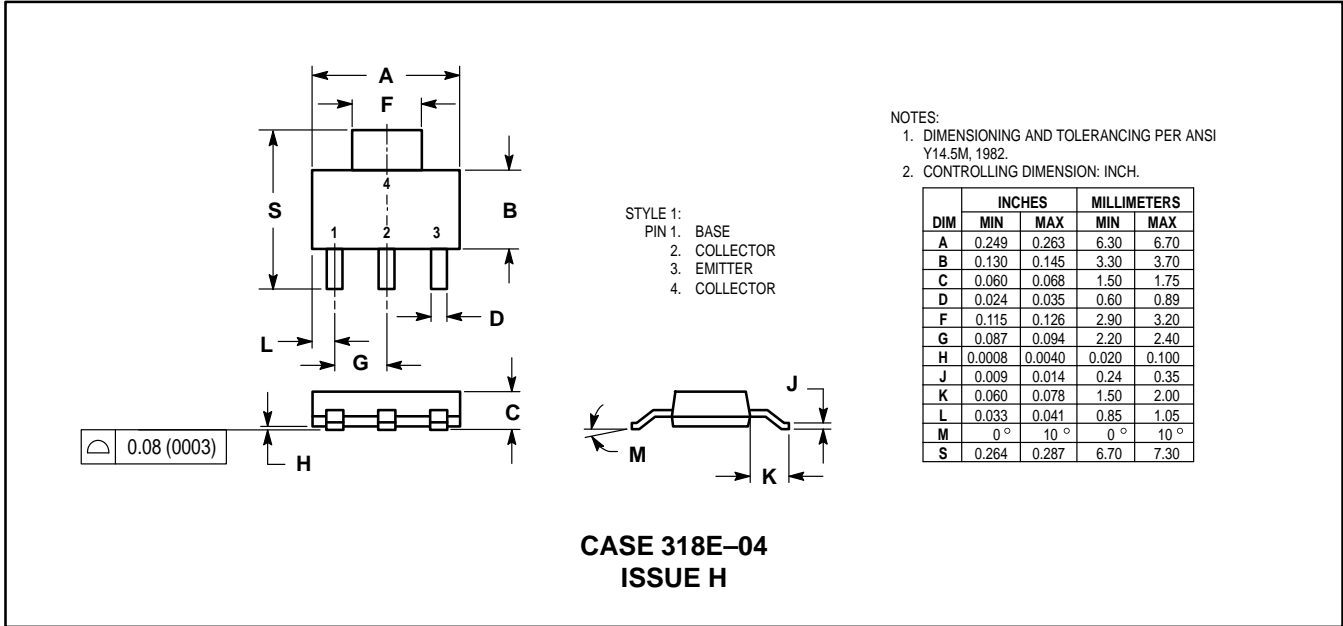


Figure 12. Thermal Response

PACKAGE DIMENSIONS



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