



DUAL J-K MASTER SLAVE FLIP-FLOP

GENERAL DESCRIPTION

The MMC 4027 is a monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package.

The MMC 4027 is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset and Clock input signals. Buffered Q and \bar{Q} signals are provided as outputs. This input-output arrangement provides for compatible operation with the MMC 4013 dual D-type flip-flop.

The MMC 4027 is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

FEATURES

- Set-Reset capability
- Static flip-flop operation-retains state indefinitely with clock level either „high“ or „low“
- Medium speed operation-16 MHz (typ.) clock toggle rate at 10 V
- 100% tested for quiescent current

APPLICATIONS

- Registers, counters, control circuits

ABSOLUTE MAXIMUM RATINGS

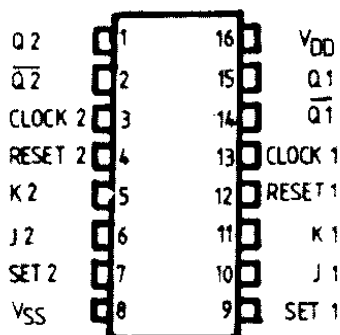
V_{DD}^*	Supply voltage: G and H types E and F types	-0.5 to -0.5 to	20 18	V V
V_i	Input voltage	-0.5 to	$V_{DD}+0.5$	V
I_i	DC input current (any one input)		± 10	mA
P_{tot}	Total power dissipation (per package) Dissipation per output transistor for T_A - full package-temperature range		200	mW
T_A	Operating temperature G and H types E and F types	-55 to -40 to	125 85	C C
T_{stg}	Storage temperature	-65 to	150	C

* All voltage values are referred to V_{SS} pin voltage

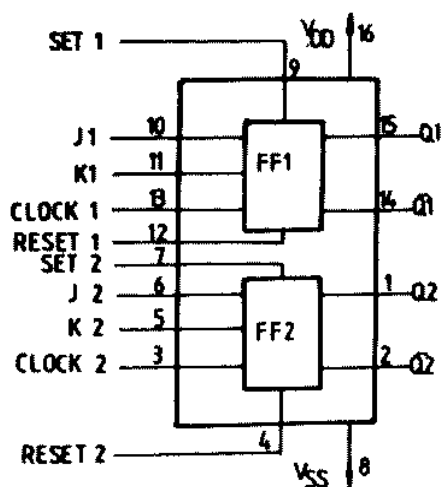
RECOMMENDED OPERATING CONDITIONS

V_{DD}^*	Supply voltage: G and H types E and F types	3 to 3 to	18 15	V V
V_i	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature G and H types E and F types	-55 to -40 to	125 85	C C

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

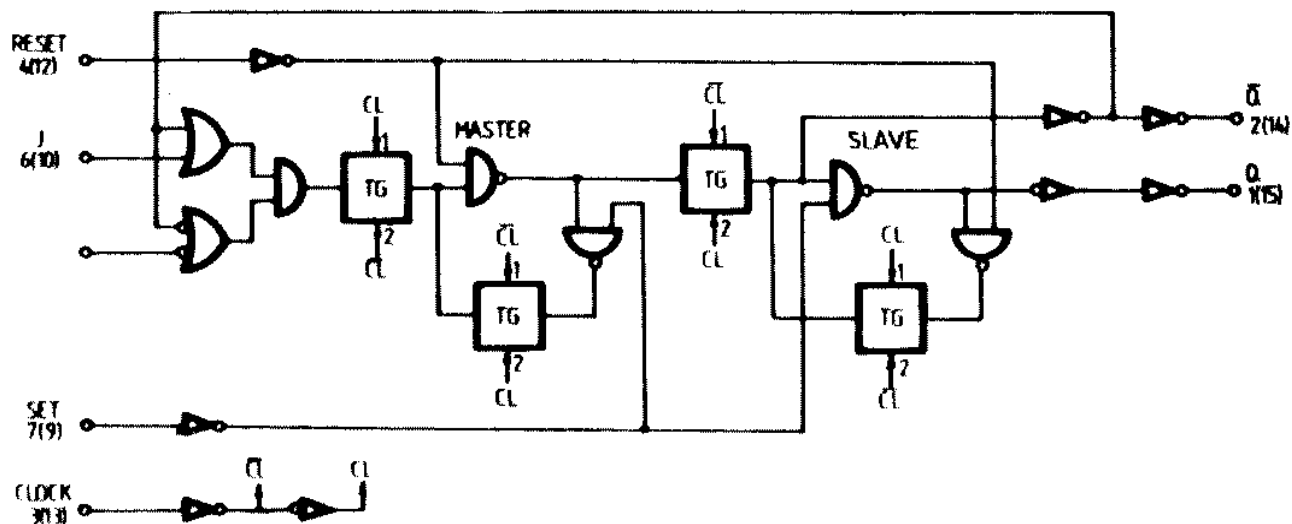


TRUTH TABLE

PRESENT STATE					CL [●]	NEXT STATE OUTPUTS	
J	K	S	R	Q		Q	Q
1	X	0	0	0		1	0
X	0	0	0	1		1	0
0	X	0	0	0		0	1
X	1	0	0	1		0	1
X	X	0	0	X	X	NO CHANGE	
X	X	1	0	X		1	0
X	X	0	1	X		0	1
X	X	1	1	X		1	1

● Level change
x Don't care

LOGIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS				VALUES						UNIT		
		V _I (V)	V _O (V)	I _O (μ A)	V _{DD} (V)	T _{LOW}		25°C			T _{HIGH}			
						min.	max.	min.	typ	max.	min.		max.	
I _L	Quiescent current	G, H types	0/5			5		1		0.02	1		30	μ A
			0/10			10		2		0.02	2		60	
0/15					15		4		0.02	4		120		
0/20					20		20		0.04	20		600		
E, F types	0/5			5		4		0.02	4		30			
	0/10			10		8		0.02	8		60			
	0/15			15		16		0.02	16		120			
V _{OH}	Output high voltage												V	
		0/5		< 1	5	4.95		4.95			4.95			
		0/10		< 1	10	9.95		9.95			9.95			
		0/15		< 1	15	14.95		14.95			14.95			
V _{OL}	Output low voltage												V	
		5/0		< 1	5		0.05			0.05		0.05		
		10/0		< 1	10		0.05			0.05		0.05		
		15/0		< 1	15		0.05			0.05		0.05		
V _{IH}	Input high voltage												V	
			0.5/4.5	< 1	5	3.5		3.5			3.5			
			1/9	< 1	10	7		7			7			
			1.5/13.5	< 1	15	11		11			11			
V _{IL}	Input low voltage												V	
			4.5/0.5	< 1	5		1.5			1.5		1.5		
			9/1	< 1	10		3			3		3		
			13.5/1.5	< 1	15		4			4		4		
I _{OH}	Output drive current	G, H types	0/5	2.5		5	-2		-1.6	-3.2		-1.15	mA	
			0/5	4.6		5	-0.64		-0.51	-1		-0.36		
0/10			9.5		10	-1.6		-1.3	-2.6		-0.9			
0/15			13.5		15	-4.2		-3.4	-6.8		-2.4			
E, F types		0/5	2.5		5	-1.53		-1.36	-3.2		-1.1			
		0/5	4.6		5	-0.52		-0.44	-1		-0.36			
		0/10	9.5		10	-1.3		-1.1	-2.6		-0.9			
		0/15	13.5		15	-3.6		-3.0	-6.8		-2.4			
I _{OL}	Output sink current	G, H types	0/5	0.4		5	0.64		0.51	1		0.36	mA	
			0/10	0.5		10	1.6		1.3	2.6		0.9		
0/15			1.5		15	4.2		3.4	6.8		2.4			
E, F types		0/5	0.4		5	0.52		0.44	1		0.36			
		0/10	0.5		10	1.3		1.1	2.6		0.9			
		0/15	1.5		15	3.6		3.0	6.8		2.4			
I _{IH} , I _{IL}	Input leakage current	G, H types	0/18	Any input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μ A
		E, F types	0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1	
C _i	Input capacitance			Any input						5	7.5		pF	

* T_{LOW} = -55°C for G, H devices; -40°C for E, F devices.* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V2 V min. with V_{DD} = 10 V2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$, typical temperature coefficient for all V_{DD} values is $0.3\%/^\circ\text{C}$, all input rise and fall times = 20 ns)

PARAMETER			TEST CONDITIONS	VALUES			UNIT
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation delay time	Clock to \overline{Q} or \overline{Q} outputs	5		150	300	ns
			10		65	130	
			15		45	190	
t_{PLH}	Propagation delay time	Set to \overline{Q} or Reset to \overline{Q}	5		150	300	
			10		65	130	
			15		45	90	
t_{PHL}	Propagation delay time	Set to \overline{Q} or Reset to \overline{Q}	5		200	400	ns
			10		85	170	
			15		60	120	
t_{THL} t_{TLH}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	
t_W	Pulse width	Clock	5	140	70		
			10	60	30		
			15	40	20		
t_W	Pulse width	Set or Reset	5	180	90		ns
			10	80	40		
			15	50	25		
t_{rp} t_f	Clock input rise or fall time		5			15	ns
			10			4	
			15			1	
t_{setup}	Setup time	Data	5	200	100		ns
			10	75	35		
			15	50	25		
f_{max}	Maximum clock input frequency*	Toggle mode	5	3.5	7		MHz
			10	8	16		
			15	12	24		

* Input t_r , $t_f = 5\text{ ns}$