Ordering number:ENN3540

CMOS IC

LC5738

4-Bit Single Chip Microcontroller with LCD Drivers for Low-Voltage, Low Power Use

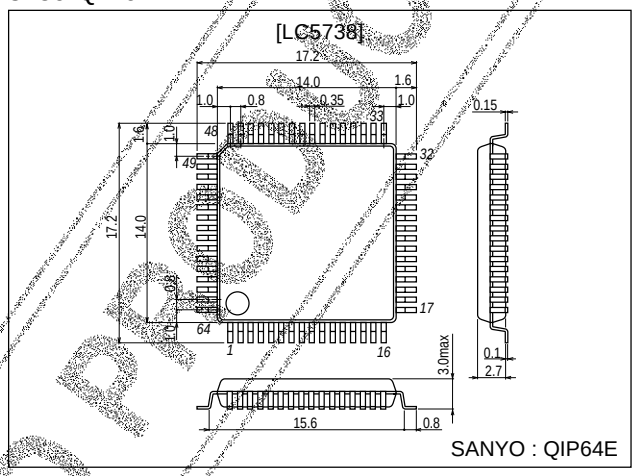
Overview

The LC5738 is a single-chip 4-bit microcontroller with LCD drivers. The features of the LC5738 include low voltage operation, low power dissipation, etc. The HALT function, which can be used to stop/start the CPU operations, facilitates the low power dissipation of the system. The LC5738 is ideally suited for use in melody function-provided timepiece/timer, game, functional watch and calculator application.

Package Dimensions

unit:mm

3159-QIP64E



Hardware Features

- ROM ..... 4096×8bits
- RAM ..... 40×4bits
- Cycle time

Cycle time	System clock source	Oscillation frequency	Operating voltage range	Remarks
122µs	X'tal oscillation / RC oscillation	32.768kHz	1.30 to 1.65V	Ag battery version
122µs	X'tal oscillation	32.768kHz	2.60 to 3.60V	Li battery version
122µs	X'tal oscillation / RC oscillation	32.768kHz	2.00 to 3.60V	EXT-V version

- Current drain

a. Basic system operation mode

Current drain	System clock source	Oscillation frequency	Operating voltage range	Remarks
2.5µA typ.	X'tal oscillation	32.768kHz	1.55V	Ag battery version
10µA typ.	RC oscillation			
2.0µA typ.	X'tal oscillation	32.768kHz	2.90V	Li battery version
6.0µA typ.	X'tal oscillation	32.768kHz	2.90V	EXT-V version
50µA typ.	RC oscillation			

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b. HALT operation mode

Current drain	System clock source	Oscillation frequency	Operating voltage range	Remarks
1.0μA typ.	X'tal oscillation	32.768kHz	1.55V	Ag battery version
5.0μA typ.	RC oscillation			
0.8μA typ.	X'tal oscillation	32.768kHz	2.90V	Li battery version
3.0μA typ.	X'tal oscillation	32.768kHz	2.90V	EXT-V version
40μA typ.	RC oscillation			

- Ports
  - Input ports : 2 ports (8 pins)
- Control output pins 3 pins
  - Output dedicated to alarm 2 pins
  - General purpose output 1 pin
- LCD drivers

LCD display mode	Number of drivable segments
Static duty · Static bias	32 segments
1/2 duty · 1/2 bias	64 segments
1/3 duty · 1/2 bias	96 segments
1/4 duty · 1/2 bias	128 segments

- Possible to use LCD drive output pins as output ports (Max. 16 pins, mask option selectable)
- On-chip melody function ..... 3 octaves × 2 channels
- On-chip segment PLA
  The LCD driver can be used to support any LCD pannel layout without software processing.
- On-chip step-up/step-down circuit.
- Shipping style : chip or FLP-64
  Note) When mounting the QIP package on the board, do not dip it in solder.

Software Features

- Powerful instruction set : 92 instructions
- Table read instruction (possible to set table in all ROM areas).
- 1 subroutine stack level.
- 15 bits time base timer.
  - Deliver and overflow signal every 32ms or 64ms, 100ms and 500ms.
- HALT function.

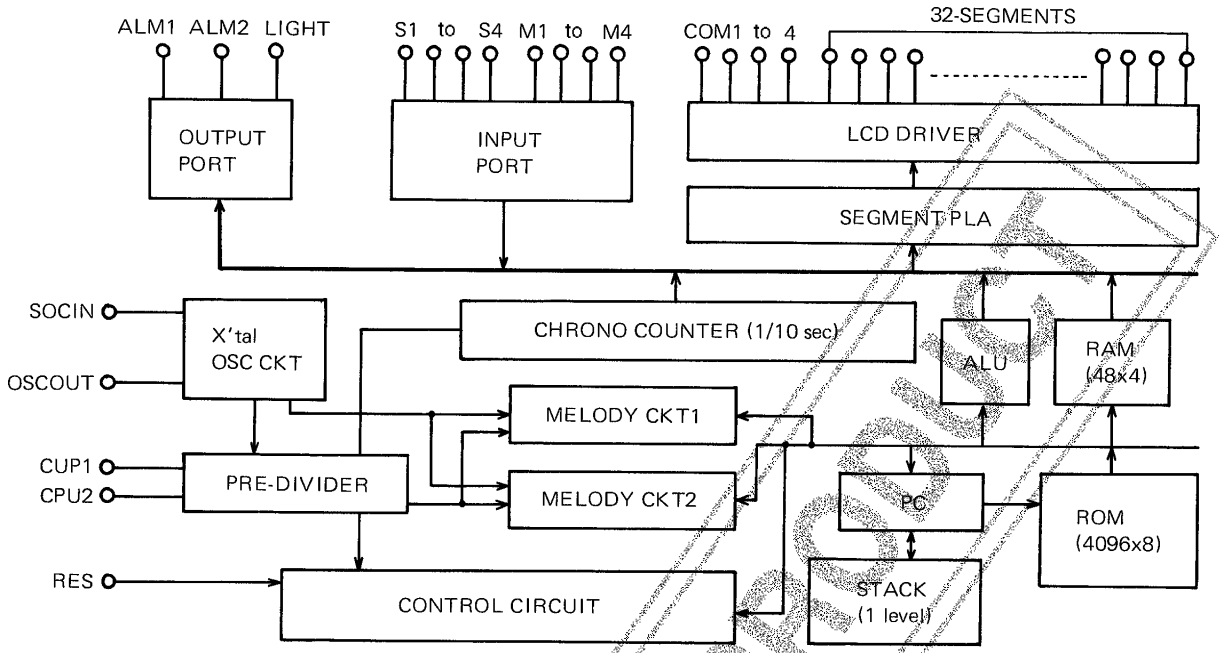
Development Support System

The development support system for the LC5738 applications consists of the following support tools :

(1) Manual
  (a) User's Manual : LC5738 user's manual
  (b) Tool Manual : LC5738 tool manual

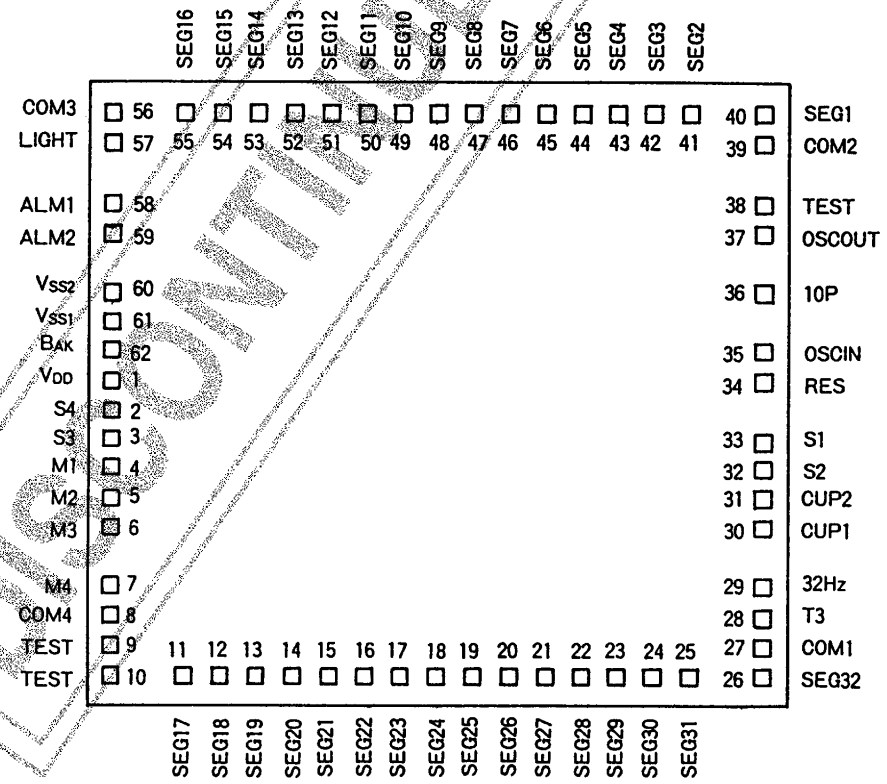
(2) Development support tools
  (a) Tools for developing the LC5738 application programs.
  - MS-DOS machine
  - Assembler (LC5738. EXE)
  - Mask option selections program (SU5738. EXE)
  (b) Tools for evaluating the LC5738 application systems.
  - Evaluation chip : LC5797
  Note 1) Since the evaluation chip LC5797 differs LC5738 with RAM capacity, be sure to check the RAM capacity when preparing or debugging programs.
  LC5738 : 48×4 bits, LC5797 : 256×4 bits
  Note 2) When developing programs, take care of the DPH value. The usable DPH values are 0 to 2 except ROM bank selection.
  We will be free from any blame even if you use DPH=3 to FH for RAM addressing.
  - Evaluation chip board : TB5738
  Note) The application evaluation board is constructed by the user.
  LCD or LEDs may be used for display.
  - Evaluation board : EVA520 (monitor ROM : SCR5738)
  Note) The EVA-520 is a modified version of the EVA-420 whose monitor ROM is replaced by the SCR-5738.
  - Display and mask-option data control board : DCB-1 (Rev.3.3)

Equivalent Circuit and Block Diagram



Pad Assignment of IC Chip

Chip size : 3.85mm×3.75mm
Chip thickness : 480µm
Pad size : 120µm×120µm



Note) SEG17 to 32 can be used for output ports. (Mask option-selectable)

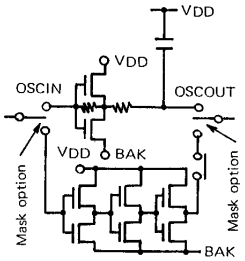
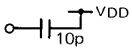
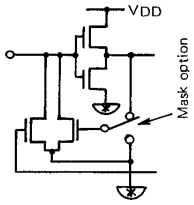
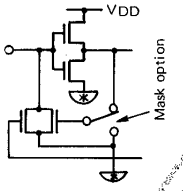
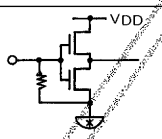
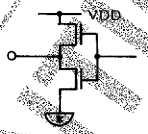
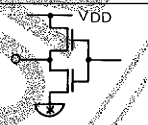
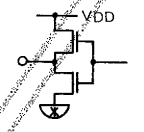
Pad Name and Coordlinates

QIP64 Pin Assignment				
	Pad No.	Pin Name	X (μm)	Y (μm)
55	1	V_{DD}	−1725	335
56	2	S4	−1725	115
57	3	S3	−1725	− 125
58	4	M1	−1725	− 360
59	5	M2	−1725	− 575
60	6	M3	−1725	− 805
61	7	M4	−1725	−1030
62	8	TEST	−1725	−1260
63	9	TEST	−1725	−1485
64	10	COM14	−1725	−1675
1	11	SEG17	−1430	−1675
2	12	SEG18	−1220	−1675
3	13	SEG19	−1010	−1675
4	14	SEG20	− 800	−1675
5	15	SEG21	− 590	−1675
6	16	SEG22	− 380	−1675
7	17	SEG23	− 170	−1675
8	18	SEG24	40	−1675
9	19	SEG25	240	−1675
10	20	SEG26	450	−1675
11	21	SEG27	660	−1675
12	22	SEG28	870	−1675
13	23	SEG29	1080	−1675
14	24	SEG30	1290	−1675
15	25	SEG31	1500	−1675
18	26	SEG32	1730	−1675
19	27	COM1	1730	−1435
20	28	T3	1730	−1185
21	29	32Hz	1730	− 940
22	30	CUP1	1730	− 695
23	31	CUP2	1730	− 455
24	32	S2	1730	− 215
25	33	S1	1730	30
26	34	RES	1730	245
27	35	OSCIN	1730	565

QIP64 Pin Assignment				
	Pad No.	Pin Name	X (μm)	Y (μm)
28	36	10P	1730	775
29	37	OSCOUT	1730	990
30	38	TEST	1730	1255
31	39	COM2	1730	1470
32	40	SEG1	1730	1675
33	41	SEG2	1425	1675
34	42	SEG3	1225	1675
35	43	SEG4	1020	1675
36	44	SEG5	815	1675
37	45	SEG6	610	1675
38	46	SEG7	405	1675
39	47	SEG8	210	1675
40	48	SEG9	10	1675
41	49	SEG10	− 195	1675
42	50	SEG11	− 400	1675
43	51	SEG12	− 605	1675
44	52	SEG13	− 810	1675
45	53	SEG14	−1010	1675
46	54	SEG15	−1215	1675
47	55	SEG16	−1420	1675
48	56	COM3	−1725	1675
49	57	LIGHT	−1725	1495
50	58	ALM1	−1725	1280
51	59	ALM2	−1725	1090
52	60	$V_{SS}2$	−1725	905
53	61	$V_{SS}1$	−1725	725
54	62	BAK	−1725	545

- The pad coordinates are such that the chip enter is taken as the origin and the values for (X, Y) represent the coordinates of the center point of each pad.
- Pin 16, 17 are NC pins.
- The NC pins must not be connected externally.

Pin Description

Pad No.	Pin Name	Input/ Output	Circuit Configuration	Function
35	OSC IN	Input		Crystal OSC mode. 32.768kHz crystal is connected across OSC IN and OSCOUT for oscillation. Used as reference clock for timepiece and system clock. RC OSC mode R and C are connected across OSCIN and OSCOUT for oscillation. Used as system clock.
37	OSCOUT	Output		
36	10P	–		Connected to OSCOUT and used as OSC phase compensation capacitor.
33 32 3 2	S1 S2 S3 S4	Input		Input-only port. IC system is reset by applying V_{DD} to S1 to S4 simultaneously.
4 5 6 7	M1 M2 M3 M4	Input		Input-only port.
34	RES	Input		Input pin for resetting IC system.
62	BAK	–		(–) power supply pin for logic unit inside the IC. For Li battery version, a capacitor must be connected across BAK and V_{DD} to prevent logic unit from malfunctioning.
57	LIGHT	Output		Output-only pin. Suited for delivering signal to drive transistor for light.
58	ALM1	Output		Output-only pin. In case of selecting melody channel-2, used to deliver melody signal of 3 octaves or *4kHz/2kHz/1kHz modulation signal with SAS or TMEL instructions. (Also used to deliver non-modulation signal)
59	ALM2	Output		Output-only pin. In case of selecting melody channel-2, used to deliver melody signal of 3 octaves or *4kHz/2kHz/1kHz modulation signal with SAS or TMEL instructions. (Also used to deliver non-modulation signal)

Continued on next page.

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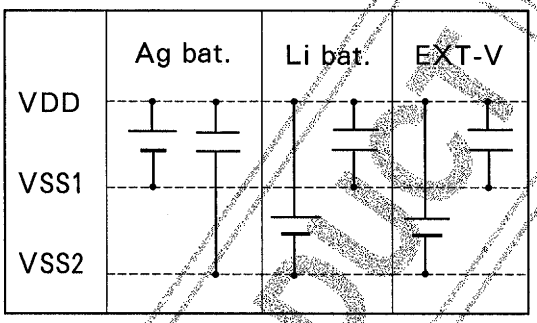
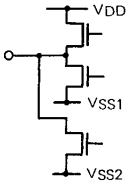
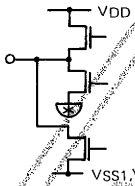
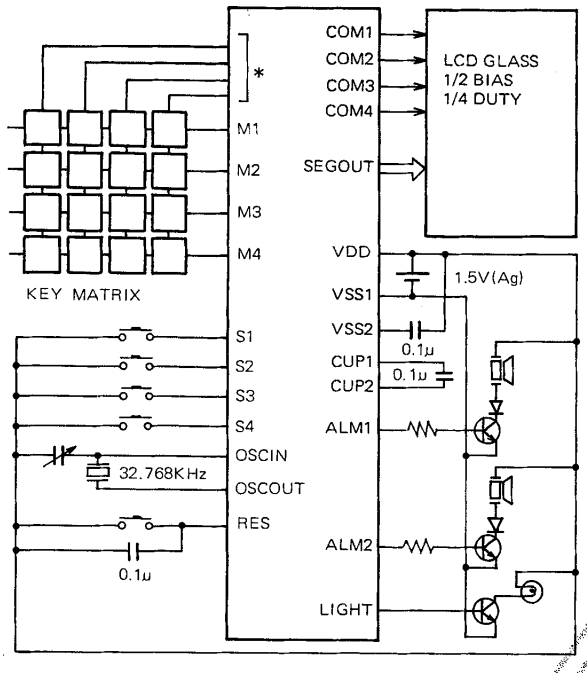
<table>
<tr><th>Pad No.</th><th>Pin Name</th><th>Input/ Output</th><th>Circuit Configuration</th><th>Function</th></tr>
<tr><td>1</td><td>V_{DD}</td><td>–</td><td></td><td>(+) power supply pin.</td></tr>
<tr><td>61
60</td><td>$V_{SS}1$
$V_{SS}2$</td><td>–</td><td></td><td>(–) power supply pin.
Mask option selectable : Ag battery/Li battery EXT-V version.
Also used as power supply for LCD drive.
The following Table shows how to connect external parts in each case.
 
</td></tr>
<tr><td>30
31</td><td>CUP1
CUP2</td><td>–</td><td></td><td>Pins for connecting voltage step-up (step-down) capacitor.</td></tr>
<tr><td>27
39
56
10</td><td>COM1
COM2
COM3
COM4</td><td>Output</td><td> 
</td><td>Output pins for LCD pannel common plate.
The following pins is used in each case.
<table>
<tr><th>Duty mode</th><th>Static</th><th>1/2</th><th>1/3</th><th>1/4</th></tr>
<tr><td>COM1</td><td>○</td><td>○</td><td>○</td><td>○</td></tr>
<tr><td>COM2</td><td>–</td><td>○</td><td>○</td><td>○</td></tr>
<tr><td>COM3</td><td>–</td><td>–</td><td>○</td><td>○</td></tr>
<tr><td>COM4</td><td>–</td><td>–</td><td>–</td><td>○</td></tr>
<tr><td>Alternating frequency</td><td>64Hz</td><td>32Hz</td><td>43Hz</td><td>32Hz</td></tr>
</table></td></tr>
<tr><td>11 to 26

40 to 55</td><td>SEG17 to SEG32
SEG1 to SEG16</td><td>Output</td><td> 
</td><td>Output pins for LCD pannel segments.
Mask option permits SEG17 to SEG32 (pad No. 11 to 26) to be used as output ports.</td></tr>
<tr><td>29
28
8
9
38</td><td>32Hz
T3
TEST
TEST
TEST</td><td>Test</td><td></td><td>Test pins (not used by user)</td></tr>
</table>

Note) For Ag battery power supply, ⏚ is connected to $V_{SS}1$; for Li battery/EXT-V power supply, connected to $V_{SS}2$.
* 4kHz/2kHz/1kHz : For 32.768kHz crystal OSC application, proportional to OSC frequency.

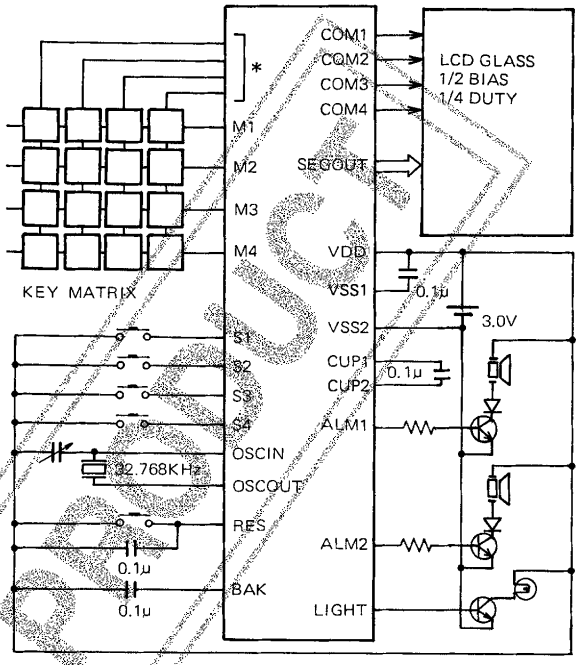
Sample Application Circuits

(1) Ag battery used application (1/2bias 1/4 duty)
* : 4 segment outputs are used for output ports.



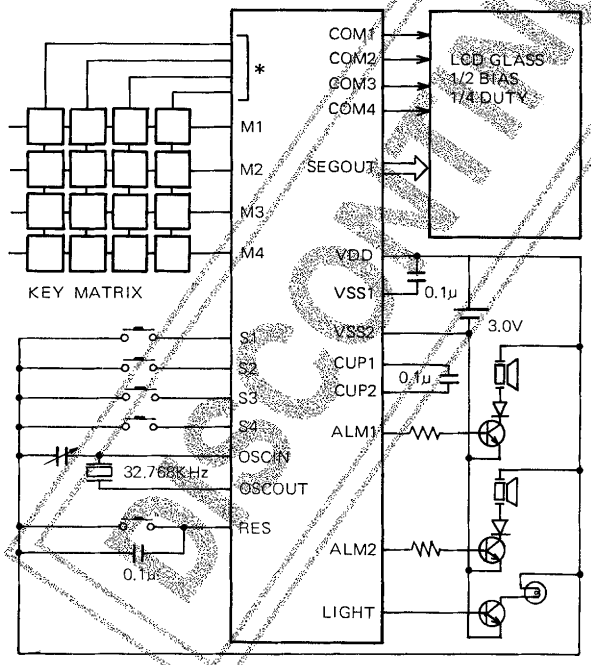
Crystal OSC
(power supply : Ag battery version)

(2) Li battery used application (1/2bias 1/4duty)
* : 4 segment outputs are used for output ports.



Crystal OSC
(power supply : Li battery version)

(3) EXT-V used application (1/2bias 1/4 duty)
* : 4 segment outputs are used for output ports.



Crystal OSC (power supply : EXT-V version)

Unit (capacitance : F)

Specifications

Ag Battery Version

Absolute Maximum Ratings at Ta = 25±2˚C, V_{DD}=0V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{SS}1$		–4.0 to +0.3	V
	$V_{SS}2$		–4.0 to +0.3	V
Input voltage	$V_{IN}1$	S1-S4, M1-M4, 32Hz, TEST, 10p, OSCIN, RES	$V_{SS}1$–0.3 to +0.3	V
Output voltage	$V_{OUT}1$	32Hz, CUP2, OSCOUT, ALM1, ALM2, LIGHT	$V_{SS}1$–0.3 to +0.3	V
	$V_{OUT}2$	SEGOUT, COM1, COM2, COM3, COM4, CUP1	$V_{SS}2$–0.3 to +0.3	V
Output current (per pin)	$I_{OUT}1$	ALM1, ALM2	4	mA
	$I_{OUT}2$	2LIGHT	1	mA
	$I_{OUT}3$	Outputs except ALM1, 2 and LIGHT	500	µA
Output current	I_{ALL}	Total output current	10	mA
Operating temperature	Topr		–30 to +70	˚C
Storage temperature	Tstg		–40 to +125	˚C

Recommended Operating Voltage Range at Ta = –30 to +70˚C, V_{DD}=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply voltage range	$V_{SS}1$		–1.65		–1.30	V
	$V_{SS}2$		–3.3		–2.4	V
Input high-level voltage	V_{IH}	S1 to S4, M1 to M4, RES	–0.2		0	V
Input low-level voltage	V_{IL}	S1 to S4, M1 to M4, RES	$V_{SS}1$		$V_{SS}1$+0.2	V
Oscillation frequency range	$f_{OPG}1$	Crystal oscillation Fig.1	32	32.768	33	kHz
	$f_{OPG}2$	RC oscillation, Fig. 2, Rext=470kΩ, Cext=30pF		32.768		kHz

Electrical Characteristics at Ta =–30 to +70˚C, V_{DD}=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Pull-down transistor	$R_{IN}1A$	$V_{SS}1$=–1.55V, V_{IL}=$V_{SS}1$+0.2V, 'L' level hold Tr, *1, Fig. 3	200		2000	kΩ
	$R_{IN}1B$	$V_{SS}1$=–1.55V, 'L' level pull-in Tr, *1, Fig. 3	200		2000	kΩ
	$R_{IN}2$	$V_{SS}1$=–1.55V, TEST, RES	10		300	kΩ
Output H-level voltage	$V_{OH}1$	$V_{SS}1$=–1.55V, I_{OH}=–0.4µA, *2	–0.2			V
Output L-leve voltage	$V_{OL}1$	$V_{SS}1$=–1.55V, I_{OL}=0.4µA, *2			$V_{SS}2$+0.2	V
Output H-level voltage	$V_{OH}2$	$V_{SS}1$=–1.55V, I_{OH}=–4µA, COM1 to 4	–0.2			V
Output M-level voltage	V_{OM}	$V_{SS}1$=–1.55V, I_{OH}=–4µA, I_{OL}=4µA, COM1 to 4	$V_{SS}1$–0.2		$V_{SS}1$+0.2	V
Output L-level voltage	$V_{OL}2$	$V_{SS}1$=–1.55V, I_{OL}=4µA, COM1 to 4			$V_{SS}2$+0.2	V
Output H-level voltage	$V_{OH}3$	$V_{SS}1$=–1.35V, I_{OH}=–250µA, ALM1, ALM2, LIGHT	–0.65			V
Output L-level voltage	$V_{OL}3$	$V_{SS}1$=–1.35V, I_{OL}=150µA, ALM1, ALM2, LIGHT			$V_{SS}1$+1.65	V
Output H-level voltage	$V_{OH}4$	$V_{SS}1$=–1.55V, I_{OH}=–20µA, *3	–0.2			V
Output L-level voltage	$V_{OL}4$	$V_{SS}1$=–1.55V, I_{OL}=20µA, *3			$V_{SS}1$+0.2	V
Output voltage	$V_{SS}2$	$V_{SS}1$=–1.35V, C1=C2=0.1µF, fopg=32.768kHz, Fig. 4	–3.3		–2.5	V
Current drain in HALT mode	$I_{DD}1$	$V_{SS}1$=–1.55V, C1=C2=0.1µF, Fig. 4, Cg=20pF, Crystal OSC (CI≤25kΩ), Back-up-flag reset, Ta≤50°C		1.0	4.0	µA
	$I_{DD}2$	$V_{SS}1$=–1.55V, C1=C2=0.1µF, Fig. 5, RC OSC (Rext=470kΩ, Cext=30pF), Back-up-flag reset, Ta≤50°C		5.0	15.0	µA
Current drain during basic operation	$I_{DD}3$	$V_{SS}1$=–1.55V, C1=C2=0.1µF, Fig. 4, Cg=20pF, Crystal OSC (CI≤25kΩ), Back-up-flag reset, Ta≤50°C		3.0	12.0	µA
	$I_{DD}4$	$V_{SS}1$=–1.55V, C1=C2=0.1µF, Fig. 5, RC OSC (Rext=470kΩ, Cext=30pF), Back-up-flag reset, Ta≤50°C		7.0	20.0	µA
Oscillation start voltage	V_{stt}	Cg=20pF, Crystal OSC (CI≤25kΩ), Back-up-flag reset, Ta=25°C, Fig. 6	–1.35			V
Oscillation hold voltage	V_{HOLD}	Cg=20pF, Crystal OSC (CI≤25kΩ), Back-up-flag reset, Ta=25°C, Fig. 6			–1.30	V
Oscillation start time	t_{stt}	$V_{SS}1$=–1.35V, Cg=20pF, Crystal OSC (CI≤25kΩ), Back-up-flag reset, Ta=25°C, Fig. 6			10	s
Oscillation compensation capacitance	10P	External pin	8	10	12	pF

Notes for developing an LC5730 series microcontroller-used system.
The low current drain is a distinctive feature of the LC5730 series microcontroller.
However, it is not easy to determine the total current reguired for LC5730 series microcontroller-used system by actual measurement when you develop a software, bacause much current flows in the peripherals of the evaluation tools.
For a system which requires low current drain, check the current drain using an evaluation sample before mass-producting the system.

Li Battery Version

Absolute Maximum Ratings at Ta = 25±2˚C, V_{DD}=0V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{SS}1$		–4.0 to +0.3	V
	$V_{SS}2$		–4.0 to +0.3	V
Input voltage	$V_{IN}1$	32Hz, 10p, OSCIN	V_{SS1}–0.3 to +0.3	V
	$V_{IN}2$	S1 to S4, M1 to M4, TEST, RES	V_{SS2}–0.3 to +0.3	V
Output voltage	V_{OUT1}	32Hz, CUP2, OSCOUT	V_{SS1}–0.3 to +0.3	V
	V_{OUT2}	SEGOUT, COM1 to COM4, CUP1, ALM1, ALM2, LIGHT	V_{SS2}–0.3 to +0.3	V
Output current (per pin)	$I_{OUT}1$	ALM1, ALM2	4	mA
	$I_{OUT}2$	LIGHT	1	mA
	$I_{OUT}3$	Output pin except ALM1, 2 and LIGHT	500	µA
Output current	I_{ALL}	Total output current	10	mA
Operating temperature	Topr		–30 to +70	˚C
Storage temperature	Tstg		–40 to +125	˚C

Recommended Operating Voltage Range at Ta = –30 to +70˚C, V_{DD}=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply voltage range	$V_{SS}1$		–3.6		–1.30	V
	$V_{SS}2$		–3.6		–2.0	V
Input high-level voltage	V_{IH}	S1 to S4, M1 to M4, RES	–0.4		0	V
Input low-level voltage	V_{IL}	S1 to S4, M1 to M4, RES	$V_{SS}2$		$V_{SS}2$+0.4	V
Oscillation frequency range	$f_{OPG}1$	Crystal oscillation Fig.1	32	32.768	33	kHz

Electrical Characteristics at Ta =–30 to +70˚C, V_{DD}=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Pull-down transistor	$R_{IN}1A$	$V_{SS}2$=–2.9V, V_{IL}=V_{SS}2+0.4V, 'L' level hold Tr, *1, Fig. 7	200		2000	kΩ
	$R_{IN}1B$	$V_{SS}2$=–2.9V, 'L' level pull-in Tr, *1, Fig. 7	100		2000	kΩ
	$R_{IN}2$	$V_{SS}2$=–2.9V, TEST, RES	10		300	kΩ
Output H-level voltage	$V_{OH}1$	$V_{SS}2$=–2.9V, I_{OH}=–0.4µA, *2	–0.2			V
Output L-leve voltage	$V_{OL}1$	$V_{SS}2$=–2.9V, I_{OL}=0.4µA, *2			$V_{SS}2$+0.2	V
Output H-level voltage	$V_{OH}2$	$V_{SS}2$=–2.9V, I_{OH}=–4µA, COM1 to 4	–0.2			V
Output M-level voltage	V_{OM}	$V_{SS}2$=–2.9V, I_{OH}=–4µA, I_{OL}=4µA, COM1 to 4	$V_{SS}2/2$–0.2		$V_{SS}2/2$+0.2	V
Output L-level voltage	$V_{OL}2$	$V_{SS}2$=–2.9V, I_{OL}=4µA, COM1 to 4			$V_{SS}2$+0.2	V
Output H-level voltage	$V_{OH}3$	$V_{SS}2$=–2.4V, I_{OH}=–250µA, ALM1, ALM2	–0.65			V
Output L-level voltage	$V_{OL}3$	$V_{SS}2$=–2.4V, I_{OL}=250µA, ALM1, ALM2			$V_{SS}2$+0.65	V
Output H-level voltage	$V_{OH}4$	$V_{SS}2$=–2.4V, I_{OH}=–150µA, LIGHT	–1.5			V
Output L-level voltage	$V_{OL}4$	$V_{SS}2$=–2.4V, I_{OL}=150µA, LIGHT			$V_{SS}2$+1.5	V
Output H-level voltage	$V_{OH}5$	$V_{SS}2$=–2.9V, I_{OH}=–40µA, *3	–0.4			V
Output L-level voltage	$V_{OL}5$	$V_{SS}2$=–2.9V, I_{OL}=40µA, *3			$V_{SS}2$+0.4	V
Output voltage	$V_{SS}1$	$V_{SS}2$=–2.8V, C1=C2=0.1µF, fopg=32.768kHz, Fig. 8			–1.35	V
Current drain in HALT mode	$I_{DD}1$	$V_{SS}2$=–2.9V, C1=C2=0.1µF, Fig. 8, Cg=20pF, Crystal OSC (CI≤25kΩ), Back-up-flag reset, Ta≤50°C		0.8	2.0	µA
Current drain during basic operation	$I_{DD}2$	$V_{SS}2$=–2.9V, C1=C2=0.1µF, Fig. 8, Cg=20pF, Crystal OSC (CI≤25kΩ), Back-up-flag reset, Ta≤50°C		1.5	5.0	µA

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Oscillation start voltage	V_{stt}	Cg=20pF, Crystal OSC (CI≤25kΩ), Back-up-flag reset, Ta=25°C, Fig. 10	–1.35			V
Oscillation hold voltage	V_{HOLD}	Cg=20pF, Crystal OSC (CI≤25kΩ), Back-up-flag reset, Ta=25°C, Fig. 10			–1.3	V
Oscillation start time	t_{stt}	$V_{SS}2$=–1.35V, Cg=20pF, Crystal OSC (CI≤25kΩ), Back-up-flag reset, Ta=25°C, Fig. 10			10	s
Oscillation compensation capacitance	1OP	External pin	8	10	12	pF

EXT-V Version

Absolute Maximum Ratings at Ta = 25±2°C, V_{DD}=0V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{SS}1$		–4.0 to +0.3	V
	$V_{SS}2$		–4.0 to +0.3	V
Input voltage	V_{IN}	S1 to S4, M1 to M4, TEST, RES, 32Hz, 10p, OSCIN	$V_{SS}2$–0.3 to +0.3	V
Output voltage	V_{OUT}	SEGOUT, COM1 to COM4, 32Hz, CUP1, CUP2, OSCOUT, ALM1, ALM2, LIGHT	$V_{SS}2$–0.3 to +0.3	V
Output current (per pin)	$I_{OUT}1$	ALM1, ALM2	4	mA
	$I_{OUT}2$	LIGHT	1	mA
	$I_{OUT}3$	Output except ALM1, 2 and LIGHT	500	µA
Output current	I_{ALL}	Total output current	10	mA
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–40 to +125	°C

Recommended Operating Voltage Range at Ta = –30 to +70°C, V_{DD}=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply voltage range	$V_{SS}1$		–3.6		–1.30	V
	$V_{SS}2$		–3.6		–2.0	V
Input high-level voltage	V_{IH}	S1 to S4, M1 to M4, RES	–0.4		0	V
Input low-level voltage	V_{IL}	S1 to S4, M1 to M4, RES	$V_{SS}2$		$V_{SS}2$+0.4	V
Oscillation frequency range	$f_{OPG}1$	Crystal OSC Fig.1	32	32.768	33	kHz
	$f_{OPG}2$	RC OSC, Fig. 2, Cext=30pF, Rext=470kΩ		32.768		kHz

Electrical Characteristics at Ta =–30 to +70°C, V_{DD}=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Pull-down transistor	$R_{IN}1A$	$V_{SS}2$=–2.9V, V_{IL}=$V_{SS}2$+0.4V, 'L' level hold Tr, *1, Fig. 7	200		2000	kΩ
	$R_{IN}1B$	$V_{SS}2$=–2.9V, 'L' level pull-in Tr, *1, Fig. 7	100		2000	kΩ
	$R_{IN}2$	$V_{SS}2$=–2.9V, TEST, RES	10		300	kΩ
Output H-level voltage	$V_{OH}1$	$V_{SS}2$=–2.9V, I_{OH}=–0.4µA, *2	–0.2			V
Output L-leve voltage	$V_{OL}1$	$V_{SS}2$=–2.9V, I_{OL}=0.4µA, *2			$V_{SS}2$+0.2	V
Output H-level voltage	$V_{OH}2$	$V_{SS}2$=–2.9V, I_{OH}=–4µA, COM1 to 4	–0.2			V
Output M-level voltage	V_{OM}	$V_{SS}2$=–2.9V, I_{OH}=–4µA, I_{OL}=4µA, COM1 to 4	$V_{SS}2/2$–0.2		$V_{SS}2/2$+0.2	V
Output L-level voltage	$V_{OL}2$	$V_{SS}2$=–2.9V, I_{OL}=4µA, COM1 to 4			$V_{SS}2$+0.2	V
Output H-level voltage	$V_{OH}3$	$V_{SS}2$=–2.4V, I_{OH}=–250µA, ALM1, ALM2	–0.65			V
Output L-level voltage	$V_{OL}3$	$V_{SS}2$=–2.4V, I_{OL}=250µA, ALM1, ALM2			$V_{SS}2$+0.65	V
Output H-level voltage	$V_{OH}4$	$V_{SS}2$=–2.4V, I_{OH}=–150µA, LIGHT	–1.5			V
Output L-level voltage	$V_{OL}4$	$V_{SS}2$=–2.4V, I_{OL}=150µA, LIGHT			$V_{SS}2$+1.5	V
Output H-level voltage	$V_{OH}5$	$V_{SS}2$=–2.9V, I_{OH}=–40µA, *3	–0.4			V
Output L-level voltage	$V_{OL}5$	$V_{SS}2$=–2.9V, I_{OL}=40µA, *3			$V_{SS}2$+0.4	V
Output voltage	$V_{SS}1$	$V_{SS}2$=–2.8V, C1=C2=0.1µF, fopg=32.768kHz, Fig. 8			–1.35	V
Current drain in HALT mode	$I_{DD}1$	$V_{SS}2$=–2.9V, C1=C2=0.1µF, Fig. 8, Cg=20pF, Crystal OSC (CI≤25kΩ), Ta≤50°C		3.0	15.0	µA
	$I_{DD}2$	$V_{SS}2$=–2.9V, C1=C2=0.1µF, Fig. 9, RC OSC (Rext=kΩ, Cext=30pF), Ta≤50°C		40	150	µA

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain during basic operation	$I_{DD}3$	$V_{SS}2$=–2.9V, C1=C2=0.1µF, Fig. 9, Cg=20pF, Crystal OSC (CI=25kΩ), Ta≤50°C		7.0	30.0	µA
	$I_{DD}4$	$V_{SS}2$=–2.9V, C1=C2=0.1µF, Fig. 9, RC OSC (Rext=470kΩ,, Cext=30pF), Ta≤50°C		50	180	µA
Oscillation start voltage	V_{stt}	Cg=20pF, Crystal OSC (CI≤25kΩ), Ta=25°C, Fig. 10	2.3			V
Oscillation hold voltage	V_{HOLD}	Cg=20pF, Crystal OSC (CI≤25kΩ), Ta=25°C, Fig. 10			2.0	V
Oscillation start time	t_{stt}	$V_{SS}2$=–2.3V, Cg=20pF, Crystal OSC (CI≤25kΩ), Ta=25°C, Fig. 10			10	s
Oscillation compensation capacitance	1OP	External pin	8	10	12	pF

*1 : S1, S2, S3, S4, M1, M2, M3, M4.
*2 : SEGOUT1 to 16 and LCD output pins out of SEGOUT17 to 32.
*3 : OUTPUT PORT pins out of SEGOUT 17 to 32.

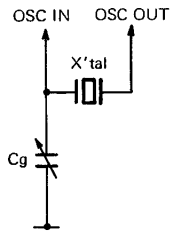

Fig. 1 Recommended crystal oscillation circuit

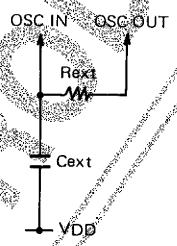

Fig. 2 Recommended CR oscillation circuit

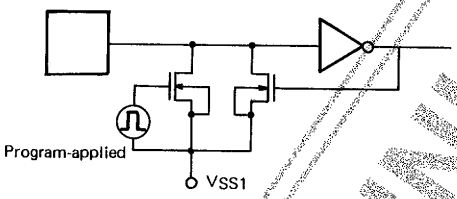

Fig. 3 Input configuration of S1-4, M1-4

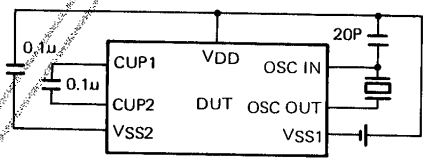

Fig. 4 Current drain, output voltage test circuit

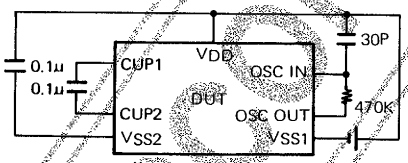

Fig. 5 Current drain, output voltage test current

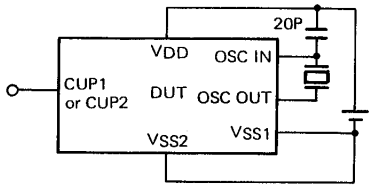

Fig. 6 Oscillation start voltage, oscillation start time, frequency stability, oscillation hold voltage test circuit

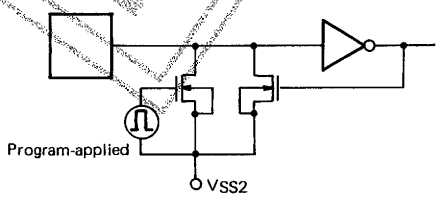

Fig. 7 Input configuration of S1-4, M1-4

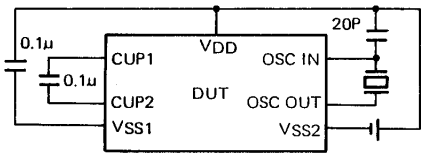

Fig. 8 Current drain, output voltage test circuit

Unit (resistance : Ω, capacitance : F)

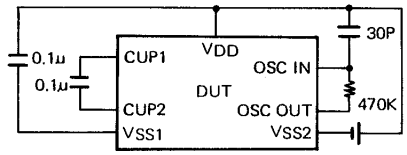

Fig. 9 Current drain, output voltage test circuit

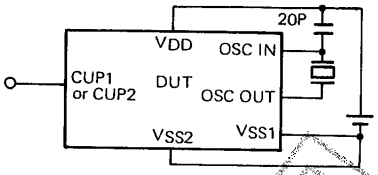

Fig. 10 Oscillation start voltage, oscillation start time, frequency stability, oscillation hold voltage test circui

Unit (resistance : Ω, capacitance : F)