

# 8031AH

Single-Chip 8-Bit Microcontroller

MILITARY INFORMATION

## DISTINCTIVE CHARACTERISTICS

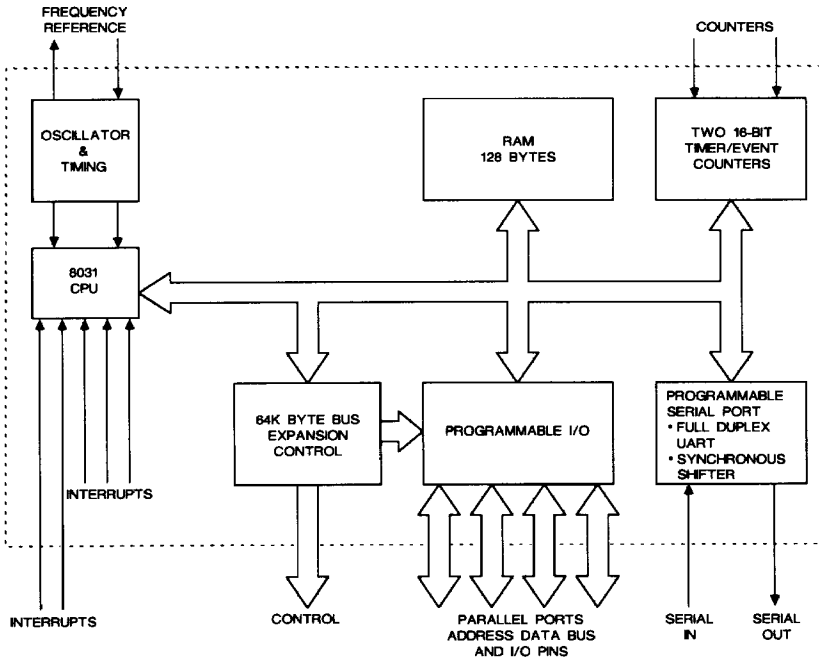
- 128 x 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- 64K addressable Program Memory
- All versions are pin-compatible
- Boolean processor
- Programmable Serial Port
- Five interrupt sources/two priority levels
- On-chip Oscillator/Clock Circuit
- 64K addressable Data Memory

## GENERAL DESCRIPTION

The 8031AH is optimized for control applications. Byte processing and numerical operations on small data structures are facilitated by a variety of fast addressing modes for accessing the internal RAM. The instruction set provides a convenient menu of 8-bit arithmetic instructions, including multiply and divide instructions. Extensive on-chip support is provided for 1-bit variables as a separate data

type. This allows direct bit manipulation and testing in control and logic systems that require Boolean processing. Efficient use of program memory results from an instruction set consisting of 44% 1-byte, 41% 2-byte, and 15% 3-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1  $\mu$ s, 40% in 2  $\mu$ s, and multiply and divide require only 4  $\mu$ s.

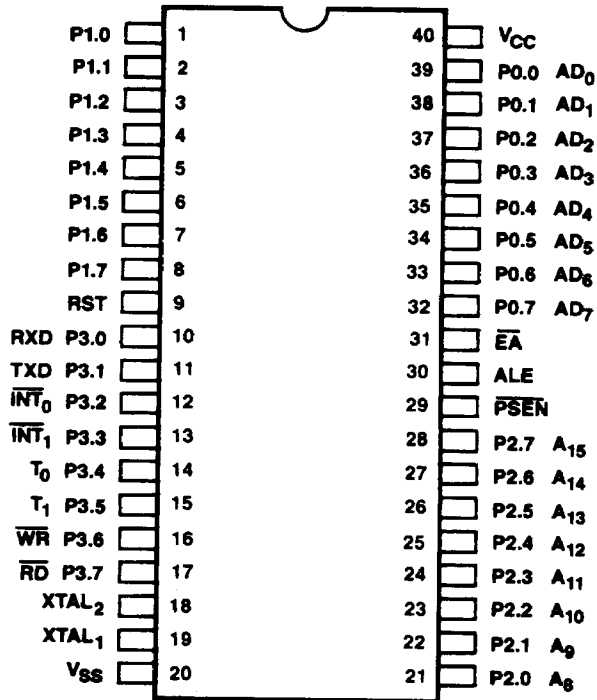
## BLOCK DIAGRAM



BD007261

Publication #	Rev.	Amendment
08399	A	/0
Issue Date: December 1987		

### CONNECTION DIAGRAM Top View



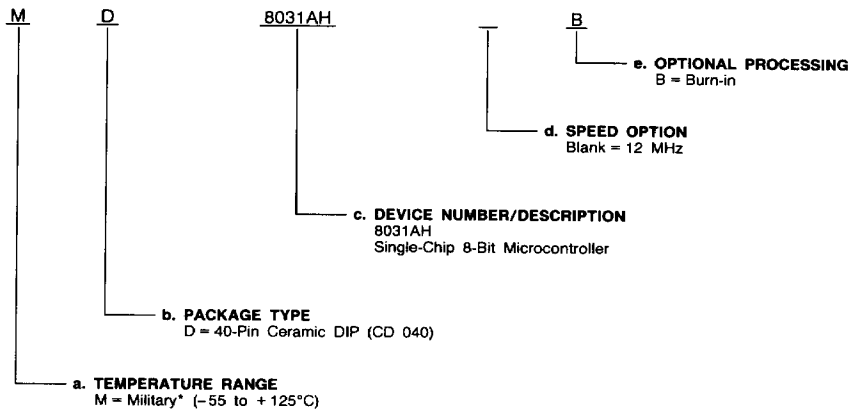
CD005551

Note: Pin 1 is marked for orientation.

### MILITARY ORDERING INFORMATION

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Temperature Range
- b. Package Type
- c. Device Number
- d. Speed Option
- e. Optional Processing



Valid Combinations	
MD	8031AHB

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

\*Military temperature range products are NPL (Non-Compliant Products List) or Non-MIL-STD-883C Compliant Products only.

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature ..... -65 to +150°C  
 Voltage on Any Pin  
   with Respect to Ground ..... -0.5 to +7.0 V  
 Power Dissipation ..... 1 W

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

**OPERATING RANGES**

Military (M) Devices  
 Temperature (T<sub>C</sub>) ..... -55 to +125°C  
 Supply Voltage (V<sub>CC</sub>) ..... +4.5 to +5.5 V  
 Ground (V<sub>SS</sub>) ..... 0 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

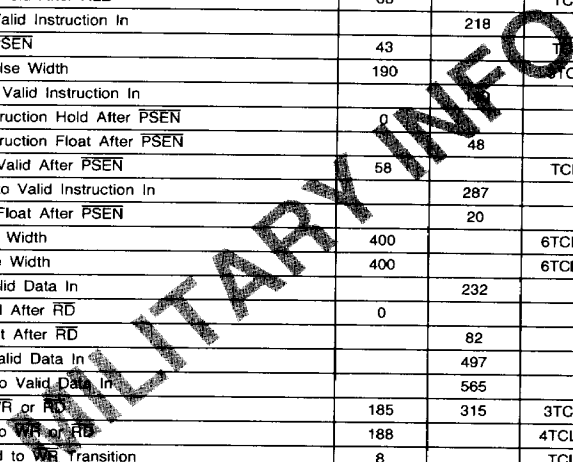
**DC CHARACTERISTICS** over operating ranges

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V <sub>IL</sub>	Input LOW Voltage		-0.5	0.7	V
V <sub>IH</sub>	Input HIGH Voltage (Except RST/V <sub>PD</sub> and XTAL <sub>2</sub> )		2.0	V <sub>CC</sub> + 0.5	V
V <sub>IH1</sub>	Input HIGH Voltage to RST/V <sub>PD</sub> , XTAL <sub>2</sub>	XTAL <sub>1</sub> = V <sub>SS</sub>	2.8	V <sub>CC</sub> + 0.5	V
V <sub>PD</sub>	Power-Down Voltage to RST/V <sub>PD</sub>	V <sub>CC</sub> = 0 V	4.5	5.5	V
V <sub>OL</sub>	Output LOW Voltage, Ports 1, 2, 3 (Note 1)	I <sub>O</sub> = 1.2 mA		0.45	V
V <sub>OL1</sub>	Output LOW Voltage, Port 0, ALE, PSEN (Note 1)	I <sub>O</sub> = 2.4 mA		0.45	V
V <sub>OH</sub>	Output HIGH Voltage, Ports 1, 2, 3	I <sub>OH</sub> = -60 μA	2.4		V
V <sub>OH1</sub>	Output HIGH Voltage, Port 0, ALE, PSEN	I <sub>OH</sub> = -400 μA	2.4		V
I <sub>IL</sub>	Logical 0 Input Current, Ports 1, 2, 3	V <sub>IL</sub> = 0.45 V		-800	μA
I <sub>IL2</sub>	Logical 0 Input Current for XTAL <sub>2</sub>	XTAL <sub>1</sub> = V <sub>SS</sub> V <sub>IN</sub> = 0.45 V		-3.2	mA
I <sub>IH1</sub>	Input HIGH Current to RST/V <sub>PD</sub> for Reset	V <sub>IN</sub> < (V <sub>CC</sub> - 1.5 V)		600	μA
I <sub>LI</sub>	Input Leakage Current to Port 0, E <sub>A</sub>	0.45 < V <sub>IN</sub> < V <sub>CC</sub>		± 10	μA
I <sub>CC</sub>	Power-Supply Current	E <sub>A</sub> = V <sub>CC</sub>		140	mA
I <sub>PD</sub>	Power-Down Current	V <sub>CC</sub> = 0 V; V <sub>PO</sub> = 5.0 V		15	mA
C <sub>IO</sub>	Capacitance of I/O Buffer	f <sub>c</sub> = 1 MHz		10	pF

Notes: 1. Capacitive load on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V<sub>OL</sub>s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.

**SWITCHING CHARACTERISTICS** over operating range (Load Capacitance for Port 0, ALE, and PSEN = 100 pF; Load Capacitance for all other outputs = 80 pF)

Parameter Symbol	Parameter Description	12-MHz Clock		Variable Clock		Unit
		Min.	Max.	Min.	Max.	
TCY 1/TCLCL	Oscillator Frequency			3.5TCLCL	12TCLCL	MHz
TLHLL	ALE Pulse Width	112		2TCLCL-55		ns
TAVLL	Address Setup to ALE	28		TCLCL-55		ns
TLLAX	Address Hold After ALE	33		TCLCL-50		ns
TLLIV	ALE to Valid Instruction In		218		4TCLCL-115	ns
TLLPL	ALE to PSEN	43		TCLCL-40		ns
TPLPH	PSEN Pulse Width	190		TCLCL-60		ns
TPLIV	PSEN to Valid Instruction In				3TCLCL-140	ns
TPXIX	Input Instruction Hold After PSEN	0		0		ns
TPXIZ	Input Instruction Float After PSEN		48		TCLCL-35	ns
TPXAV	Address Valid After PSEN	58		TCLCL-25		ns
TAVIV	Address to Valid Instruction In		287		5TCLCL-130	ns
TPLAZ	Address Float After PSEN		20		20	ns
TRLRH	RD Pulse Width	400		6TCLCL-100		ns
TWLWH	WR Pulse Width	400		6TCLCL-100		ns
TRLDV	RD to Valid Data In		232		5TCLCL-185	ns
TRHDX	Data Hold After RD	0		0		ns
TRHDZ	Data Float After RD		82		2TCLCL-85	ns
TLLDV	ALE to Valid Data In		497		8TCLCL-170	ns
TAVDV	Address to Valid Data In		565		9TCLCL-185	ns
TLLWL	ALE to WR or RD	185	315	3TCLCL-65	3TCLCL+65	ns
TAVWL	Address to WR or RD	188		4TCLCL-145		ns
TQWWX	Data Valid to WR Transition	8		TCLCL-75		ns
TQVWH	Data Setup Before WR	508		7TCLCL-75		ns
TWHQX	Data Hold After WR	18		TCLCL-65		ns
TRLAZ	Address Float After RD		20		20	ns
TWHLH	WR or RD HIGH to ALE HIGH	18	148	TCLCL-65	TCLCL+65	ns

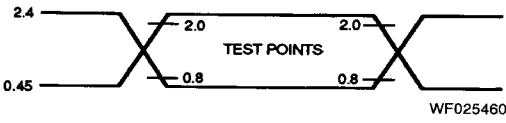


**EXTERNAL CLOCK DRIVE**

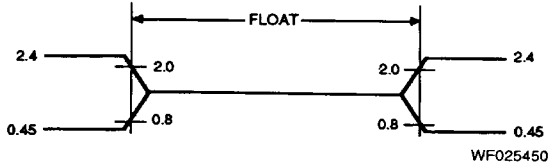
Parameter Symbol	Parameter Description	Min.	Max.	Units
1/TCLCL	Oscillator Frequency	3	2	MHz
TCHCX	HIGH Time	20		ns
TCLCX	LOW Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

MILITARY INFO

**AC TESTING**



**Input/Output Waveform**



**Float Waveform**

AC inputs during testing are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0". For timing purposes, the float state is defined as the point at which a P0 pin sinks 2.4 mA or sources 400  $\mu$ A at the voltage test levels.