OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
HI1-5051-2 or DG4030J

March 2000 File Number 3133.3

Dual SPDT, CMOS Analog Switch

The IH5151 solid state analog switch is designed using an improved, high voltage CMOS technology.

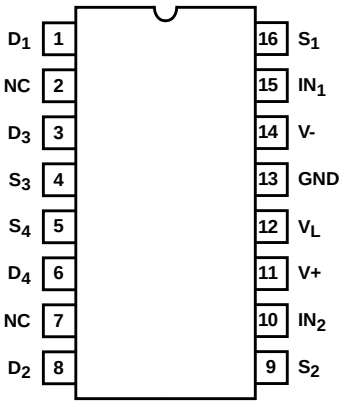
Key performance advantages in the IH5151 are TTL compatibility and ultra low power operation. $r_{DS(ON)}$ switch resistance is typically in the 14Ω to 18Ω area, for signals in the -10V to +10V range. Quiescent current is less than 10µA. The IH5151 also guarantees Break-Before-Make switching which is logically accomplished by extending the t_{ON} time (200ns typical) such that it exceeds t_{OFF} time (120ns typical). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. The need for external logic required to avoid channel to channel shorting during switching is thus eliminated.

Part Number Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
IH5151MJE	-55 to 125	16 Ld CERDIP	F16.3

Pinout

IH5151
(CERDIP)
TOP VIEW

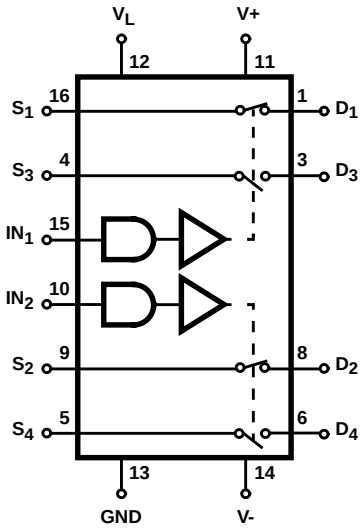


Features

- Low $r_{DS(ON)}$ 25Ω
- Switches Greater than $20V_{P-P}$ Signals with ±15V Supplies
- Quiescent Current (Max) 100µA
- Break-Before-Make Switching
  - t_{OFF} 120ns
  - t_{ON} 200ns
- TTL, CMOS Compatible
- Complete Monolithic Construction
- Supply Range. . . . . ±5V to ±15V

Functional Diagram

SWITCH STATE SHOWN FOR LOGIC "1" INPUT



TRUTH TABLE

LOGIC	SWITCH 1, 2	SWITCH 3, 4
0	Off	On
1	On	Off

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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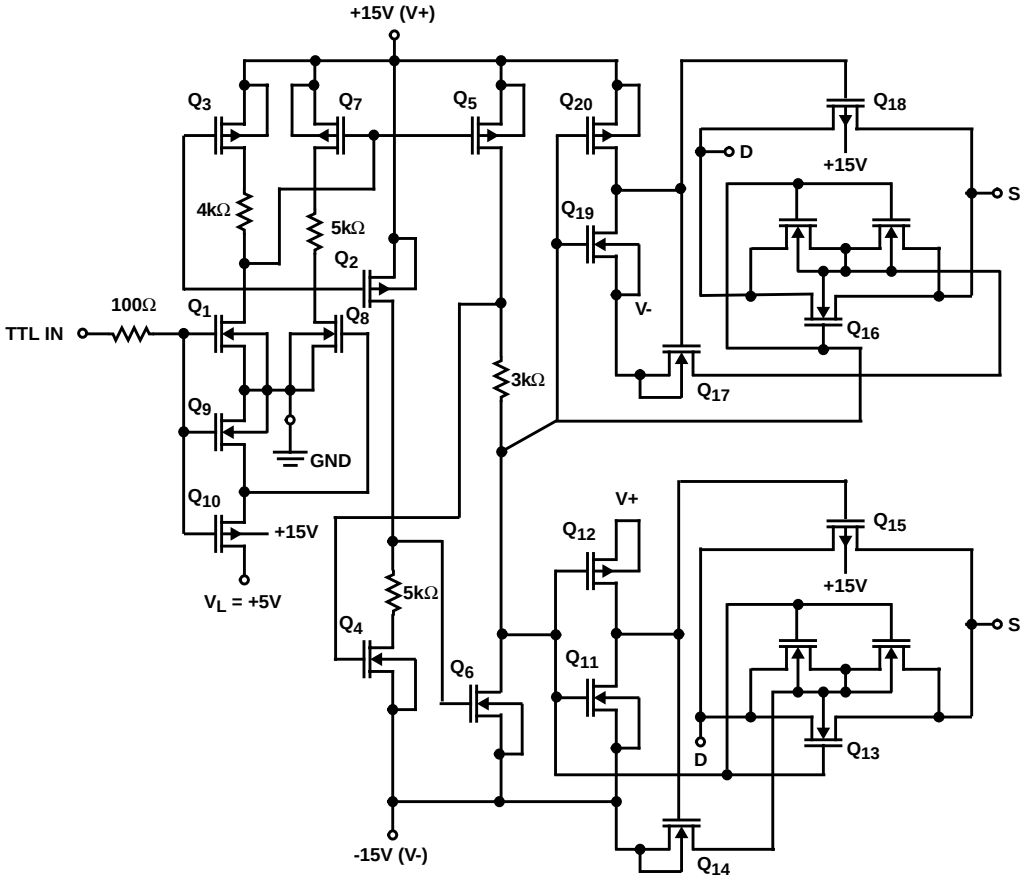
Schematic Diagram

ONE SET OF SWITCHES SHOWN



Absolute Maximum Ratings

V+ to V- . . . . . <36V
V+ to V_D . . . . . <30V
V_D to V- . . . . . <30V
V_D to V_S . . . . . <±22V
V_L to V- . . . . . <33V
V_L to V_{IN} . . . . . <30V
V_L . . . . . <20V
V_{IN} . . . . . <20V
Current (Any Terminal) 50mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	75	18

Maximum Junction Temperature
CERDIP Package . . . . . 175^oC
Maximum Storage Temperature . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V+ = +15V, V- = -15V, V_L = +5V

PER CHANNEL PARAMETER	TEST CONDITIONS	(NOTES 3, 5)			UNITS
		-55^oC	25^oC	125^oC	
DYNAMIC CHARACTERISTICS					
Turn ON Time, t_{ON}	R_L = 1kΩ, V_{ANALOG} = -10V to +10V; (Figure 6, Note 4)	-	-	500	ns
Turn OFF Time, t_{OFF}		-	-	250	ns
Charge Injection, Q	Figure 5	-	10 (Typ)	-	mV
OFF Isolation, OIRR	f = 1MHz, R_L = 100Ω, $C_L \leq$ 5pF (Figure 3)	-	54 (Typ)	-	dB
Crosstalk, CCRR	Figure 2	-	-54 (Typ)	-	dB
DIGITAL INPUT CHARACTERISTICS					
Input Logic Current, $I_{IN(ON)}$	V_{IN} = 2.4V (Note 2)	±1	±1	±10	µA
Input Logic Current, $I_{IN(OFF)}$	V_{IN} = 0.8V (Note 2)	±1	±1	±10	µA
ANALOG SWITCH CHARACTERISTICS					
Drain-Source ON Resistance, $r_{DS(ON)}$	V_D = ±10V, I_S = -10mA	25	25	50	Ω
Channel-to-Channel $r_{DS(ON)}$ Match, $\Delta r_{DS(ON)}$		-	10 (Typ)	-	Ω
Minimum Analog Signal Handling Capability, V_{ANALOG}		-	±14 (Typ)	-	V
Switch OFF Leakage Current, $I_{D(OFF)}$, $I_{S(OFF)}$	V_{ANALOG} = -10V to +10V	-	±1.0	100	nA
Switch ON Leakage Current, $I_{D(ON)}+I_{S(ON)}$	$V_D = V_S$ = -10V to +10V	-	±1.0	100	nA
POWER SUPPLY CHARACTERISTICS					
+ Power Supply Quiescent Current, I+		10	10	100	µA
- Power Supply Quiescent Current, I-		10	10	100	µA
+5V Supply Quiescent Current, I_L		10	10	100	µA
Ground Quiescent Current, I_{GND}		10	10	100	µA

NOTES:

2. Some channels are turned on by high (1) logic inputs and other channels are turned on by low (0) inputs; however 0.8V to 2.4V describes the minimum range for switching properly. Refer to logic diagrams to find logical value of logic input required to produce ON or OFF state.
3. Typical values are for design aid only, not guaranteed or production tested.
4. For IH5151 devices, channels which are off for logic input ≥ 2.4V (Pins 3 and 4, 5 and 6) have slower t_{ON} time, than channels on Pins 1, 16 and 8, 9. This is done so switch will maintain break-before-make action when connected in DT configuration, i.e., Pin 1 connected in Pin 3.
5. Min or Max value, unless otherwise specified.

Test Circuits and Waveforms

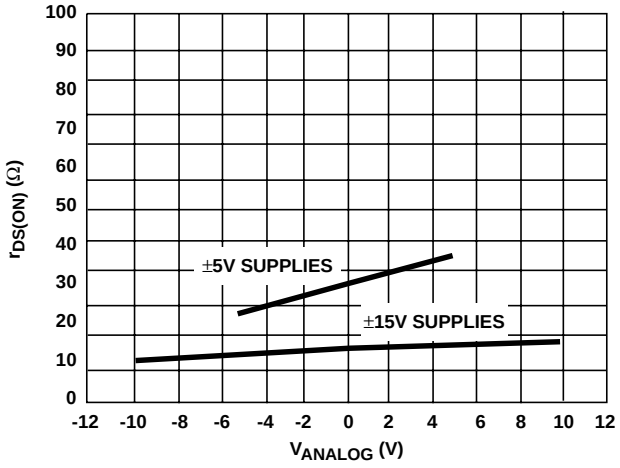


FIGURE 1. $r_{DS(ON)}$ vs ANALOG INPUT VOLTAGE

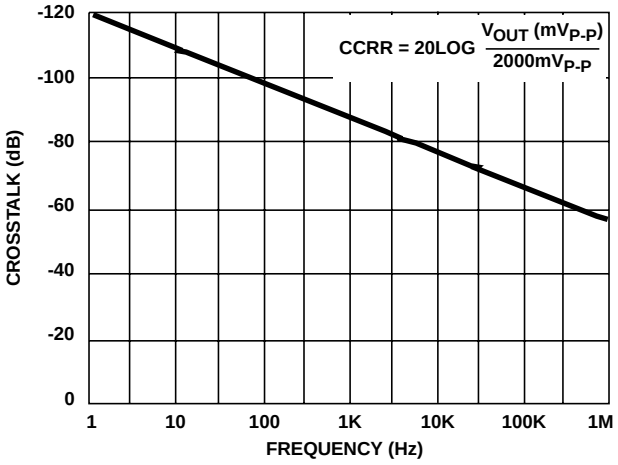


FIGURE 2A. CROSSTALK vs FREQUENCY

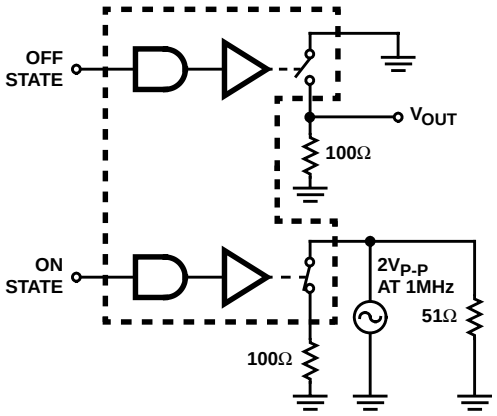


FIGURE 2B. TEST CIRCUIT

FIGURE 2. CROSSTALK

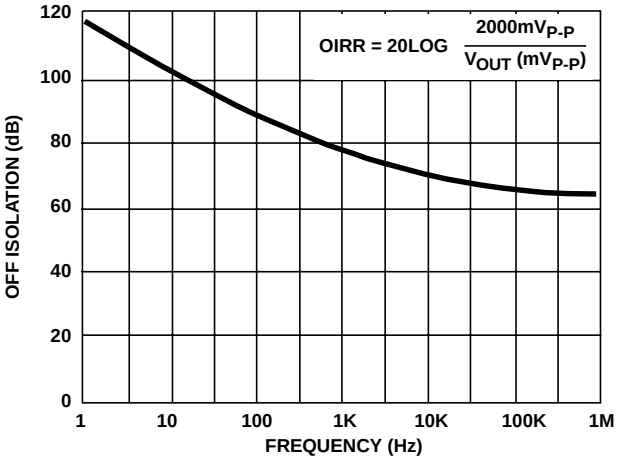


FIGURE 3A. OFF ISOLATION vs FREQUENCY

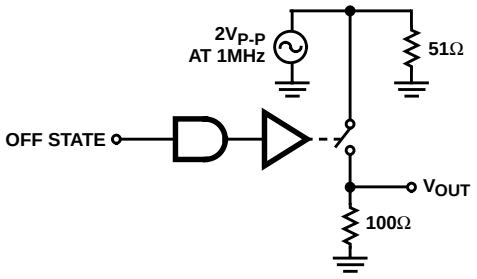


FIGURE 3B. TEST CIRCUIT

FIGURE 3. OFF ISOLATION

Test Circuits and Waveforms (Continued)

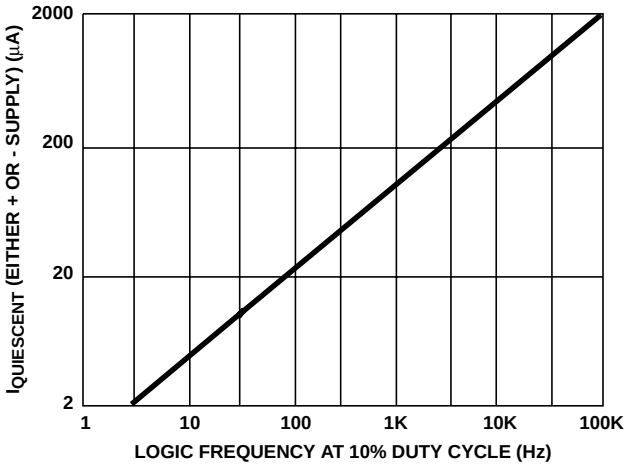


FIGURE 4A. SUPPLY CURRENT vs FREQUENCY

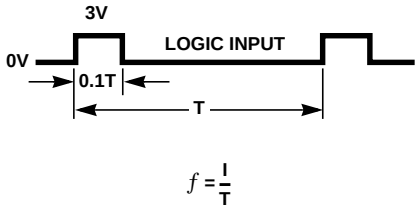


FIGURE 4B. LOGIC INPUT WAVEFORM

FIGURE 4. SUPPLY CURRENT vs LOGIC FREQUENCY

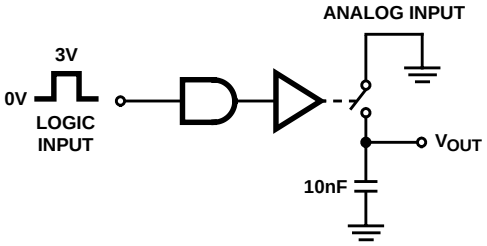


FIGURE 5. CHARGE INJECTION TEST CIRCUIT

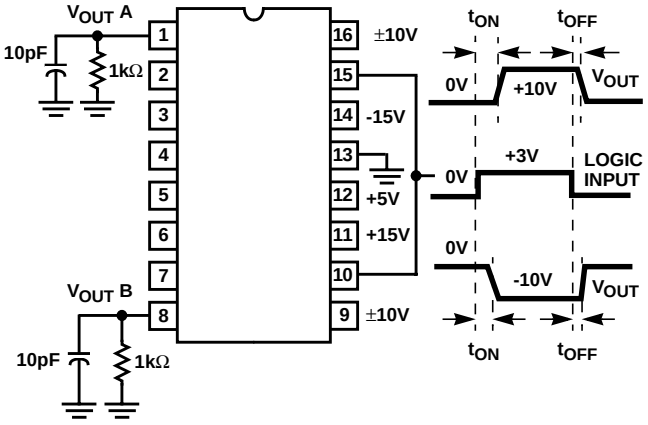


FIGURE 6. t_{ON} AND t_{OFF} TEST CIRCUIT AND MEASUREMENT POINTS

Typical Applications

Nulling Out Charge Injection

Charge injection (Q_{INJ} on spec. sheet) is caused by gate to drain, or gate to source capacitance of the output switch MOSFETs. The gates of these MOSFETs typically swing from -15V to +15V as a rapidly changing pulse; thus this $30V_{P-P}$ pulse is coupled through gate capacitance to output load capacitance, and the output "step" is a voltage divider from this combination. For example:

$$Qinject\ (V_{P-P}) \cong \frac{C_{GATE}}{C_{LOAD}} \times 30V\ step.$$

i.e.,

$C_{GATE} = 1.5pF$, $C_{LOAD} = 1000pF$, then

$$Qinject\ (V_{P-P}) = \frac{1.5pF}{1000pF} \times 30V\ step = 45mV_{P-P}$$

Thus if you are using a switch in a Sample and Hold application with C_{SAMPLE} = 1000pF, a $45mV_{P-P}$ "Sample-to-Hold Error Step" will occur.

To null this error step out to zero the circuit in Figure 7 can be used.

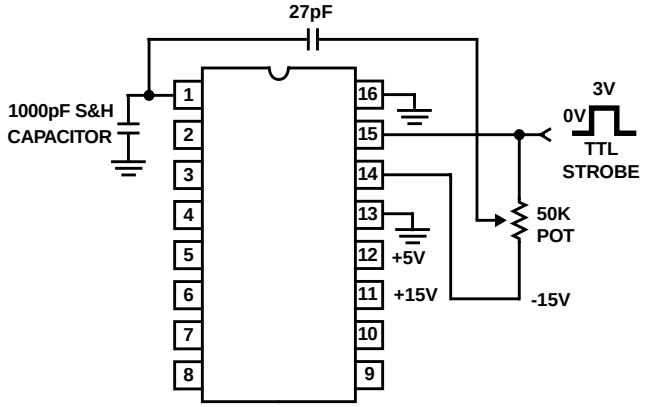


FIGURE 7. ADJUSTABLE CHARGE INJECTION COMPENSATION CIRCUIT

The circuit in Figure 7 nulls out charge injection effects on switch pins 1 and 16; a similar circuit would be required on switch pins 8 and 9.

Simply adjust the pot until V_{OUT} = 0mV_{P-P} pulse, with V_{ANALOG} = 0V.

If you do not desire to do any adjusting, but wish the least amount of charge injection possible, then the circuit in Figure 8 should be used.

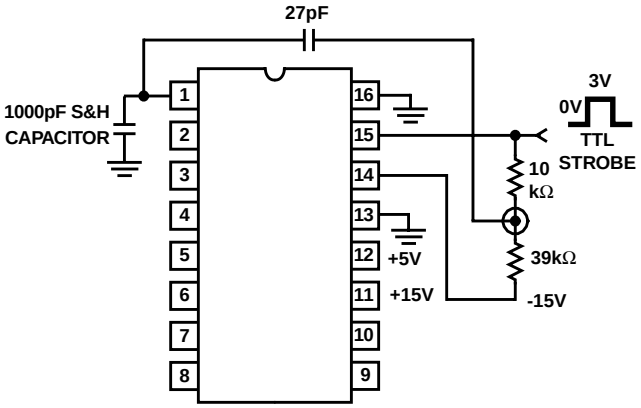


FIGURE 8. NO-ADJUST CHARGE INJECTION COMPENSATION CIRCUIT

This configuration will produce a typical charge injection of V_{OUT} ±10mV_{P-P} into the 1000pF S & H capacitor shown.

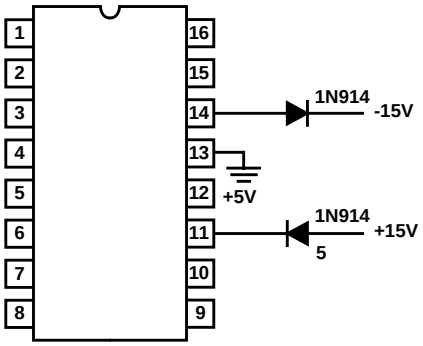


FIGURE 9. ADDING DIODES PROTECTS SWITCH

Fault Condition Protection

If your system has analog voltage levels which are independent of the ±15V (Power Supplies), and these analog levels can be present when supplies are shut off, you should add fault protection diodes as shown in Figure 9.

If the analog input levels are below ±15V, the PN junctions of Q_{13} and Q_{15} are reversed biased. However if the ±15V supplies are shut off and analog levels are still present, the configuration becomes as shown in Figure 10.

The need for the diodes in this circumstance is shown in Figure 11. If ANALOG INPUT is greater than 1V, then the PN junction of Q_{15} is forward biased and excessive current will be drawn. The addition of 1N914 diodes prevents the fault currents from destroying the switch. A similar event would occur if ANALOG INPUT was less than or equal to -1V, wherein Q_{13} would become forward biased. The 1N914 diodes form a “back to back” diode arrangement with Q_{13} and Q_{15} bodies.

This structure provides a degree of overvoltage protection when supplies are on normally, and analog input level exceeds supplies.

This circuit will switch up to about ±8V ANALOG overvoltages. Beyond this drain (N) to body (P) breakdown VOLTAGE of Q_{13} limits overvoltage protection.

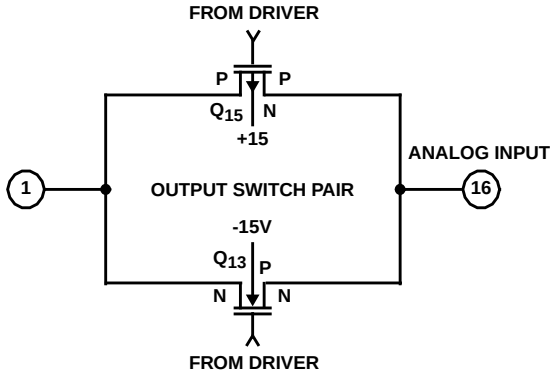


FIGURE 10. SWITCH WITHOUT PROTECTION DIODES

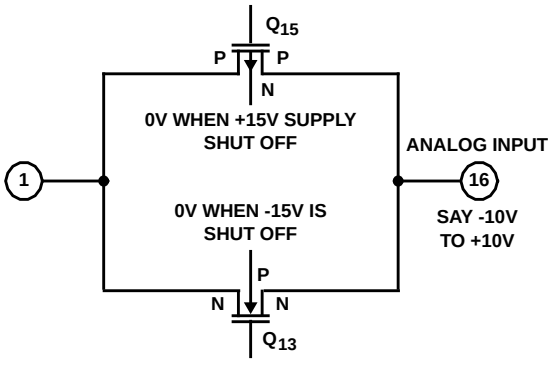


FIGURE 11. FAULT CONDITION WITHOUT PROTECTION DIODES

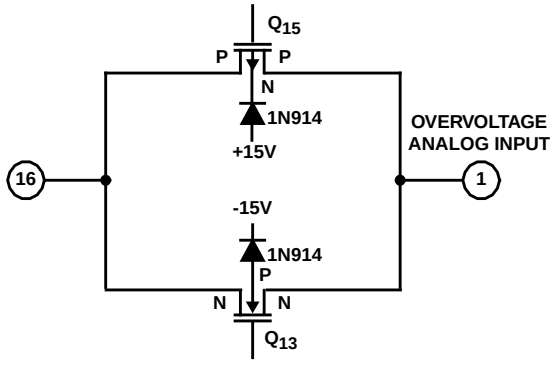


FIGURE 12. FAULT CONDITION WITH PROTECTION DIODES

Die Characteristics

DIE DIMENSIONS:

2515µm x 3074µm

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

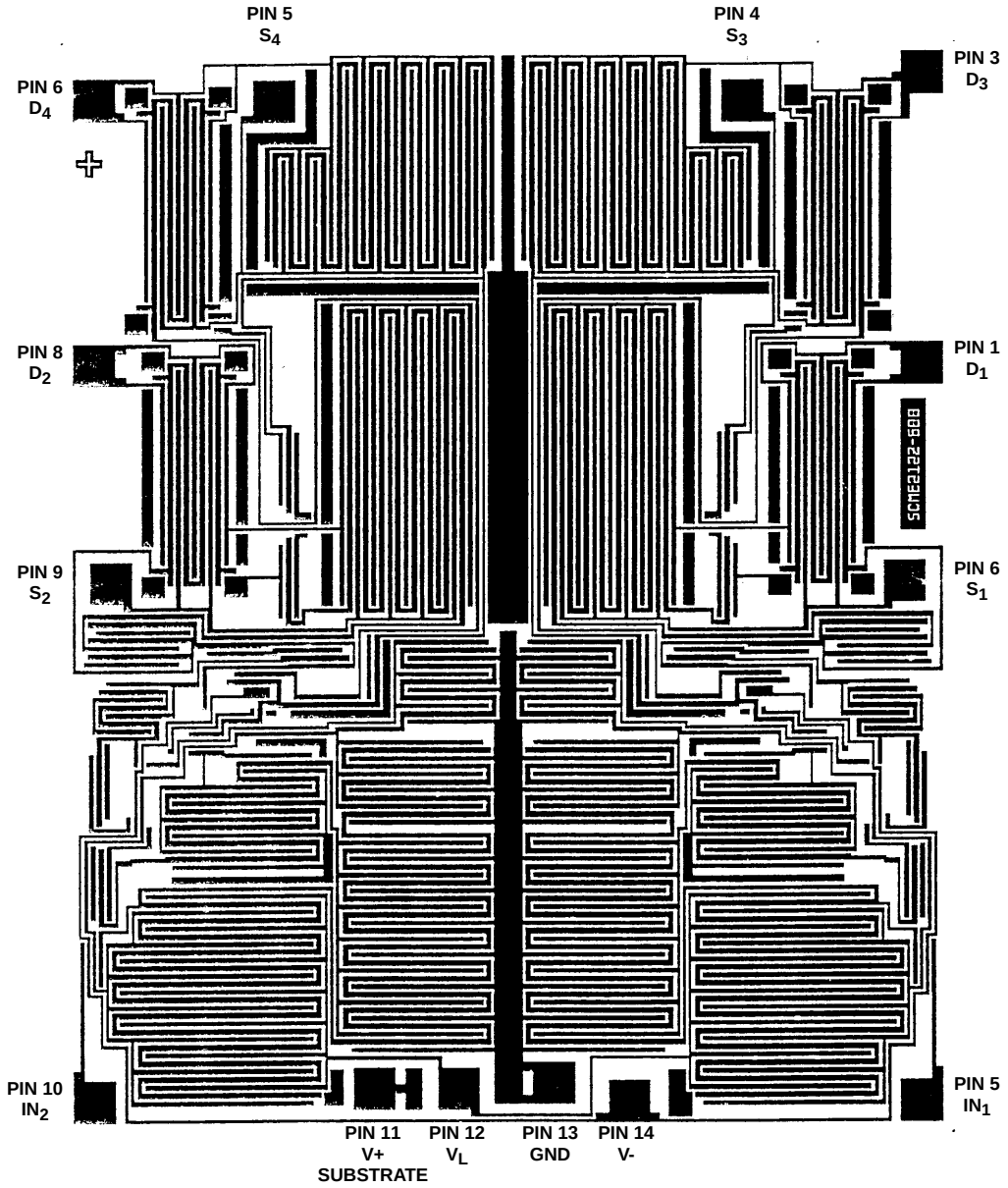
Type: PSG Over Nitride
PSG Thickness: 7kÅ ±1.4kÅ
Nitride Thickness: 8kÅ ±1.2kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

IH5151



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