HIGH-SPEED CMOS DUAL 4-INPUT MULTIPLEXER

IDTQS74FCT153AT/CT

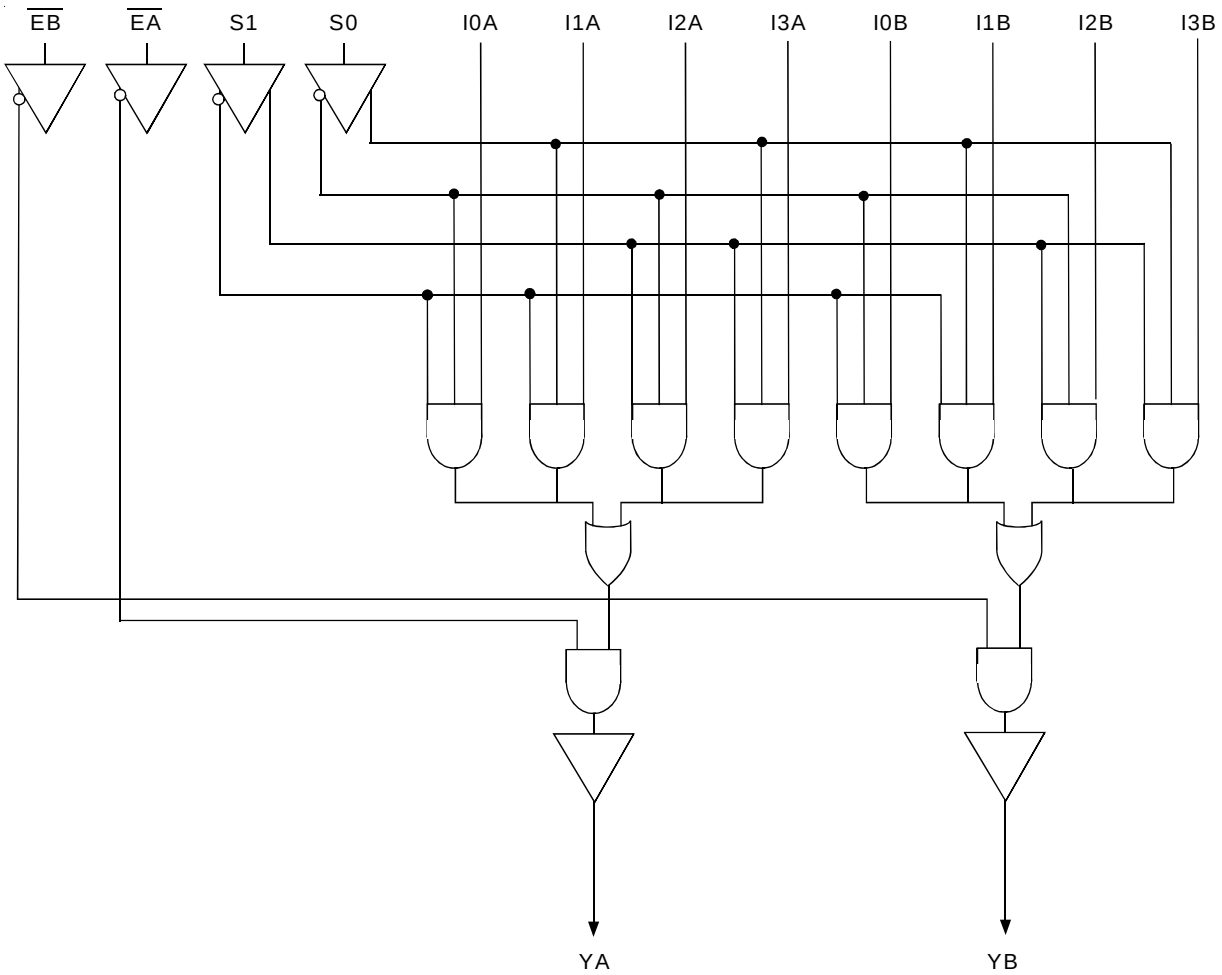
FEATURES:

- **CMOS power levels: <7.5mW static**
- **Undershoot clamp diodes on all inputs**
- **True TTL input and output compatibility**
- **Ground bounce controlled outputs**
- **Reduced output swing of 0 to 3.5V**
- **A and C grades with 4.5ns t_{PD} for C**
- **I_{OL} = 48mA**
- **Available in SOIC and QSOP packages**

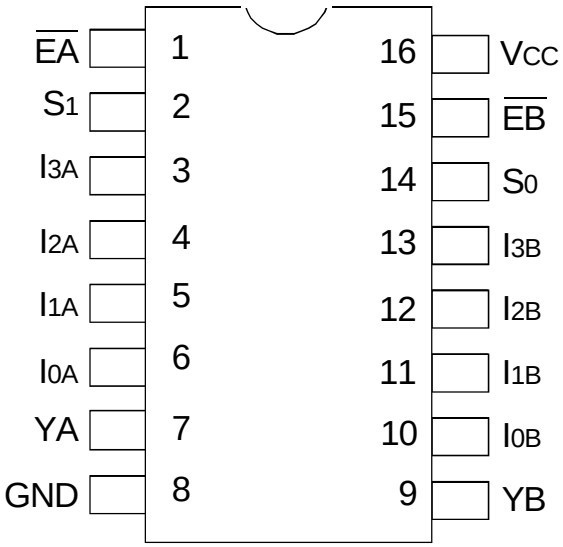
DESCRIPTION:

The IDTQS74FCT153T is a high-speed CMOS TTL-compatible dual 4-input multiplexer. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression. Outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current Max Current Sink/Pin	+120	mA
I_{IK}	Input Diode Current, $V_{IN} < 0$	-20	mA
I_{OK}	DC Output Current, $V_{OUT} < 0$	-50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4	—	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	—	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	I/O	Description
Ixx	I	Data In
S_0 - S_1	I	Select
$\overline{EA}$, $\overline{EB}$	I	Enable
YA, YB	O	Data Out

FUNCTION TABLE(1)

Enable		Inputs		Output		
$\overline{EA}$	$\overline{EB}$	S_1	S_0	YA	YB	Function
H	X	X	X	L	X	Disable A
X	H	X	X	X	L	Disable B
L	L	L	L	1_{0A}	1_{0B}	S_1 - 0 = 0
L	L	L	H	1_{1A}	1_{1B}	S_1 - 0 = 1
L	L	H	L	1_{2A}	1_{2B}	S_1 - 0 = 2
L	L	H	H	1_{3A}	1_{3B}	S_1 - 0 = 3

NOTE:
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
ΔV_T	Input Hysteresis	V_{TLH} - V_{THL} for all inputs		—	0.2	—	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	0 ≤ V_{IN} ≤ V_{CC}	—	—	±5	µA
I_{IL}	Input LOW Current						
I_{OS}	Short Circuit Current	V_{CC} = Max., V_{OUT} = GND(2)		–60	—	—	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18mA, T_A = 25°C(2)		—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –15mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 48mA	—	—	0.5	V

NOTES:
1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)	Min.	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. freq = 0 0V ≤ V_{IN} ≤ 0.2V or V_{CC} - 0.2V ≤ V_{IN} ≤ V_{CC}	—	1.5	mA
ΔI_{CC}	Supply Current per Input TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(2) freq = 0	—	2	mA
I_{CCD}	Supply Current per Input per MHz	V_{CC} = Max. Outputs Open and Enabled One Bit Toggling 50% Duty Cycle Other inputs at GND or V_{CC}(3,4)	—	0.25	mA/ MHz

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under DC Electrical Characteristics.
2. Per TTL driven input (V_{IN} = 3.4V).
3. For flip-flops, I_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance.
4. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Output Frequency
   N_i = Number of Outputs at f_i

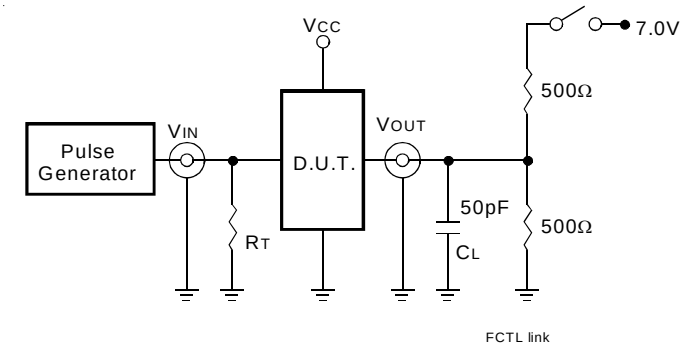
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE(1)

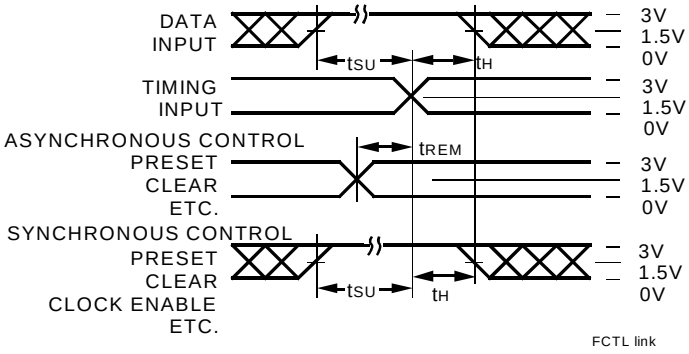
Symbol	Parameter	74FCT153AT		74FCT153CT		Unit
		Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Ixx to Y	1.5	5.2	1.5	4.5	ns
t_{PLH} t_{PHL}	Propagation Delay Sx to Y	1.5	6.6	1.5	5.6	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Y	1.5	5.2	1.5	4.8	ns

NOTE:
1. C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

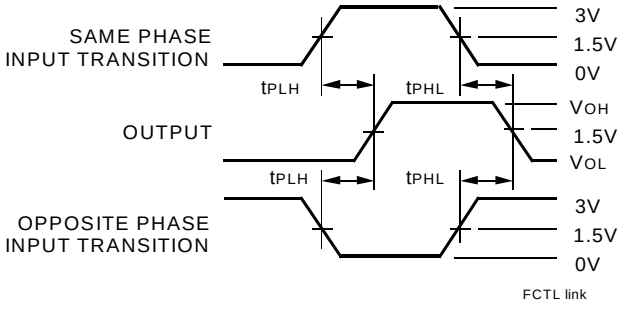
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



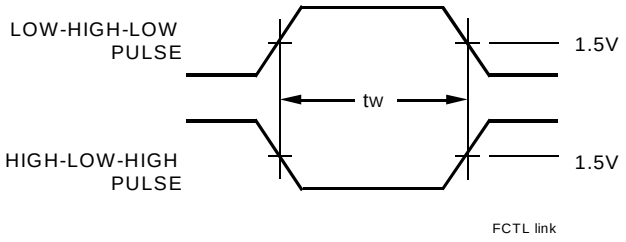
Propagation Delay

SWITCH POSITION

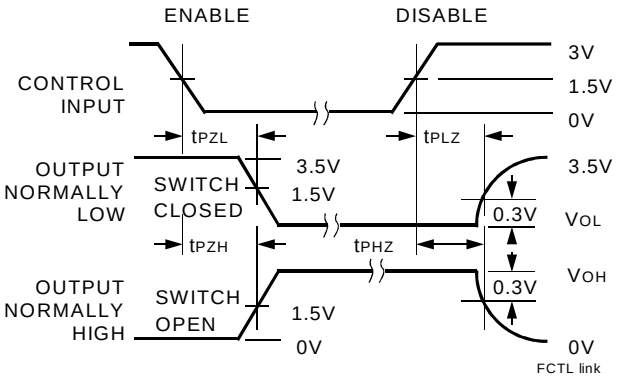
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



Pulse Width

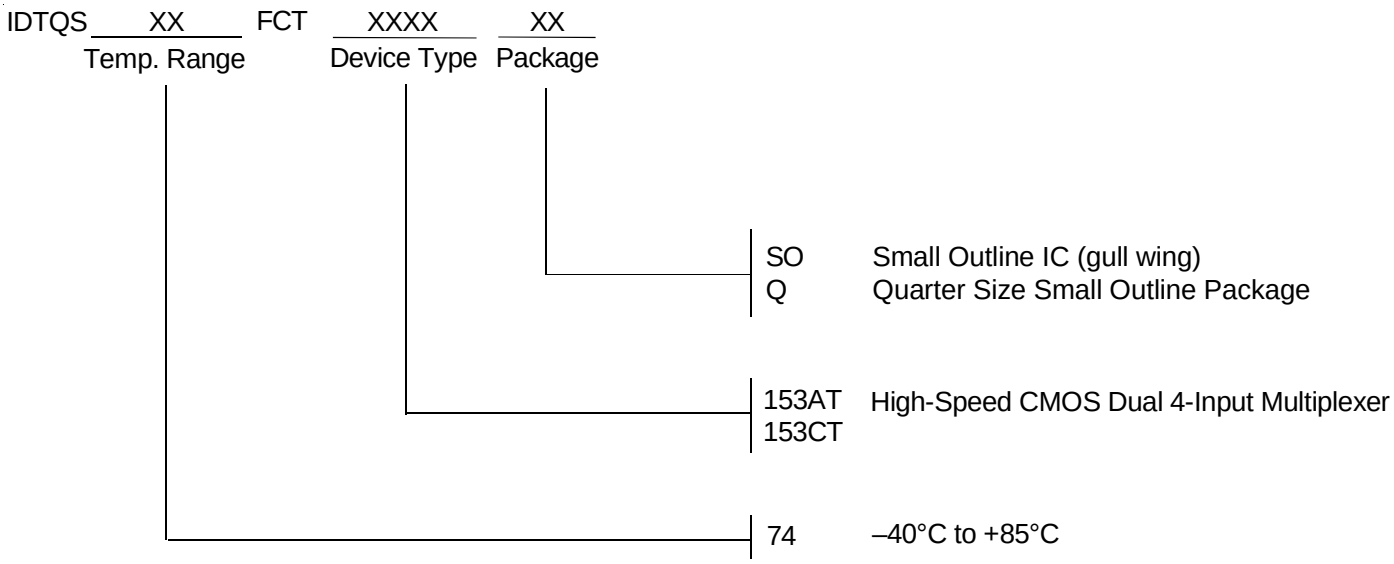


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



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