



DUAL BCD COUNTER

The HEF4518B is a dual 4-bit internally synchronous BCD counter. The counter has an active HIGH clock input (CP_0) and an active LOW clock input (\overline{CP}_1), buffered outputs from all four bit positions (O_0 to O_3) and an active HIGH overriding asynchronous master reset input (MR). The counter advances on either the LOW to HIGH transition of the CP_0 input if \overline{CP}_1 is HIGH or the HIGH to LOW transition of the \overline{CP}_1 input if CP_0 is LOW. Either CP_0 or \overline{CP}_1 may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on MR resets the counter (O_0 to $O_3 = \text{LOW}$) independent of CP_0 , \overline{CP}_1 . Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

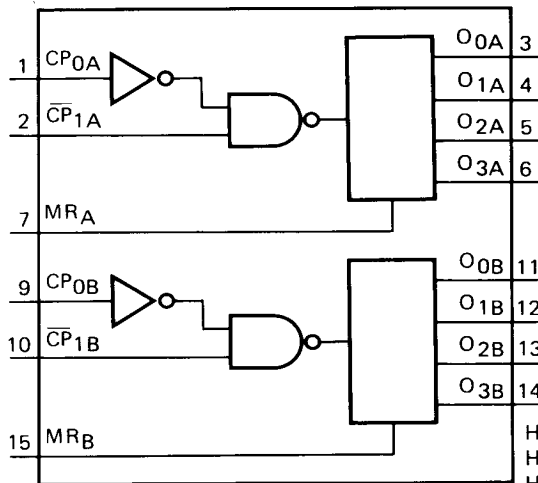


Fig. 1 Functional diagram.

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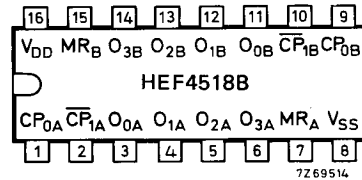


Fig. 2 Pinning diagram.

HEF4518BP : 16-lead DIL; plastic (SOT-38Z).
HEF4518BD : 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4518BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

CP_{0A} , CP_{0B} clock inputs (L to H triggered)
 \overline{CP}_{1A} , \overline{CP}_{1B} clock inputs (H to L triggered)
 MR_A , MR_B master reset inputs
 O_{0A} to O_{3A} outputs
 O_{0B} to O_{3B} outputs

APPLICATION INFORMATION

Some examples of applications for the HEF4518B are:

- Multistage synchronous counting.
- Multistage asynchronous counting.
- Frequency dividers.

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

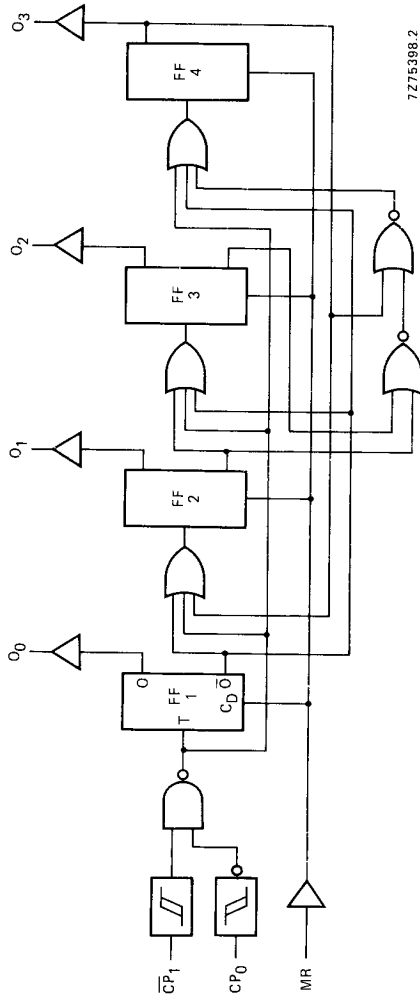


Fig. 3 Logic diagram (one counter).

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial
 / = positive-going transition
 \ = negative-going transition

FUNCTION TABLE

CP0	CP1	MR	mode
/	H	L	counter advances
L	\	L	counter advances
\	X	L	no change
X	/	L	no change
/	L	L	no change
H	\	L	no change
X	X	H	O ₀ to O ₃ = LOW

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays $CP_0, \overline{CP}_1 \rightarrow O_n$ HIGH to LOW	5	tPHL		120	240 ns	$93\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		55	110 ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		40	80 ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	tPLH		120	240 ns	$93\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		55	110 ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		40	80 ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$	
MR $\rightarrow O_n$ HIGH to LOW	5	tPHL		75	150 ns	$48\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		35	70 ns	$24\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		25	50 ns	$17\text{ ns} + (0,16\text{ ns/pF}) C_L$	
Output transition times HIGH to LOW	5	tTHL		60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60 ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40 ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
LOW to HIGH	5	tTLH		60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60 ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40 ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
Minimum CP_0 pulse width; LOW	5	tWCPL	60	30	ns	
	10		30	15	ns	
	15		20	10	ns	
Minimum \overline{CP}_1 pulse width; HIGH	5	tWCPH	60	30	ns	
	10		30	15	ns	
	15		20	10	ns	
Minimum MR pulse width; HIGH	5	tWMRH	30	15	ns	
	10		20	10	ns	
	15		16	8	ns	
Recovery time for MR	5	tRMR	50	25	ns	see also waveforms Figs 4 and 5
	10		30	15	ns	
	15		20	10	ns	
Set-up times $CP_0 \rightarrow \overline{CP}_1$	5	t _{su}	50	25	ns	
	10		30	15	ns	
	15		20	10	ns	
$\overline{CP}_1 \rightarrow CP_0$	5	t _{su}	50	25	ns	
	10		30	15	ns	
	15		20	10	ns	
Maximum clock pulse frequency	5	f _{max}	8	16	MHz	
	10		15	30	MHz	
	15		20	40	MHz	

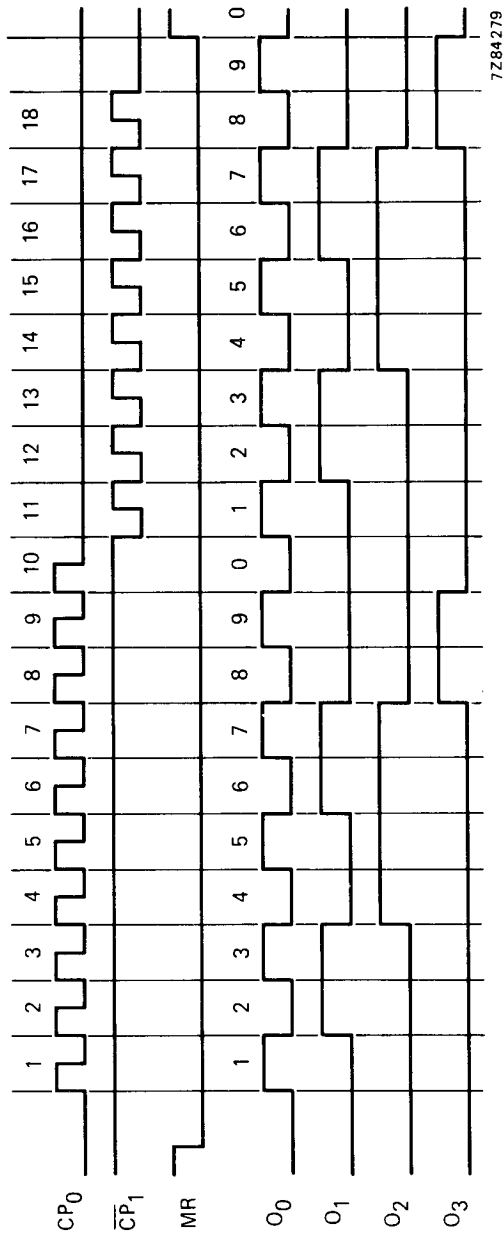


Fig. 6 Timing diagram.