

CD4007C Dual Complementary Pair Plus Inverter

General Description

The CD4007C consists of three complementary pairs of N- and P-channel enhancement mode MOS transistors suitable for series/shunt applications. All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS} .

For proper operation the voltages at all pins must be constrained to be between $V_{SS} - 0.3V$ and $V_{DD} + 0.3V$ at all times.

Features

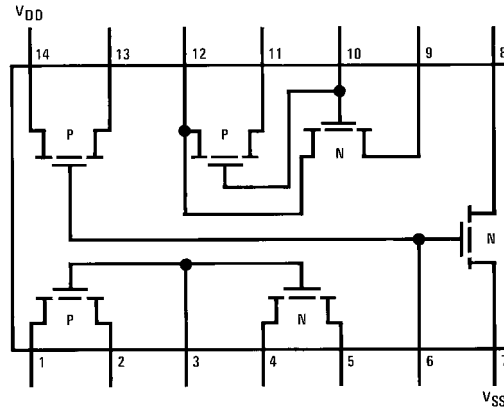
- Wide supply voltage range: 3.0V to 15V
- High noise immunity: $0.45 V_{CC}$ (typ.)

Ordering Code:

Order Number	Package Number	Package Description
CD4007CM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4007CN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Note: All P-channel substrates are connected to V_{DD} and all N-channel substrates are connected to V_{SS} .

Top View

Absolute Maximum Ratings(Note 1)

Voltage at Any Pin	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{DD} Range	$V_{SS} + 3.0V$ to $V_{SS} + 15V$
Lead Temperature (Soldering, 10 seconds)	260°C

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

DC Electrical Characteristics

Symbol	Parameter	Conditions	Limits									Units
			-55°C			+25°C			+125°C			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_L	Quiescent Device Current	$V_{DD} = 5.0V$ $V_{DD} = 10V$			0.05 0.1		0.001 0.001	0.05 1.0			3.0 6.0	μA
P_D	Quiescent Device Dissipation Package	$V_{DD} = 5.0V$ $V_{DD} = 10V$			0.25 1.0		0.005 0.001	2.5 10			15 60	μW
V_{OL}	Output Voltage LOW Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$			0.05 0.05		0 0	0.01 0.01			0.05 0.05	V
V_{OH}	Output Voltage HIGH Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$	4.95 9.95			4.95 9.95	5.0 10		4.95 9.95			V
V_{NL}	Noise Immunity (All inputs)	$V_{DD} = 5.0V, V_O = 3.6V$ $V_{DD} = 10V, V_O = 7.2V$			1.5 3.0		2.25 4.5	1.5 3.0			1.4 2.9	V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V, V_O = 0.95V$ $V_{DD} = 10V, V_O = 2.9V$	3.6 7.1			3.5 7.0	2.25 4.5		3.5 7.0			V
I_{DN}	Output Drive Current N-Channel	$V_{DD} = 5.0V, V_O = 0.4V, V_I = V_{DD}$ $V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}$	0.75 1.6			0.6 1.3	1.0 2.5		0.4 0.95			mA
I_{DP}	Output Drive Current P-Channel	$V_{DD} = 5.0V, V_O = 2.5V, V_I = V_{SS}$ $V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}$	-1.75 -1.35			-1.4 -1.1	-4.0 -2.5		-1.0 -0.75			mA
I_I	Input Current						10					pA

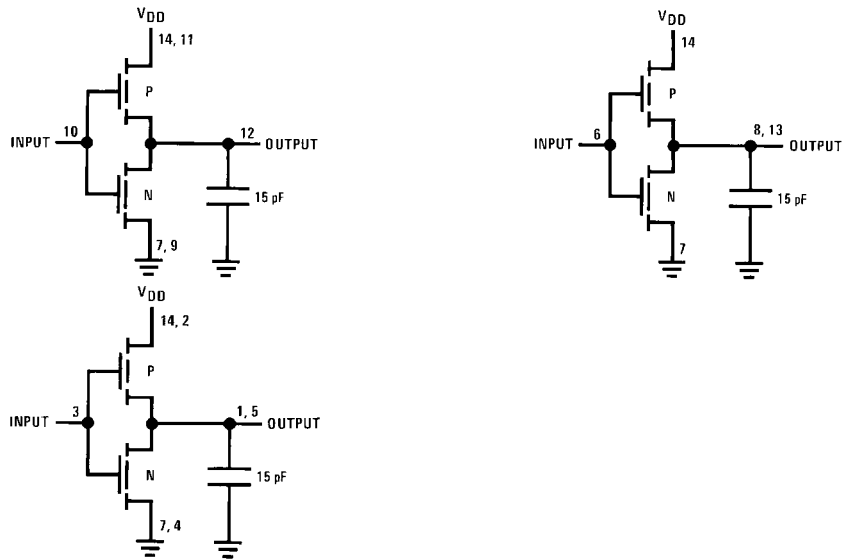
AC Electrical Characteristics (Note 2)

$T_A = 25^\circ C$ and $C_L = 15$ pF and rise and fall times = 20 ns. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/^\circ C$

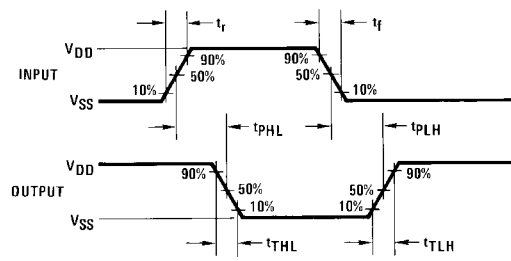
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PLH} = t_{PHL}$	Propagation Delay Time	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 20	75 50	ns
$t_{TLH} = t_{THL}$	Transition Time	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 30	100 50	ns
C_I	Input Capacitance	Any Input		5		pF

Note 2: AC Parameters are guaranteed by DC correlated testing.

AC Test Circuits



Switching Time Waveforms

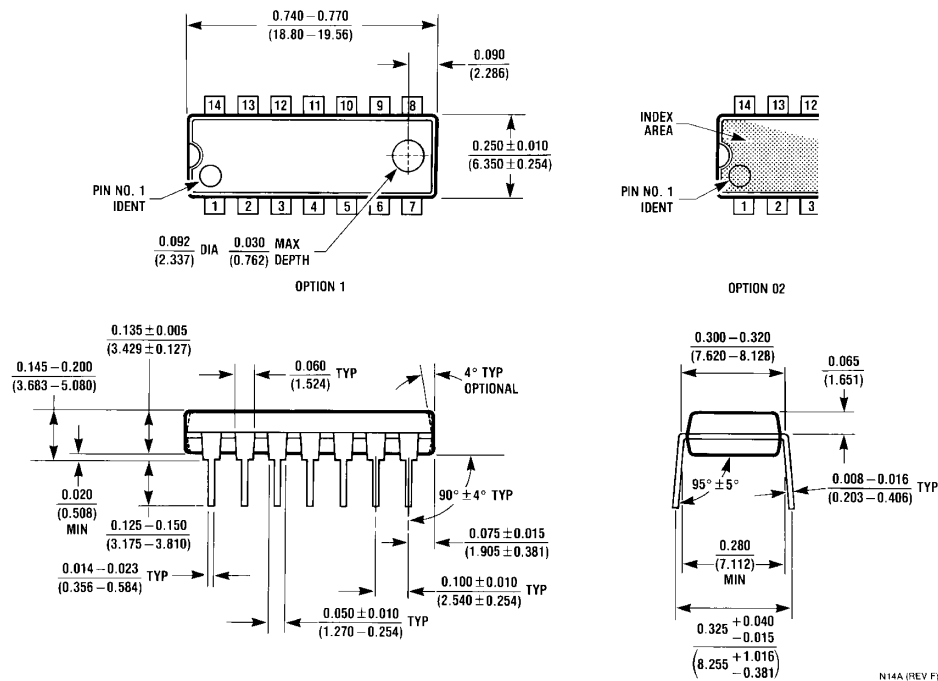


Physical Dimensions inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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