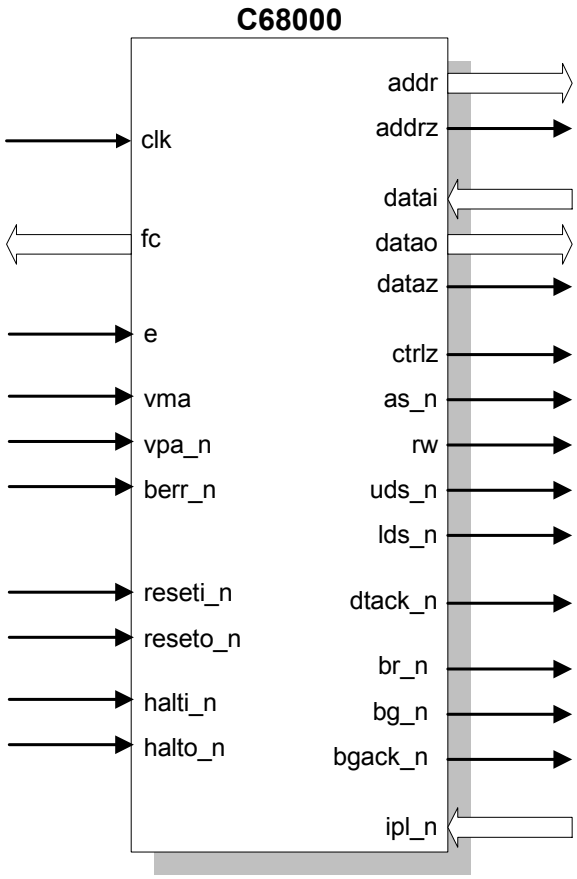
C68000
16-bit Microprocessor Megafunction

General Description

The C68000 is megafunction of a powerful 16/32-bit microprocessor and is derived from the Motorola MC68000 microprocessor. The C68000 is a fully functional 32-bit internal and 16-bit external equivalent for the MC68000. The C68000 serves interrupts and exceptions, and provides an interface for M6800 family peripherals.

The C68000 is the microcode-free design developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous without internal tri-states and with a synchronous reset.

Symbol



Features

- Control Unit
  - 16-bit two levels instruction decoder
  - Three levels instruction queue
- 55 instructions and 14 address modes
- Supervisor and User mode
  - Independent stack for both modes
- Users registers
  - Eight 32-bit data & address registers
  - 16-bit status register
- Data format
  - Integer 8, 16 or 32-bit
  - BCD packet
  - Bit
- Memory interface
  - Independent data and address buses
  - Asynchronous bus control
  - 4 GB-address space
  - 31-bit address bus (optional 32-bit)
  - 8-address spaces (used 5)
  - 16-bit data bus
- Interrupt Controller
  - Seven Priority Levels
  - Unlimited interrupt sources
  - Vectored or auto-vectored interrupt modes
- Arithmetic-Logic Unit
  - 8, 16, 32-bit arithmetic and logic operations
  - Boolean manipulations
  - 16 x 16-bit multiplication (sign or unsigned)
  - 32 / 16-bit division (sign or unsigned)
- M6800 peripherals family synchronous interface
- Two or Three wire bus arbitration interface
- Operation execution is the same for data or address registers
  - No different for operation on data or address registers

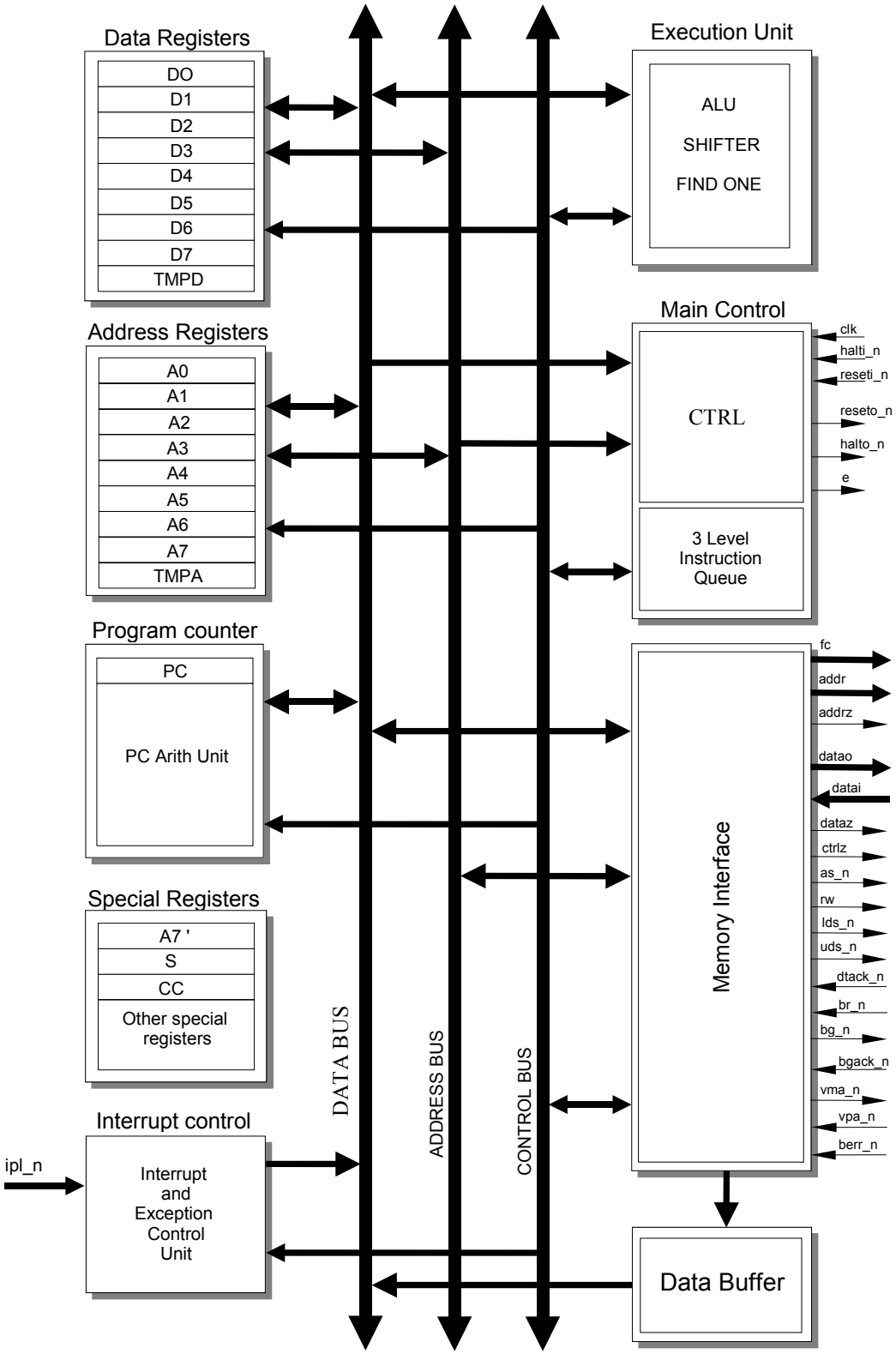
Pin Description

Name	Type	Polarity/ Bus size	Description
p0i p0o	I O	8 8	**Port 0:** is an 8-bit bi-directional I/O port with separated inputs and outputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memories.
p1i p1o	I O	8 8	**Port 1:** is an 8-bit bi-directional I/O port with separated inputs and outputs. Port 1 also serves special features.
p2i p2o	I O	8 8	**Port 2:** is an 8-bit bi-directional I/O port with separated inputs and outputs. Port 2 emits the high-order address byte during fetches from external program memory that use 16-bit addresses (MOVX @DPTR).
p3i p3o	I O	8 8	**Port 3:** is an 8-bit bi-directional I/O port with separated inputs and outputs. Port 3 also serves special features.
clk	I	Rise	**Clock:** Is an input of pulse for internal clock counters and all synchronous circuits
rtcx	I	Rise	**Timekeeping clock:** is a 32.768 kHz pulse supplies the time-base for the Real Time Clock
reset	I	High	**Hardware reset input:** A high on this pin for two clock cycles while the oscillator is running resets the device
pfi	I	High	**Power Fail Interrupt:** The input of off-megafunction voltage comparator, which generates early warning interrupt
ea	I	Low	**External Access Enable:** The 'ea' must be externally held low to enable the device to fetch code from external program memory0000H and 0FFFH. If 'ea' is held high, the device executes from in-circuit program memory unless the Program counter contains an address greater than 0FFFH.
ale	O	High	**Address Latch Enable:** The output pulse for latching the low byte of the Address during an access to external memory. In normal operations, 'ale' is driven at a constant rate of 1/6 the oscillator frequency.
psen	O	Low	**Program Store Enable:** The read strobe to external program memory. When the C68000 is executing code from the external program memory, 'psen' is activated each machine cycle, 'psen' is not activated during fetches from in-circuit program memory.
			Internal Program Memory interface:
romdatai	O	8	Memory data bus
romaddr	O	14	Memory address bus
romoe	O	High	Memory output enable
			Internal Data Memory interface:
ramdatai	I	8	Memory data bus input
ramdatao	O	8	Memory data bus output
ramaddr	O	8	Memory address bus
ramwe	O	High	Memory write enable
ramoe	O	High	Memory output enable
			External Special Function Registers interface:
sfrdatai	I	8	SFR data bus input
sfrdatao	O	8	SFR data bus output
sfraddr	O	7	SFR address bus
sfrwe	O	High	SFR write enable
sfroe	O	High	SFR output enable

Applications

- Microcomputer systems
- Embedded microcontroller systems
- Data computation and transfer
- Communication systems
- Professional audio and video

Block Diagram



Functional Description

The C68000 megafunction is partitioned into modules as shown above and described below.

Execution Unit

Arithmetic-Logic Unit. (ALU) performs:

- 32-bit arithmetic operations
- 32-bit logic operations
- Bit manipulations

Address/Data Shifter performs various types of shift and rotate operations by one bit position.

These two units with some additional logic, allows all basic operation on data and address registers.

Program counter

The program counter (PC) is 32 bits wide. This register can be incremented or loaded by the control unit during instruction execution.

Interrupt control

Provides seven priority levels of interrupt and calculates an internal vector during the auto-vector interrupt. It also holds the internal state of the interrupt and exception level.

Data registers

Contains eight 32-bit wide data registers (user visible). There is also a temporary data register that is invisible to the user.

Address registers

Contains eight 32-bit wide address registers (user visible). There is also a temporary data register that is invisible to the user.

Special registers

Contains the stack pointer, SR and additional special purpose registers.

Main control

Decodes and executes instructions. Contains main processor sequencer and control unit for all inner resources.

Interface

Manages all accesses to memory. Generates all control signals to memory and peripherals. This is a synchronous device working with both rising and falling edge of the *clk* (clock) signal.

Deliverables

- VHDL or Verilog RTL
- Post-synthesis EDIF netlist (netlist license)
- Testbench (self checking)
- Vectors for testing the megafunction
- Place & Route Scripts (netlist license)
- Synthesis and simulation scripts
- Constraint file
- Instantiation templates
- Documentation

Verification Methods

The C68000 megafunction's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Motorola MC68000 chip, and the results compared with the megafunction's simulation outputs

Device Utilization & Performance

Supported Family	Device Tested	LEs	Memory	I/O	Performance Fmax
Flex	EPF10K130-1	5823	-	60	21 MHz
Apex	EP20K160E-1	5496	-	60	29 MHz
Apex2	EP2A15C-7	5507	-	60	36 MHz
Cyclone	EP1C12C-6	6152	-	60	57 MHz
Stratix	EP1S10C-5	6560	-	60	69 MHz
Stratix-II	EP2S15C-3	4758	-	60	114 MHz

Notes:
1. Optimized for speed

Related Information

- M68000 8-/16-/32-Bit Microprocessors User's Manual Ninth Edition © Motorola Inc., 1993
- Motorola M68000 FAMILY Programmer's Reference Manual © Motorola Inc., 1992

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This megafunction developed by the processor experts at Evatronix SA