

HyperTransport-to-PCI/PCI-X Bridge

Overview

The AS90L10208 is a high performance third generation HyperTransport™-to-PCI/PCI-X bridge capable of transferring data between the HT host port and the other HT port or the PCI/PCI-X port. It is designed for bandwidth-hungry and performance-intensive applications in communications, networking, servers, and storage systems.

The next generation AS90L10208 HT-to-PCI/PCI-X bridge expands the possibilities of today's systems architects by providing HT-based design options never possible before. Each HT port operates at a frequency of up to 800 MHz DDR for both

transmit and receive directions and sustains a total aggregate bandwidth up to 25.6 Gbps per 8-bit bidirectional HT port. Each AS90L10208 HT port can be 2, 4, or 8 bits wide in both transmit and receive directions.

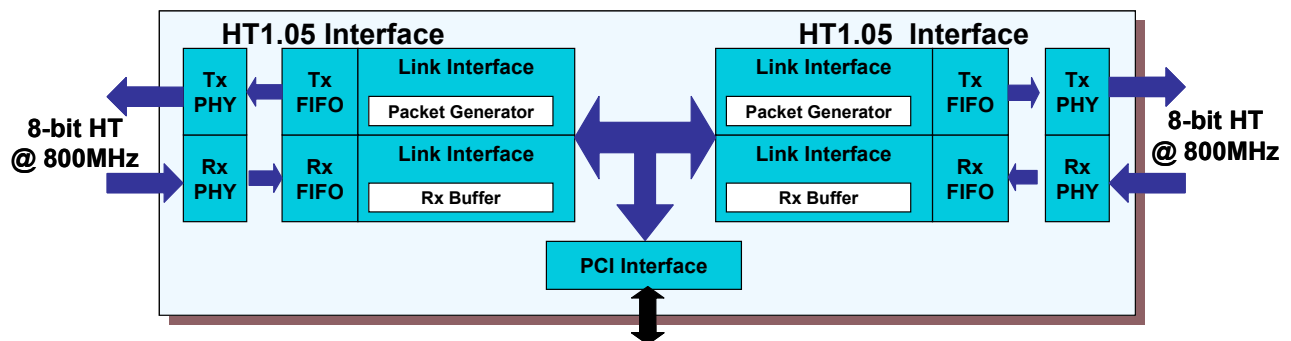
AS90L10208 supports one 64-bit, PCI/PCI-X1.0b configurable port. A fairness algorithm allocates bandwidth among devices, thereby eliminating starvation of bridges at the end of the chain. Up to 31 devices can be daisy-chained to build higher capacity systems with multiple PCI/PCI-X buses and HT-based peripherals.

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Key Features

- Two bidirectional 8-bit HyperTransport interfaces:
 - Supports 200, 300, 400, 500, 600 and 800 MHz DDR (double data rate) for peak bandwidth of 3.2GB/s per 8-bit bidirectional HT port
 - Supports dynamic frequency reprogramming
- Complies with HyperTransport 1.05 Interface Specification.
- Tunnels between the two HyperTransport interfaces.
- No protocol-induced maximum HyperTransport link length, which allows system designers to optimize speed vs. distance.
- The HT interfaces support dual-hosted chain.
- One 64-bit configurable PCI/PCI-X1.0 port:
 - 1 x 64 bit, up to 66 MHz PCI 2.2 or up to 133 MHz PCI-X 1.0b
 - 2 x 32 bit, up to 66 MHz PCI 2.2 or up to 133 MHz PCI-X 1.0b
- Complies with PCI Local Bus Specifications, Rev. 2.2
- Supports with parity and error checking features.
- Supports daisy-chaining up to 31 devices. The bandwidth is shared among the devices using a fairness algorithm.
- Built-in two-level PCI arbiter with support for up to six devices
 - Can also be configured to support an external arbiter.
- 3.3 V PCI I/O with 5 V tolerant I/Os.
- Superset register compatible with the SP1011 to leverage the same software driver
- Can be configured to emulate a single or a dual SP1011 devices
- Transaction forwarding for the following commands:
 - All I/O and memory commands
 - Type 1 to Type 1 configuration commands (downstream only)
 - Type 1 to Type 0 configuration commands (downstream only)
- Evaluation board available with firmware and software drivers.
- 1.8 V core, 1.2 V HT IO, 3.3 V PCI/PCI-X IO.
- JTAG port.

Device Block Diagram



Configurable PCI Port

- 1x 64-bit, 66MHz PCI or 133MHz PCI-X 1.0b
- 2x 32-bit, 66MHz PCI or 133MHz PCI-X 1.0b

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Summary of Benefits

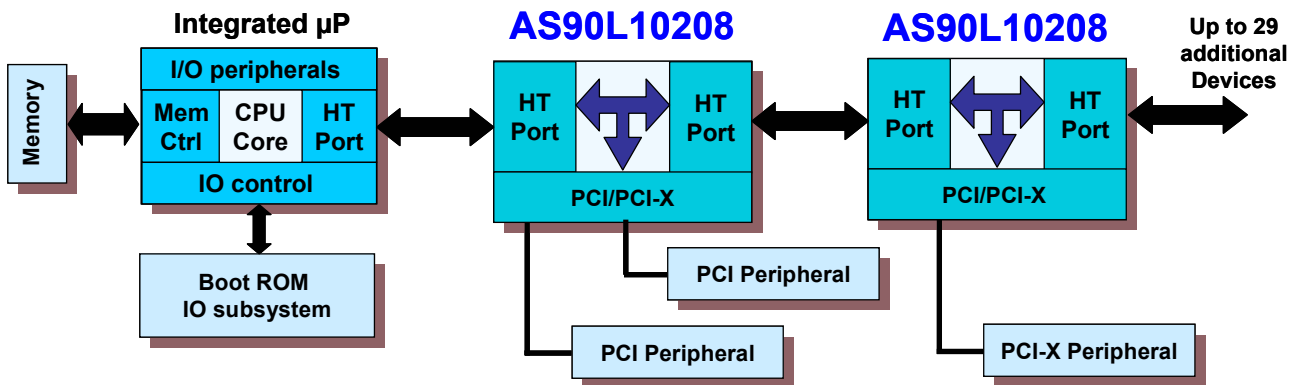
- Bridges between HyperTransport and legacy PCI and PCI-X bus, breathing new life into legacy systems, which are encumbered by the limits of traditional PCI fabrics.
- 3.2 GB/sec bandwidth supports the needs of data transfer applications.
- Host CPUs can be connected to both HT interfaces for greater system flexibility and for sharing PCI-based resources.
- Supports PCI Plug and Play capability reducing system design complexity and time to market.
- Low power consumption increases system reliability.
- Built-in PCI/PCI-X arbiter reduces system cost.
- Uses existing PCI/PCI-X drivers and firmware to reduce system development and debug time.
- 31 devices can be daisy-chained to enable a flexible and modular system implementation.
- Deterministic low latency per tunnel meets the requirements of real-time applications.

Target Applications

The feature set of the AS90L10208 makes it ideal for a variety of computing and embedded systems including:

- Enterprise LAN switches
- Storage systems and switches (SAN, NAS, RAID, FC)
- Firewalls and security gateways
- High-end computing systems
- Servers and server clusters
- Printing, graphics, and imaging Systems
- VPN switches and routers
- Edge and access routers
- MAN switches
- Wireless gateways
- Voice and multimedia access gateways
- Multiservice access concentrators
- IP service switches and core routers
- Test equipment and network probes

System Block Diagram



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