

MOS FIELD EFFECT TRANSISTOR
2SK2515

**SWITCHING
 N-CHANNEL POWER MOS FET
 INDUSTRIAL USE**

DESCRIPTION

The 2SK2515 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

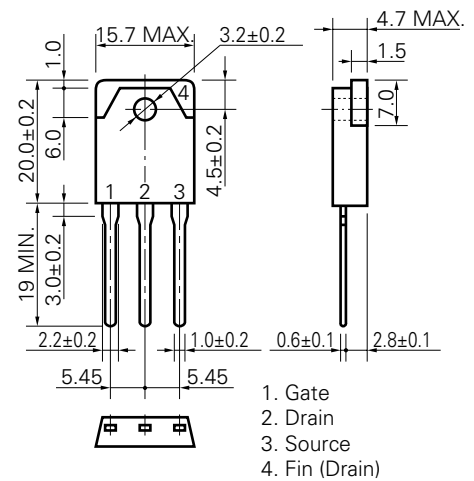
- Super Low On-Resistance
 $R_{DS(on)1} = 9\text{ m}\Omega$ ($V_{GS} = 10\text{ V}$, $I_D = 25\text{ A}$)
 $R_{DS(on)2} = 14\text{ m}\Omega$ ($V_{GS} = 4\text{ V}$, $I_D = 25\text{ A}$)
- Low C_{iss} $C_{iss} = 3\ 400\text{ pF TYP.}$
- Built-in G-S Protection Diode

ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$)

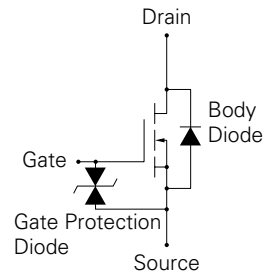
Drain to Source Voltage	V_{BSS}	60	V
Gate to Source Voltage	V_{GSS}	± 20	V
Drain Current (DC)	I_D (DC)	± 50	A
Drain Current (pulse)*	I_D (pulse)	± 200	A
Total Power Dissipation ($T_c = 25\text{ }^\circ\text{C}$)	P_{T1}	150	W
Total Power Dissipation ($T_A = 25\text{ }^\circ\text{C}$)	P_{T2}	3.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

* $PW \leq 10\ \mu\text{s}$, Duty Cycle $\leq 1\ \%$

**PACKAGE DIMENSIONS
 (in millimeter)**



MP-88

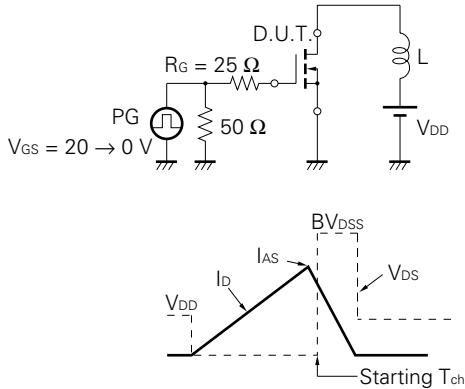


The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

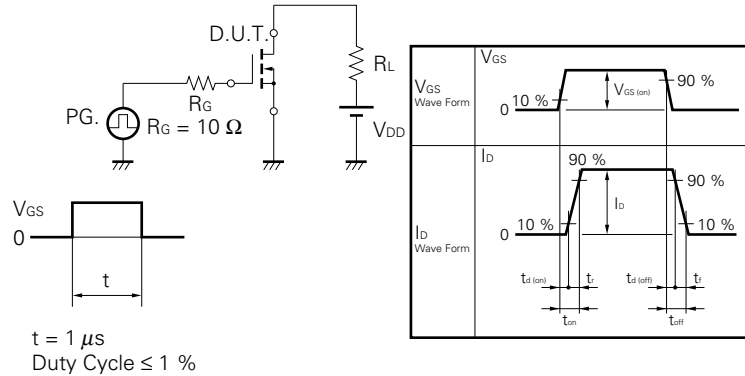
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	R _{DS (on)1}		7.3	9.0	mΩ	V _{GS} = 10 V, I _D = 25 A
Drain to Source On-Resistance	R _{DS (on)2}		11	14	mΩ	V _{GS} = 4 V, I _D = 25 A
Gate to Source Cutoff Voltage	V _{GS (off)}	1.0	1.5	2.0	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	20	58		S	V _{DS} = 10 V, I _D = 25 A
Drain Leakage Current	I _{bss}			10	μA	V _{DS} = V _{DSS} , V _{GS} = 0
Gate to Source Leakage Current	I _{gss}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0
Input Capacitance	C _{iss}		3 400		pF	V _{DS} = 10 V
Output Capacitance	C _{oss}		1 600		pF	V _{GS} = 0
Reverse Transfer Capacitance	C _{rss}		770		pF	f = 1 MHz
Turn-On Delay Time	t _{d (on)}		55		ns	I _D = 25 A
Rise Time	t _r		360		ns	V _{GS(on)} = 10 V
Turn-Off Delay Time	t _{d (off)}		480		ns	V _{DD} = 30 V
Fall Time	t _f		360		ns	R _G = 10 Ω
Total Gate Charge	Q _G		152		nC	I _D = 50 A
Gate to Source Charge	Q _{GS}		11		nC	V _{DD} = 48 V
Gate to Drain Charge	Q _{GD}		60		nC	V _{GS} = 10 V
Body Diode Forward Voltage	V _{F (S-D)}		0.92		V	I _F = 50 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		105		ns	I _F = 50 A, V _{GS} = 0
Reverse Recovery Charge	Q _{rr}		265		nC	di/dt = 100 A/μs

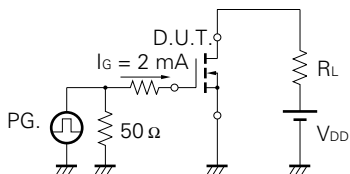
Test Circuit 1 Avalanche Capability



Test Circuit 2 Switching Time

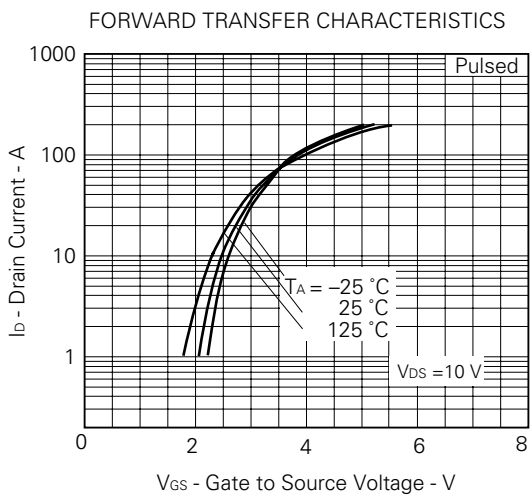
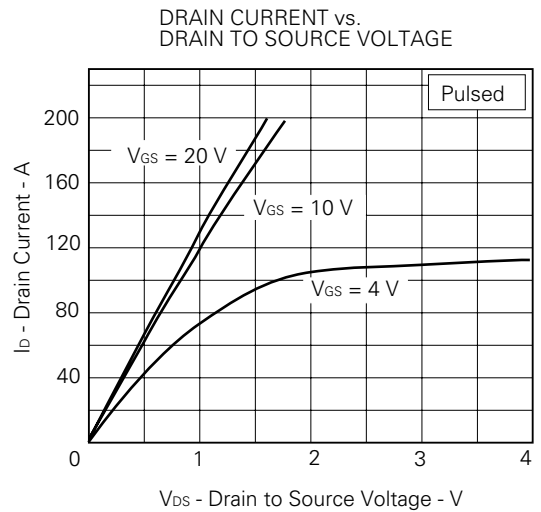
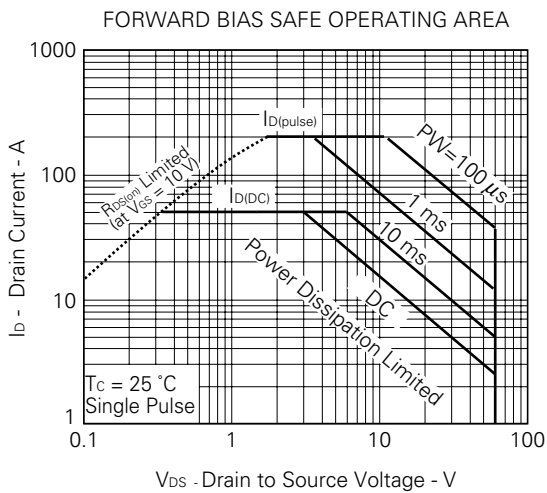
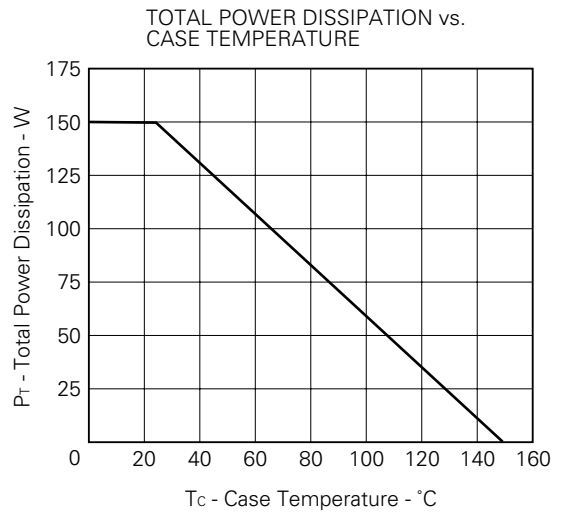
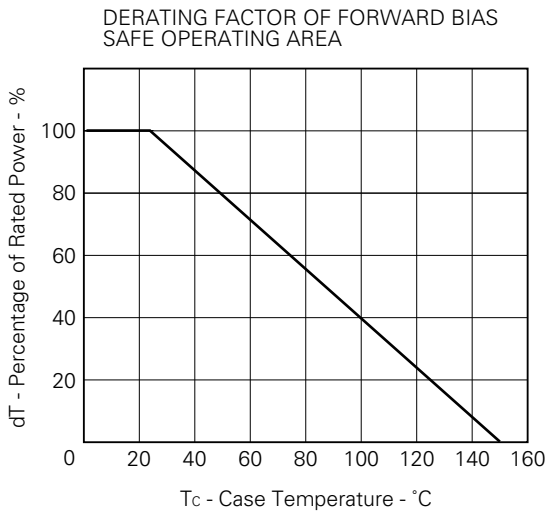


Test Circuit 3 Gate Charge

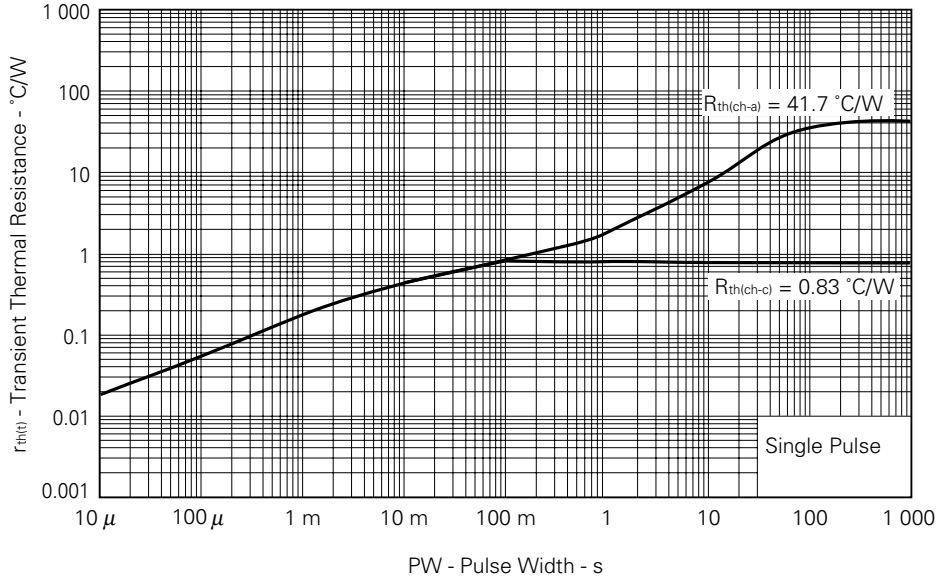


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

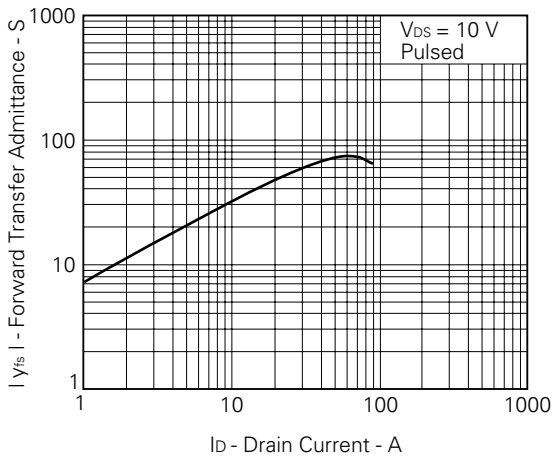
TYPICAL CHARACTERISTICS (T_A = 25 °C)



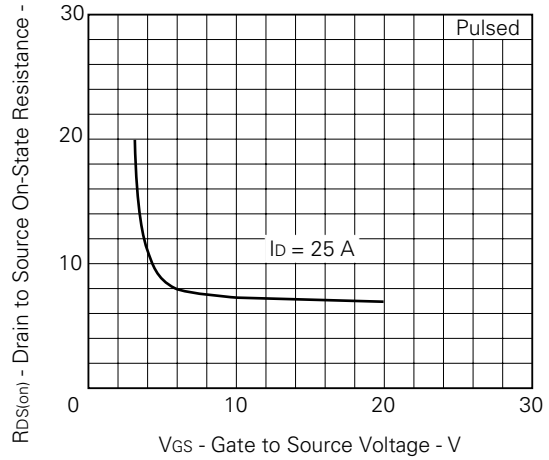
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



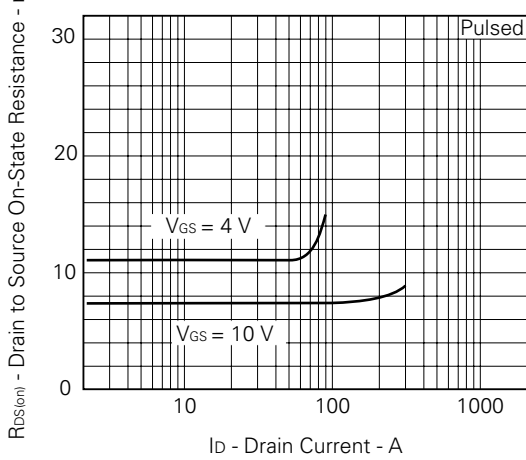
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



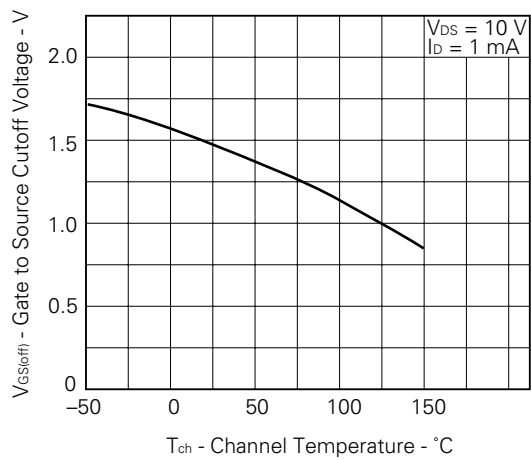
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

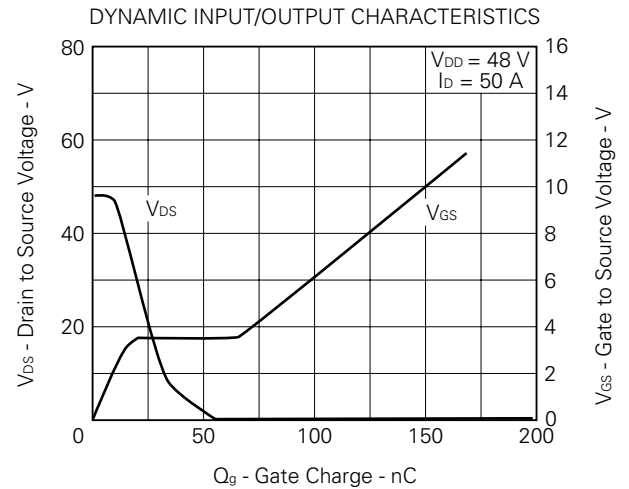
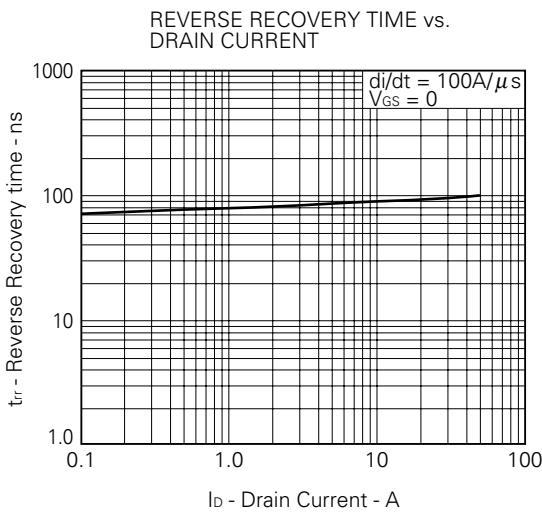
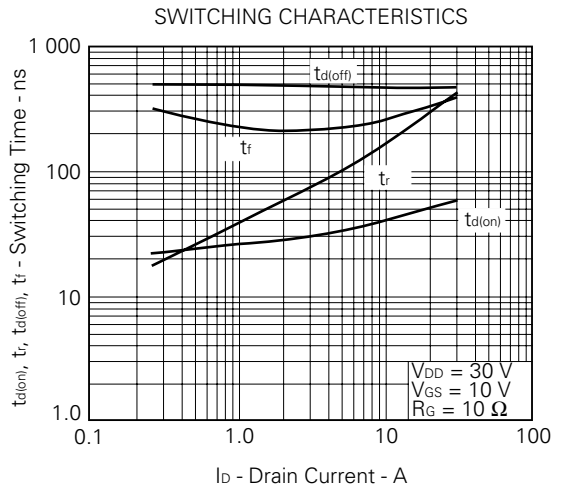
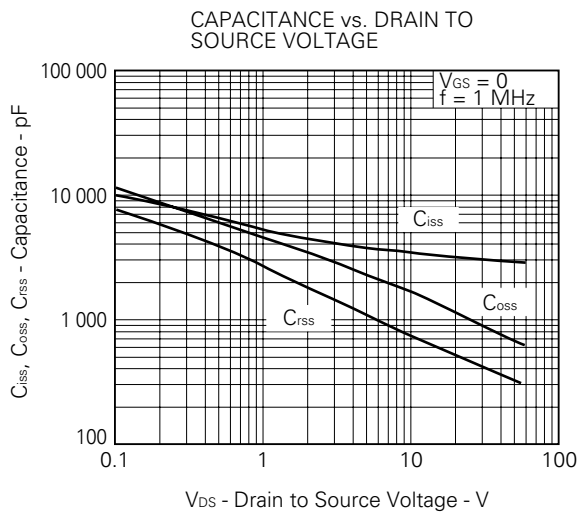
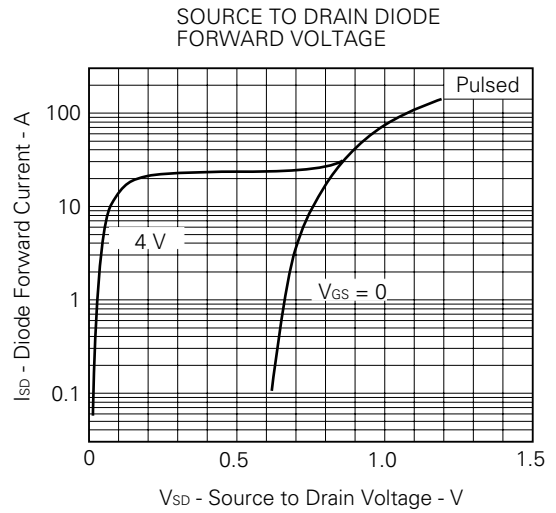
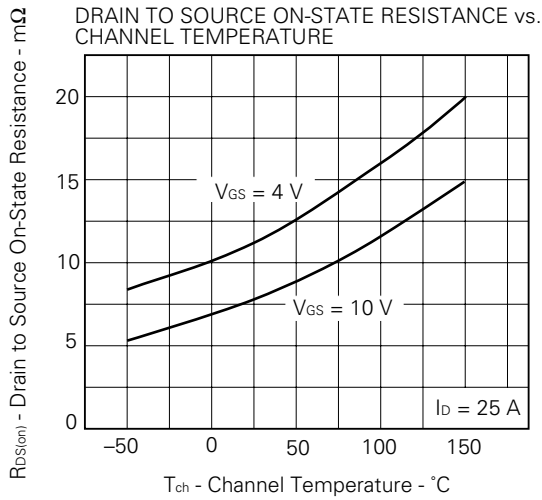


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

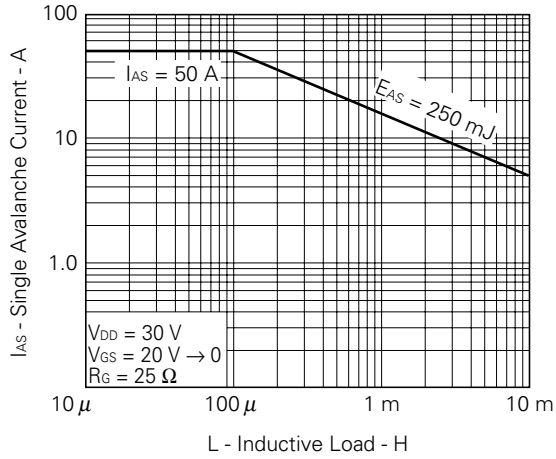


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

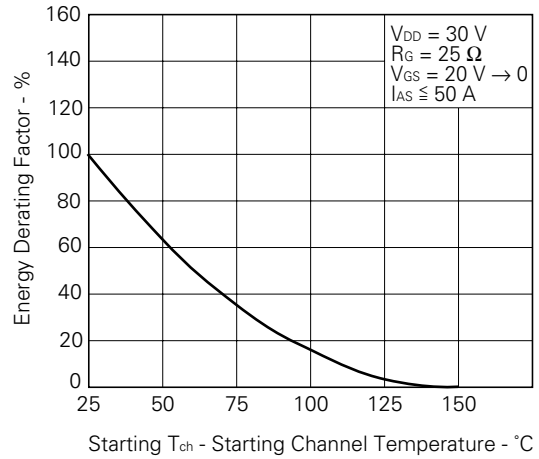




SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

[MEMO]

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Anti-radioactive design is not implemented in this product.