

PRELIMINARY
REFERENCE DESIGN
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PM73123 AAL1GATOR-8
PM4354 COMET-QUAD

ISSUE 2

AAL1GATOR-8 REFERENCE DESIGN

PM73123

AAL1GATOR-8

REFERENCE DESIGN

PRELIMINARY

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1 INTRODUCTION

The AAL1gator-8 Reference Design assists customers in designing a Circuit Emulation Service (CES) and/or a Dynamic Bandwidth Circuit Emulation Service (DBCES) card. The CES/DBCES card is used to emulate circuit oriented transmission characteristics to support Constant Bit Rate (CBR) traffic.

1.1 PURPOSE

This reference design will assist engineers in designing their products using PMC-Sierra's AAL1gator-8, COMET and COMET-QUAD devices thereby bringing customers' designs to market earlier.

1.2 SCOPE

This document is a paper reference design and describes the scope and deliverables required for the AAL1gator-8 Reference Design. Note that the design was not actually built and tested, but has only been designed on paper.

This reference design is a modularized card with two design options:

1. AAL1gator-8, two COMET-QUADs, a microprocessor interface, and line interfaces.
2. AAL1gator-8, eight COMETs, a microprocessor interface, and line interfaces.

A block diagram is shown for the two designs. Descriptions are provided for each of the functional blocks and detailed implementation descriptions then follow.

1.3 APPLICATIONS

Emulating existing TDM circuits is an essential function for ATM switches. Currently TDM circuits provide most voice and data services and therefore seamless interaction between TDM and ATM has become a system requirement. The ATM Forum has standardized an internetworking function that satisfies this requirement called the Circuit Emulation Services (CES) Specification.

The following are some application examples of the AAL1gator-8 Reference Design:

- An 8-Link T1/E1 CES Cards in a PBX

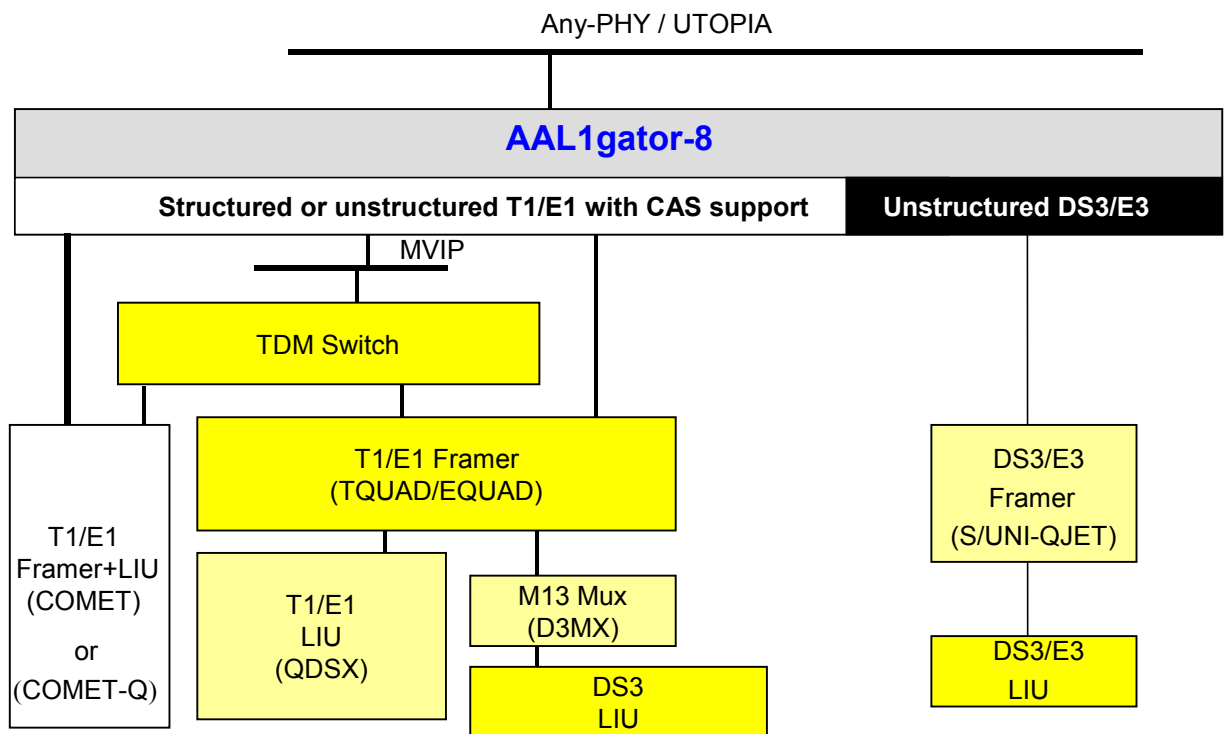
- TDM to ATM Access Service Concentrator
- Part of a TDM to ATM Multiservice ATM Switch

2 GENERAL DESCRIPTION

2.1 AAL1gator-8 Architecture

The purpose of the AAL1gator-8 is to provide high density T1/E1, or DS3/E3/J2 line interfaces access to an AAL1 CBR ATM network. The AAL1gator-8 can support 8 T1/E1 lines, 1 DS3/E3/STS-1 link or 2 8Mbps H-MVIP links. The AAL1gator-8 is capable of supporting 256 VCs. On the system side, the AAL1gator-8 supports a standard UTOPIA Level 2 interface that optionally supports parity and runs up to 52 MHz. An optional 8/16-bit Any-PHY slave interface and UTOPIA Level 1 master/slave interface are also supported on the system side. Figure 1 indicates the ways in which an AAL1gator-8 can be used to connect to T1/E1 or DS3/E3 line interfaces.

Figure 1 AAL1gator-8 Configurations



Figures 2 and 3 show the system context in which the AAL1gator-8 devices reside within the reference designs. In these designs each AAL1gator-8 can interface with eight COMETs or two COMET-QUADs to support 8 structured/unstructured T1s or E1s.

The PM4351 COMET is a single channel combined E1/T1 transceiver and framer, and the PM4354 COMET-QUAD is a four channel combined E1/T1 transceiver and framer – both devices are capable for use in long and short haul T1, J1 and E1 systems with a minimum of external circuitry. When used with the COMETs or COMET-QUADs, AAL1gator-8 can be part of a multiservice switch application which can provide circuit emulation services on E1 or T1 pipes.

Figure 2 AAL1gator-8 and COMETs

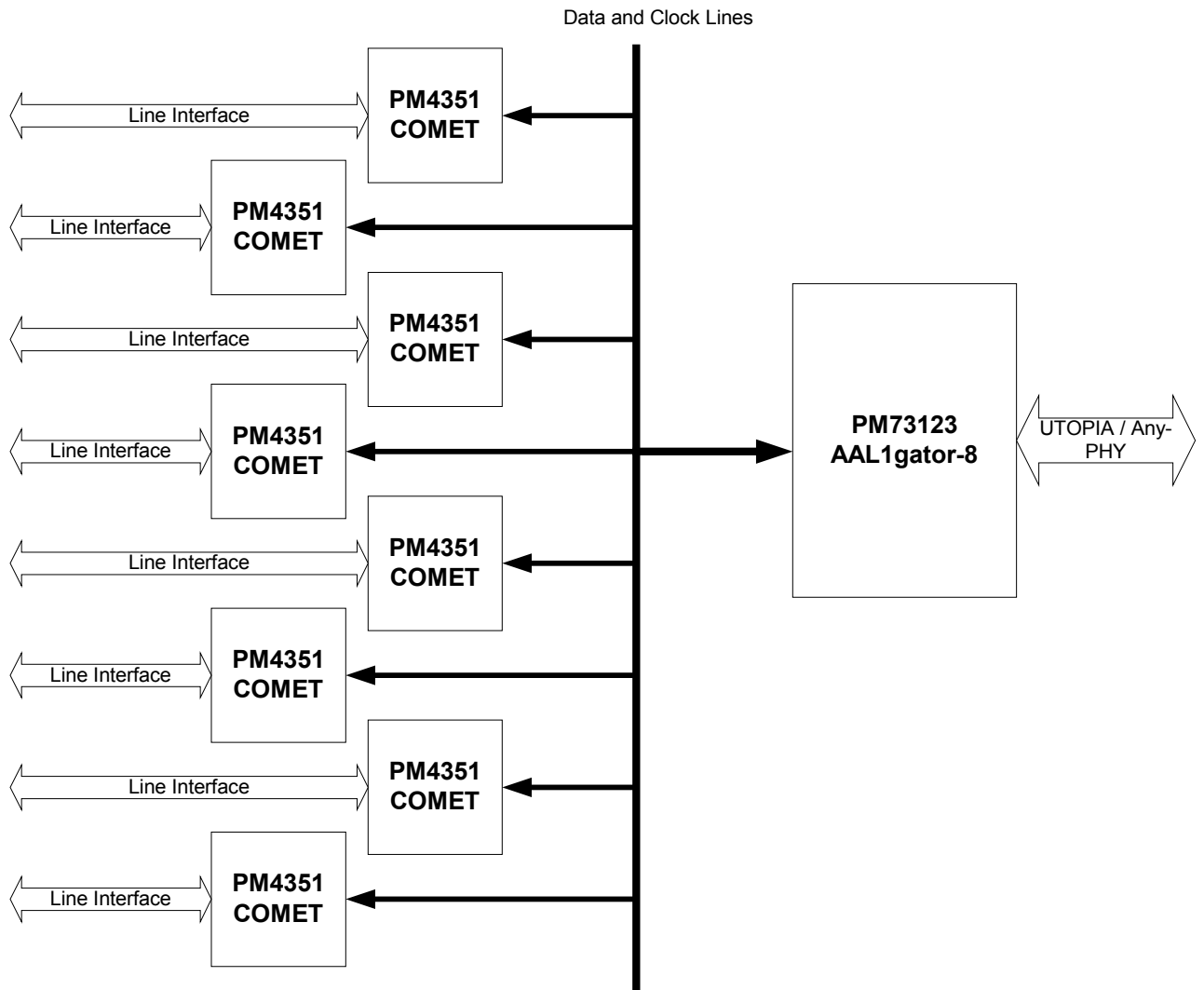
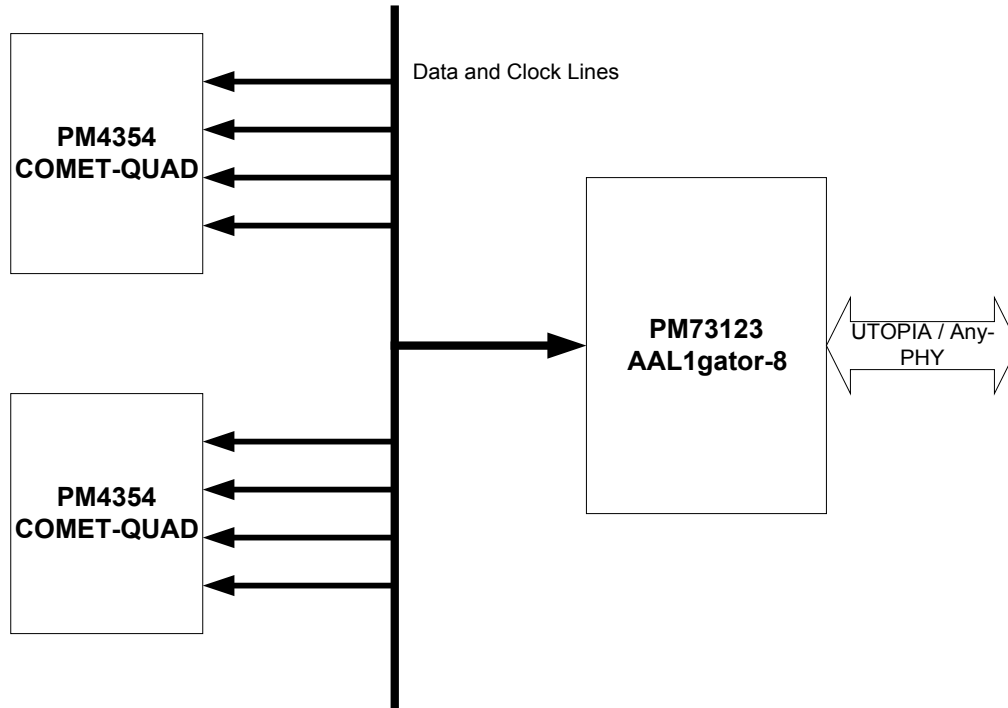


Figure 3 AAL1gator-8 and COMET-QUADs



The COMETs or COMET-QUADs receive data through the T1/E1 line interfaces. The formatted data is then passed through the T1/E1 framers to the AAL1gator-8 for CBR servicing. The cells are then routed through a UTOPIA L2 connector for routing, switching, traffic policing and shaping.

In the transmit path, the AAL1gator-8 receives the ATM cells from the UTOPIA bus. The AAL1gator-8 retrieves the data and signaling information, and places the data to be transmitted over the T1 or E1 lines via the COMETs or COMET-QUADs in the appropriate port and time slot.

3 FEATURES

- Implementation strategy for the AAL1gator-8 in a Multi Service Access Concentrator environment using the PM4351 COMET and PM4354 COMET-QUAD.
- Supports 8 T1/E1 rates and channelized mode.
- Supports a CES.
- Supports independently clocked links.
- Has a microprocessor interface for configuration and monitoring.

4 HIGH LEVEL DESIGN

The block diagrams of the AAL1gator-8 reference design are shown in Figure 4 and Figure 5. Figure 4 illustrates the high level design of the reference design with 8 COMET devices while Figure 5 shows the high level design with two COMET-QUAD devices.

Figure 4 AAL1gator-8 Ref Design Block Diagram with COMETs

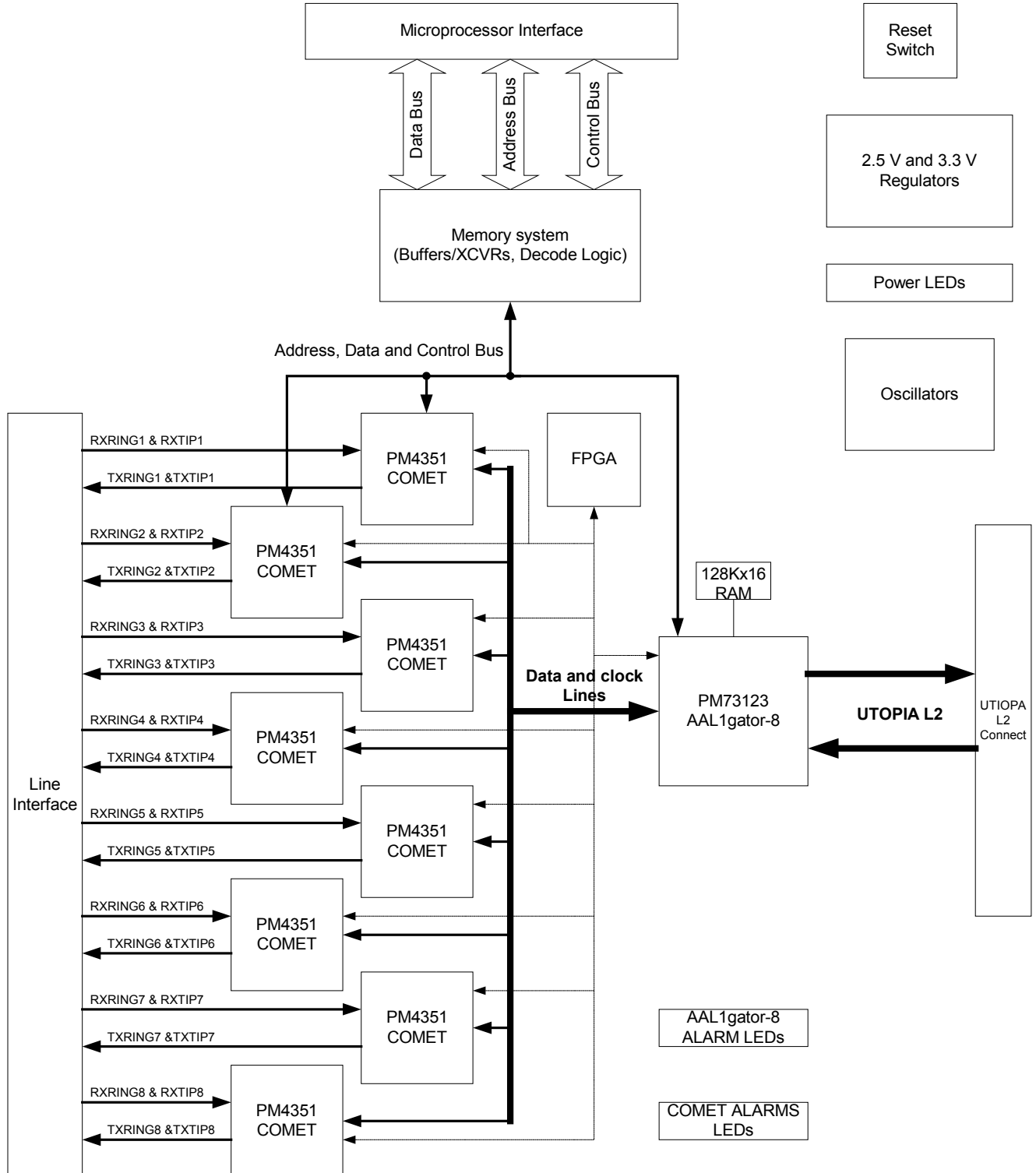
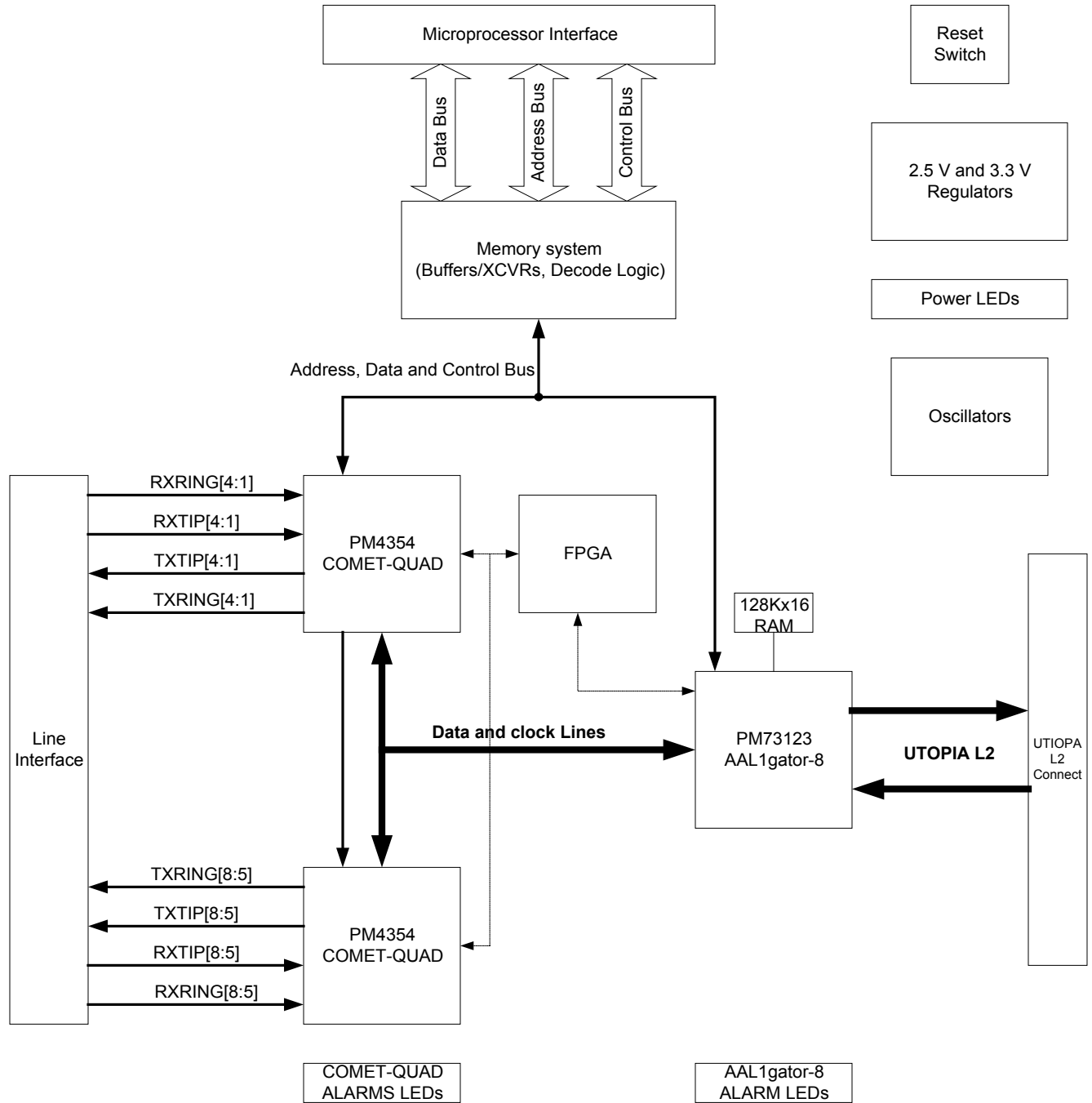


Figure 5 AAL1gator-8 Ref Design Diagram with COMET-QUADs



As illustrated, the designs contain the following functional blocks:

1. PM73123 AAL1gator-8
2. PM4351 COMET/PM4354 COMET-QUAD
3. Microprocessor and Memory System Interface
4. Field Programmable Gate Array (FPGA)
5. Line Interface
6. UTOPIA Interface
7. Power and Clock Sources

The hardware allows full access to the AAL1gator-8 and COMET/COMET-QUAD devices via the microprocessor interface. Each COMET device acts as a single line interface unit with the integrated long haul LIU, and a T1/E1 framer/de-framer while each COMET-QUAD device acts as four line interface units with the integrated long haul LIUs, and T1/E1 framers/de-framers.

In the receive path (from a T1 or E1 line), a COMET or COMET-QUAD converts the incoming line data (in the form of channels) to a serial bit stream. The AAL1gator-8 then receives this data and clocking information and builds AAL1 cells to be sent to the UTOPIA bus.

In the transmit path (to a T1 or E1 line), the AAL1gator-8 receives the ATM cells from the UTOPIA bus. The AAL1gator-8 retrieves the data and signaling information, and places the data to be transmitted over the T1 or E1 lines via the COMETs/COMET-QUADs in the appropriate port and time slot.

As illustrated in both Figure 4 and Figure 5, the connections from the FPGA to the PMC's devices are dotted lines. This is because it is possible to connect the AAL1gator-8 to the COMETs or COMET-QUADs directly (i.e. without using a FPGA). Figure 6 shows the direct connection between the AAL1gator-8 and COMETs while Figure 7 illustrates this glueless interconnection between AAL1gator-8 and COMET-QUADs.

Figure 6 Glueless AAL1gator-8 to COMETs Connection

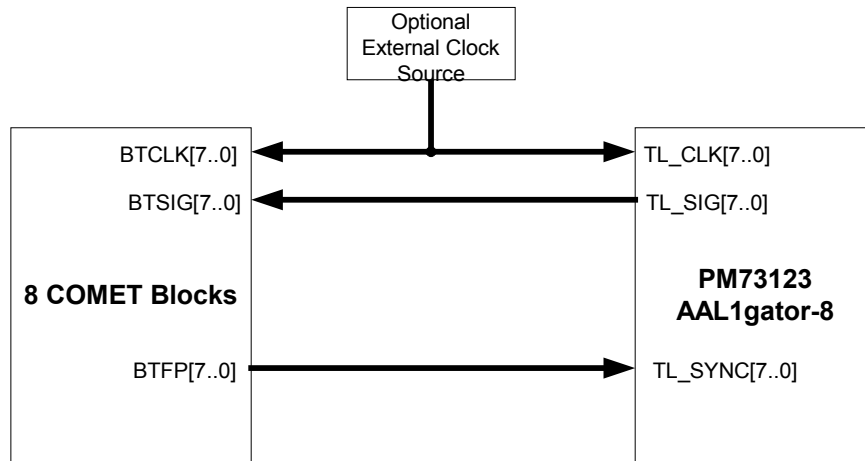
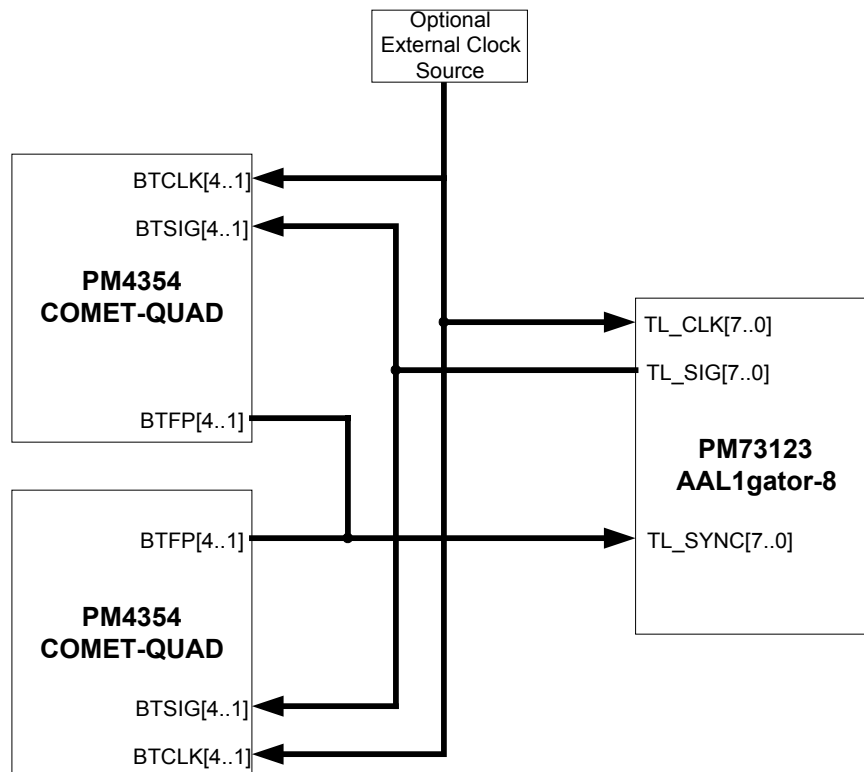


Figure 7 Glueless AAL1gator-8 to COMET-QUADs Connection



The AAL1gator-8 also supports 8Mbit/s H-MVIP on the line interface, and the COMET-QUAD also supports 8Mbit/s H-MVIP on the system interface.

Therefore, an H-MVIP interface is optionally provided for the AAL1gator-8 with COMET-QUAD Reference design.

The main purpose of the FPGA is to provide maximum clock distribution flexibility by allowing for independently clocked links. The AAL1gator-8 is capable of implementing SRTS and the Adaptive Clock Recovery algorithm on its own; however, using an FPGA it is possible to implement an external Adaptive Clock Recovery scheme or SRTS clock scheme. The FPGA is also used for the generation of TL_CLK (AAL1gator-8) and BTCLK (COMET and COMET-QUAD). In addition, the FPGA generates an appropriate signal for the AAL1gator-8 network clock pin, N_CLK, (at 2.43 MHz), and also distributes XCLK signals to the 8 COMET or two COMET-QUAD devices from only two clock oscillators: 1.544 MHz and 2.048 MHz.

In H-MVIP mode, the FPGA is used to distribute the 16.384 MHz clock to the AAL1gator-8's C16B and to the COMET-QUADs' CMV8MCLK input pins. The FPGA is also used to distribute the 4.096 MHz Frame Pulse Clock to the AAL1gator-8's C4B and to the COMET-QUADs' CMVPFC inputs, and to generate the 8 kHz Common H-MVIP Frame Pulse from the Frame Pulse Clock.

In addition, in both Figures 6 and 7, the TL_SYNC pins of the AAL1gator-8 are connected to the COMET BTFP pin or the COMET-QUAD BTFP pins (configured as outputs). Depending on the value of MF_SYNC_MODE in the LI_CFG_REG register of the AAL1gator-8 for the line, this allows for alignment of signaling bits on multiframe boundaries or a frame boundary.

Power requirements of the boards are +5.0V, +3.3V and +2.5V. The AAL1gator-8 and COMET-QUADs require +3.3V and +2.5V while COMETs require only +3.3V. +5.0V is used as input to the COMETs' BIAS pins and to generate the +3.3V and +2.5V using voltage regulators.

In this reference design, the AAL1gator-8, COMET and COMET-QUAD devices are configured with de-multiplexed microprocessor address and data bus. The microprocessor interface has been provided through a 96-pin connector. This interface provides configuration and monitoring for PMC-Sierra's devices.

The memory sub-unit of the AAL1gator-8's block contains a 128k x 16 SRAM module connected to the AAL1gator-8 device's RAM interface.

Two 80-pin female UTOPIA connectors carry the receive and transmit UTOPIA signals between the AAL1gator-8 and an external PHY board or a Parallel Cell Traffic Generator and Analyzer.

The designs also include several LED circuits for the device alarms and power indications.

5 BLOCK DESCRIPTION

5.1 AAL1gator-8

The AAL1 Segmentation and Reassembly (SAR) Processor (AAL1gator-8) is a monolithic single chip device that provides DS1, E1, E3, or DS3 line interface access to an ATM Adaptation Layer One (AAL1) Constant Bit Rate (CBR) ATM network. It arbitrates access to an external (128K x 16/18 bits) 10ns SRAM for storage of the configuration, the user data, and the statistics. Some of the device's important functionality is as follows:

- Compliant with the ATM Forum's Circuit Emulation Services (CES) specification (AF-VTOA-0078), and the ITU-T I.363.1
- Supports Dynamic Bandwidth Circuit Emulation Services (DBCES). Compliant with the ATM Forum's DBCES specification (AF-VTOA-0085).
- Supports idle channel detection via processor intervention, CAS signaling, or data pattern detection.
- Provides idle channel indication on a per channel basis.
- Provides AAL1 segmentation and reassembly of 8 individual E1 or T1 lines, 2 H-MVIP lines at 8Mbit/s, or 1 E3 or DS3 line.
- Provides a standard 16/8 bits UTOPIA level 2 Interface which optionally supports parity and runs up to 50 MHz. The following modes are supported:
 - 16-bit Level 2, Multi-Phy Mode (MPHY)
 - 8-bit Level 2, MPHY
 - 8-bit Level 1, SPHY
 - 8-bit Level 1, ATM Master
- Supports up to 256 Virtual Channels (VC).

The AAL1gator-8 is configured, controlled and monitored via a generic 8-bit microprocessor bus through which all internal registers are accessed. All sources of interrupts can be masked and acknowledged through the microprocessor interface.

In this reference design, the AAL1gator-8 is configured with the direct mode at the line interface to connect to 8 COMETs or 2 COMET-QUADs. The line mode of operation needs to be setup from hardware reset and cannot be changed once the chip is powered up. The line mode is controlled by the AAL1gator-8's LINE_MODE pin. When the LINE_MODE pin is set to low using the provided jumpers the AAL1gator-8 will support 8 low speed lines, or one high speed line, to interface with the COMET or COMET-QUAD devices. When the LINE_MODE pin is set to high, the AAL1gator-8 will be in H-MVIP mode when interfacing to the COMET-QUADs. This mode is provided as an extra and optional interface and can be ignored.

The UTOPIA interface of the AAL1gator-8 will power up with all outputs tri-stated and will remain tri-stated until the UI_EN bit in the UI_COMN_CFG register is set.

Also, during the hardware configuration of the AAL1gator-8, the TL_CLK_OE signal is tied high to use the clock provided on its RL_CLK pin as its TL_CLK and will drive this clock externally.

When the chip is taken out of hardware reset, the internal DLL on SYSCLK, which used to maintain low skew on the RAM interface, will go into hunt mode and will adjust the internal SYSCLK until it aligns with the external SYSCLK. The microprocessor should poll the RUN bit in the DLL_STAT_REG register until this bit is set. At this point, the entire chip with the exception of the microprocessor interface and the DLL are in reset. Before any configuration can be done, including accessing the RAM, the chip must be taken out of software reset by clearing the SW_RESET bit in the DEV_ID_REG register. Then, the RAM should be cleared to all zeros. At this point, the A1SP block is still in reset because its SW_RESET bit in the CMD_REG register is still set. The line interface is configured in the direct low speed mode indicated by the LINE_MODE pins but all internal registers are in the reset state. The line interface is out of reset at this point but will only be driving data as if all lines and/or queues are disabled. The UTOPIA interface, as mentioned above, is disabled and all UTOPIA outputs are tri-stated.

The software configuration of the AAL1gator-8 is done in three steps:

1. Line Configuration: while the A1SP is in reset, the memory mapped registers which contain the line configuration (the LIN_STR_MODE and HS_LIN_REG registers) can be initialized. Then, the CMD_ATTN bit in the CMD_REG register can be set so that the A1SP can read its configuration. The SW_RESET bit of the CMD_REG register should remain set.
2. Queue Configuration: the SW_RESET bit in the CMD_REG register is cleared which takes A1SP out of reset. The R_CHAN_2_QUE_TBL will then

begin a 640 SYSCLK cycle initialization, which reset each timeslot to playing out conditioned data. At this point, the queues can be initialized as needed.

3. Adding Queues: By setting the corresponding bits in the ADDQ_FIFO register, the queues are added.

For a more detailed description of the AAL1gator-8, please refer to [1].

5.2 COMET

The PM4351 Combined E1/T1 Transceiver (COMET) is a feature-rich monolithic integrated circuit suitable for use in long haul and short haul T1 and E1 systems with a minimum of external circuitry. The COMET is software configurable, allowing feature selection without changes to external wiring.

Analog circuitry is provided to allow direct reception of long haul E1 and T1 compatible signals with up to 36 dB cable loss (at 1.024MHz in E1 mode) or up to 36 dB cable loss (at 772 kHz in T1 mode) using a minimum of external components. Typically, only line protection, a transformer and a line termination resistor are required. Digital line inputs are provided for applications not requiring a physical T1 or E1 interface.

The COMET recovers clock and data from the line and frames to incoming data. In T1 mode, it can frame to several DS-1 signal formats: SF, ESF, T1DM (DDS) and SLC®96. In E1 mode, the COMET frames to basic G.704 E1 signals and CRC-4 multiframe alignment signals, and automatically performs the G.706 interworking procedure. AMI, HDB3 and B8ZS line codes are supported.

In T1 mode, the COMET generates framing for SF, ESF and T1DM (DDS) formats. In E1 mode, the COMET generates framing for a basic G.704 E1 signal. The signaling multiframe alignment structure and the CRC multiframe structure may be optionally inserted. Framing can be optionally disabled.

Internal analog circuitry allows direct transmission of long haul and short haul T1 and E1 compatible signals using a minimum of external components. Typically, only line protection, a transformer and a line termination resistor are required. Digitally programmable pulse shaping allows transmission of DSX-1 compatible signals up to 655 feet from the cross-connect, E1 short haul pulses into 120 ohm twisted pair or 75 ohm coaxial cable, E1 long haul pulses into 120 ohm twisted pair as well as long haul DS-1 pulses into 100 ohm twisted pair with integrated support for LBO filtering as required by the FCC rules. In addition, the programmable pulse shape extending over 5-bit periods allows customization of short haul and long haul line interface circuits to application requirements. Digital line inputs and outputs are provided for applications not requiring a physical T1 or E1 interface.

The COMET provides both a parallel microprocessor interface for controlling the operation of the device and serial PCM interfaces that allow backplane rates from 1.544 Mbit/s to 8.192 Mbit/s to be directly supported.

In this reference design, each COMET interfaces with the AAL1gator-8 can be configured independently in T1 or E1 mode. After the power up or a hardware/software reset, the following steps are performed to configure the COMET:

1. Initialize the XLPG (Transmit Pulse Template) registers to clear the pulse template.
2. Setup the XLPG to program the pulse template to generate short-haul or long-haul pulses as specified in [2]. Also, set the amplitude of the pulse template and enable the XLPG.
3. Program the COMET for T1 or E1 mode by writing to the E1/T1B bit of the Global Configuration register.
4. Configure the Clock Synthesis Unit (CSU) by selecting 1.544MHz or 2.048MHz for the line rate (XCLK and TCLKO).
5. Configure the Clock and Data Recovery Unit (CDRC) to receive the appropriate line decoding (AMI or B8ZS in T1 mode, HDB3 in E1 mode).
6. Configure the Receive and Transmit Elastic Stores units (RX-ELST and TX-ELST).
7. Set the framing format and line encoding for the transmitter (XBAS in T1 mode, E1-TRAN in E1 mode).
8. Program the framing format for the receiver.
9. Configure the framing format and the data rate for the facility data link.
10. Configure the Signaling Extraction Block register (SIGX).
11. Configure the Receive Line Interface (RLPS).
12. Configure the Transmit/Receive Jitter Attenuator and the Receive Option registers to disable or enable the jitter attenuation on transmit or receive line side.
13. Configure the Backplane Receive System Interface (BRIF) block (registers 0x30 and 0x31):

- Full Frame mode
- BRCLK as an output
- BRPCM, BRSIG, and BRFP updated on the rising edge of BRCLK
- BRCLK backplane rate (1.544MHz or 2.048MHz)
- BRFP (Backplane Frame Pulse) as an output

14. Configure the Backplane Transmit System Interface (BTIF) block (registers 0x40 and 0x41):

- Full Frame mode
- BRCLK as an input
- BTPCM, BTSIG, and BTFP updated on the rising edge of BTCLK
- BTCLK backplane rate (1.544MHz or 2.048MHz)
- BRFP (Backplane Frame Pulse) as an output

15. Program the Receive Line Equalization table as stated in [2].

For more information about the COMET please refer to [2].

5.3 COMET-QUAD

The PM4354 Four Channel Combined E1/T1/J1 Transceiver and Framer (COMET-QUAD) is a feature-rich monolithic integrated circuit suitable for use in long haul and short haul T1, J1 and E1 systems with a minimum of external circuitry. The COMET-QUAD is software configurable, allowing feature selection without changes to external wiring.

Analog circuitry is provided to allow direct reception of long haul E1 and T1/J1 compatible signals typically with up to 43 dB cable loss at 1024 kHz (E1) and up to 44 dB cable loss at 772 kHz (T1/J1) using a minimum of external components. Typically, only line protection, a transformer and a line termination resistor are required.

The COMET-QUAD recovers clock and data from the line and frames to incoming data. In T1 mode, it can frame to SF and ESF signal formats. In E1

mode, the COMET-QUAD frames to basic G.704 E1 signals and CRC-4 multiframe alignment signals, and automatically performs the G.706 interworking procedure. AMI, HDB3 and B8ZS line codes are supported.

In T1 mode, the COMET-QUAD generates framing for SF and ESF formats. In E1 mode, the COMET-QUAD generates framing for a basic G.704 E1 signal. The signaling multiframe alignment structure and the CRC multiframe structure may be optionally inserted. Framing can be optionally disabled.

Internal analog circuitry allows direct transmission of long haul and short haul T1 and E1 compatible signals using a minimum of external components. Typically, only line protection, a transformer and a line termination resistor are required. Digitally programmable pulse shaping allows transmission of DSX-1 compatible signals up to 655 feet from the cross-connect, E1 short haul pulses into 120 ohm twisted pair or 75 ohm coaxial cable, E1 long haul pulses into 120 ohm twisted pair as well as long haul DS-1 pulses into 100 ohm twisted pair with integrated support for LBO filtering as required by the FCC rules. In addition, the programmable pulse shape extending over 5-bit periods allows customization of short haul and long haul line interface circuits to application requirements.

Serial PCM interfaces to each T1 framer allow 1.544 Mbit/s backplane receive/backplane transmit system interfaces to be directly supported. Tolerance of gapped clocks allows other backplane rates to be supported with a minimum of external logic.

In synchronous backplane systems 8Mbit/s H-MVIP interfaces are provided for access channel associated signaling (CAS) and common channel signaling (CCS) for each T1 or E1. The DS0 data channel H-MVIP and CAS H-MVIP access is multiplexed with the serial PCM interface pins. The CCS signaling H-MVIP interface is independent of the DS0 channel and CAS H-MVIP access. The use of any of the H-MVIP interfaces requires that common clocks and frame pulse be used along with T1/E1 slip buffers.

The COMET-QUAD is configured, controlled and monitored via a generic 8-bit microprocessor bus through which all internal registers are accessed. All sources of interrupts can be masked and acknowledged through the microprocessor interface.

Please refer to [3] for more information about the COMET-QUAD.

5.4 The Microprocessor Interface Block

The microprocessor interface contains de-multiplexed address and data buses and a control bus to perform the following functions on the AAL1gator-8 Reference Design:

- Configuration of the AAL1gator-8 and COMET or COMET-QUAD devices
- Monitoring of alarms and interrupts in the AAL1gator-8 and COMET or COMET-QUAD devices

In order to provide maximum system implementation flexibility, a particular microprocessor has not been specified. However, the system microprocessor must have the following minimum capabilities:

1. 23 bit address bus
2. 6 bit data bus
3. 3 programmable chip selects
4. 2 independent interrupt request lines

An example of a microprocessor that meets these minimum requirements is the Motorola MC68340. Another option would be to implement the design in a PCI or compact PCI system.

5.5 AAL1gator-8 to COMET/COMET-QUADs Interconnections

The AAL1gator-8 communicates with the COMET/COMET-QUAD devices via framer bus signals listed in Table 1. Four bits of each signal group connects to one COMET-QUAD device. For instance, TL_SYNC[3..0] are connected to the COMET-QUAD 1, while TL_SYNC[7..4] are connected to COMET-QUAD 2.

Table 1 AAL1gator-8 to COMET/COMET-QUAD Connections

SIGNAL	DESCRIPTION
TL_SYNC[7..0]	The FPGA generates this signal for both the AAL1gator-8 and COMET/COMET-QUADs. In T1 mode, this signal consists of a pulse once every 193 bit periods.
TL_CLK[7..0]	This is a clock signal at the transmit line rate. Its source is determined by the configuration of the FPGA.
RL_CLK[7..0]	Receive line clock at either 1.544 MHz or 2.048 MHz, derived from the recovered line rate timing.
RL_SYNC[7..0]	Carries receive frame synchronization from the COMET/COMET-QUAD devices.
RL_SIG[7..0]	Carries the CAS signaling information from the COMET/COMET-QUAD devices.
RL_DATA[7..0]	Carries the receive data from the COMET/COMET-QUAD devices.
TL_SIG[7..0]	Carries the CAS signaling outputs to the COMET/COMET-QUAD devices.
TL_DATA[7..0]	Carries the serial data to the COMET/COMET-QUAD devices.

5.6 The FPGA Block

If the direct connections between the AAL1gator-8 and the COMETs or the COMET-QUADs are not used, depending upon the configuration, the Field Programmable Gate Array (FPGA) performs the following optional functions:

1. Implements an external Adaptive Clock Recovery scheme if a designer would like to perform an external algorithm instead of the AAL1gator-8's own internal algorithm.
2. Distributes XCLK source among the COMET or COMET-QUAD devices.
3. Generates the 8 kHz framing pulses.
4. Generates a software selected N_CLK signal (2.43 MHz) from the Network clock.

Note that the AAL1gator-8 is capable of implementing SRTS or Adaptive Clock Recovery scheme on its own; therefore, the FPGA is not required to perform these methods, but it is required to perform the other functions as mentioned in items 2-4 above.

In the adaptive Clock recovery mode, the AAL1gator-8 provides a queue depth difference for controlling of an external clock. The FPGA latches the channel status and frame difference and uses them to adjust the synthesized clock frequency. If the queue depth is low, the clock frequency is reduced; however, if the queue depth is high, the clock frequency is increased.

The FPGA also distributes XCLK signals to the 8 COMET or two COMET-QUAD devices from only two clock oscillators: 1.544 MHz and 2.048 MHz.

Another function of the FPGA is to generate the 8 kHz framing pulse from the transmit line clock (BTCLK in the COMET or in the COMET-QUAD) to the framers. This 8 kHz signal connects to the AAL1gator-8 TL_SYNC input and the COMET's or COMET-QUAD's BTFP input. In the T1 mode, the frame pulse (BTFP) is one clock (BTCLK) period wide, generated every 193 bits. But, in the E1 mode, the frame pulse is generated every 256 bits.

For implementation of the synchronous residual time stamp (SRTS), the AAL1gator-8's network clock (N_CLK) must be a 2.43 MHz signal. This signal is generated by dividing a 155.52 MHz ATM network clock by 64 in the FPGA.

In the AAL1gator-8 with COMET-QUADs Reference Design, if the H-MVIP mode is used, the FPGA is used to distribute the 16.384 MHz clock to the AAL1gator-8's C16B and to the COMET-QUADs' CMV8MCLK input pins. The FPGA is also used to distribute the 4.096 MHz Frame Pulse Clock to the AAL1gator-8's C4B

and to the COMET-QUADs' CMVPFC inputs, and to generate the 8 kHz Common H-MVIP Frame Pulse from the Frame Pulse Clock. The H-MVIP common frame pulse is sampled on the falling edge of the 4.096 MHz clock and occurs every 125us (i.e. occurs every 512 pulse).

5.7 AAL1gator-8's SRAM

A 128k x 16 bit pipelined SRAM or ZBT RAM can be used to interface with AAL1gator-8. In this reference design, a pipelined Synchronous NBT (No Bus Turn Around) SRAM, GS841Z18, from GSI Technology is used due to low power consumption (of approximately 100 mA at 3.3V less than other vendors). The GS841Z18 SRAM (256k x 18) has 18 bi-directional data pins two of which indicate odd parity for the lower and upper bytes of data. Note that since there is not any 128k x 16-bit ZBT SRAMs in the market, a 256k x 16-bit ZBT SRAM is used for this reference design.

Other manufacturers such as Cypress Semiconductor's NoBL, Samsung Electronics' NtRAM, or Integrated Device Technology's ZBT RAMS can also be used instead of the GS841Z8 NBT SRAM due to the pin compatibility.

5.8 Regulators Block

To generate +3.3V and +2.5V voltages from +5V (Vcc), two low drop out voltage regulators: LT1528 and LT1118CST are used in the AAL1gator-8 Reference Design. The LT1528 voltage regulator provides up to 3A at 3.3V to the board. The LT1118CST voltage regulator provides up to 0.500A at 2.5V to the AAL1gator-8 with COMETs reference design and up to 0.750A at 2.5 V to the AAL1gator-8 with COMET-QUADs reference design. Both regulators should be in the DD package, so that no additional heat sink is required. The dissipated heat for each regulator is:

$$P = (5 - 3.3) \text{ V} \times 3.0 \text{ A} = 5.1 \text{ W for LT1528}$$

$$P = (5 - 2.5) \text{ V} \times 0.5 \text{ A} = 1.25 \text{ W for LT1118CST in AAL1gator-8 w/COMETs}$$

$$P = (5 - 2.5) \text{ V} \times 0.75 \text{ A} = 1.875 \text{ W for LT1118CST in AAL1gator-8 w/COMET-Q}$$

5.9 LED Blocks

The LED blocks contain super green and yellow LEDs.

The 3 super green LEDs are used to show power status of +5V, +3.3V and +2.5V power sources.

The yellow LEDs are used for interrupt and alarm monitoring the AAL1gator-8, COMET and COMET-QUAD devices.

5.10 RESET Block

The hardware reset circuitry is constructed with a pushbutton switch and the MAX700 Power-Supply Monitor with Reset device circuitry.

5.11 JTAG Port

The JTAG port is connected among all devices to allow for boundary scan testing. The signals are connected in the following way:

- **TMS** The Test Mode Select signal is connected in parallel among all COMET/COMET-QUAD devices, NBT SRAM and the AAL1gator-8.
- **TCK** The Test Clock signal is connected in parallel among all COMET/COMET-QUAD devices, NBT SRAM and the AAL1gator-8.
- **TRSTB** The Test Reset Select signal is connected in parallel among all COMET/COMET-QUAD devices and the AAL1gator-8. The source of this signal may either be the JTAG controller, or from a pushbutton activation
- **TDI/TDO** The Test Data Input/Test Data Output signal is connected serially among all COMET/COMET-QUAD devices, NBT SRAM and the AAL1gator-8, beginning with the AAL1gator-8, and ending with the last COMET/COMET-QUAD device.

The JTAG port signals connect to an externally accessible header.

5.12 Timing Block

The timing block consists of the oscillators and part of the FPGA. The 50ppm HCMOS oscillators chosen are packaged in half-sized metal can DIP. Table 2 shows the type and functionality of the oscillators used in the reference design.

Table 2 Oscillators

Frequency (MHz)	PPM	Usage
1.544	50	Provides XCLK signals to the COMETs or COMET-QUADs in T1 mode.
2.048	50	Provides XCLK signals to the COMETs or COMET-

QUADs in E1 mode.		
38.88	50	Provides the AAL1gator-8's system clock (AAL1_SYSCLK) and the AAL1gator-8's SRAM clock (RAM_CLK)
4.096	50	Used in H-MVIP mode to generate and sample the H-MVIP frame pulse signal.
16.384	50	Used in H-MVIP mode to provide the common clock used to transfer data across the H-MVIP bus.

5.13 UTOPIA Interface

The AAL1gator-8 can communicate with any ATM layer devices (such as the S/UNI-ATLAS) via the UTOPIA interface. Please refer to UTOPIA Interface signals in the AAL1gator-8 data sheet [1] for description of the individual signals.

There are two possible bus modes of operation for the AAL1gator-8: UTOPIA mode and Any-PHY mode. These configurations are possible through the AAL1gator-8's UI_Source_Config Register (UI_SRC_CFG). When the ANY_PHY_EN bit in this register is cleared (ANY_PHY_EN = '0'), the AAL1gator-8 is configured with a UTOPIA interface. When the ANY_PHY_EN bit is set (ANY_PHY_EN = '1'), the device is in the Any-PHY mode. Also, the UTOP_MODE [1:0] bits in this register selects the UTOPIA operating mode for the source side interface as illustrated in Table 3.

Table 3 AAL1gator-8's UTOPIA Operating Modes

UTOP_MODE[1:0]	Operating Mode
'00'	UTOPIA-Level 1 Master
'01'	UTOPIA-Level 1 Slave
'10'	UTOPIA-Level 2 Single Address Slave
'11'	Reserved

6 DESIGN ISSUES

6.1 AAL1gator-8 Design Considerations

6.1.1 Power Supply

The power to the +3.3V pins should be applied before power to +2.5V pins is applied. All the ground pins (PPL, PQL, and PCL) should be connected together.

6.1.2 Decoupling

A 0.01 μ F capacitor is placed between power and ground for the +2.5V and +3.3V pins. The capacitors should be placed as close to the actual pin as possible.

6.1.3 Line Mode Selection

The AAL1gator-8 can be configured to operate in direct mode by setting the Line_Mode pin low or high for H-MVIP mode. For this purpose a set of jumpers are provided to select ground (low) or +3.3V. (high). This hardware configuration must be done prior to power up.

6.2 Line Termination

For each of the 8 line terminations to the COMET or COMET-QUAD devices, this reference design uses a termination that compromises between 100 Ohm T1 and 120 Ohm E1. The 75 Ohm E1 termination has not been used.

6.3 COMET Design Considerations

6.3.1 Power Supply

During power-up, the BIAS pin must be equal to or greater than the voltage on the VDD pins. This is accomplished with the voltage regulator. The voltage on the BIAS pin is also the same one used to regulate the VDD voltage. Therefore, the worst case is that the regulator malfunctions and shorts, which still leaves the BIAS pin equal to VDD. Also, an extra protection diode is used to limit the VDD to a maximum of 0.5V above the BIAS voltage.

Analog power pins must be applied after VDD or they must be current limited to the maximum latch-up current of 100mA. A simple solution is to use a small filtering network between the VDD and AVD pins to delay the power.

The differential voltage measured between AVD supplies and VDD must be less than 0.5V.

6.3.2 Decoupling

A 0.01 μ F capacitor is placed between power and ground for the VDDO pins. A 0.1 μ F capacitor is placed between power and ground for the VDDI pins. The capacitors should be placed as close to the actual pin as possible.

The AVD pins require a filtering network between the VDD plane and each AVD pin. The network is a single RC network with the resistor between the VDD plane and the AVD pin and the capacitor from the AVD pin to the GND plane. Please refer to the schematics in Appendix A for component values.

6.3.3 Voltage References

The Transmit Voltage Reference pin (TVREF) requires a 4.7 μ F capacitor to analog ground and two 12.7 Ω resistors to the corresponding TxRING and TxTIP pins.

The Reference Voltage Reference pin (RVREF), which is reserved for a precision analog voltage or current reference, must be connected to a RC circuit consisting of a 100 k Ω resistor connected in parallel with a 10nF capacitor to analog ground.

6.4 COMET-QUAD Design Considerations

6.4.1 Power Supply Sequencing

The following power up sequence for the COMET-QUAD must be followed:

1. +3.3V digital pins
2. +3.3V analog pins (TAVDx, CAVD, RAVDx, QAVD)
3. +2.5V digital pins

Power to the +3.3V pins, both analog and digital, must be applied before +2.5V. Power to the +3.3V digital pins must be applied before power to the +3.3V analog. A simple solution for the latter statement is to use a small filtering network between the +3.3V digital and +3.3V analog pins to delay the power.

6.4.2 Decoupling

0.01 μ F and 0.1 μ F capacitors are placed between power and ground for the VDD (+2.5 V and +3.3V) pins. The capacitors should be placed as close to the actual pins as possible.

The AVD pins require a filtering network between the VDD plane and each AVD pin. The network is a single RC network with the resistor between the VDD plane and the AVD pin and the capacitor from the AVD pin to the GND plane. Please refer to the schematics in Appendix A for component values.

6.4.3 Voltage References

Each of The Transmit Common Mode pin (TxCM[1:4]) requires 4.7 μ F capacitors to analog ground and two 12.7Ohm resistors to the corresponding TxRING and TxTIP pins.

The Reference Voltage Reference pin (RVREF), which is reserved for a precision analog voltage or current reference, must be connected to a RC circuit consisting of a 100 kohm resistor connected in parallel with a 10nF capacitor to analog ground.

6.5 Microprocessor Interface

Table 4 and Table 5 list the pin assignment of potential microprocessor interfaces (96 pin DIN) for AAL1gator-8 reference design with COMETs and COMET-QUADs, respectively. Note that these interfaces include all connections from the microprocessor to the AAL1gator-8, COMET and COMET-QUAD devices, and FPGA.

Table 4 Interface Pinout for AAL1gator-8 w/COMETs

PIN NAME	PIN TYPE	PIN NUMBER	FUNCTION
UP_D(15)	I/O	A17	16 bit data bus
UP_D(14)		A18	
UP_D(13)		A19	
UP_D(12)		A20	
UP_D(11)		A21	
UP_D(10)		A22	
UP_D(9)		A23	
UP_D(8)		A24	
UP_D(7)		A25	
UP_D(6)		A26	

PIN NAME	PIN TYPE	PIN NUMBER	FUNCTION
UP_D(5)		A27	
UP_D(4)		A28	
UP_D(3)		A29	
UP_D(2)		A30	
UP_D(1)		A31	
UP_D(0)		A32	
UP_A(23)	Input (from uP)	C9	24 bit address bus
UP_A(22)		C10	
UP_A(21)		C11	
UP_A(20)		C12	
UP_A(19)		C13	
UP_A(18)		C14	
UP_A(17)		C15	
UP_A(16)		C16	
UP_A(15)		C17	
UP_A(14)		C18	
UP_A(13)		C19	
UP_A(12)		C20	
UP_A(11)		C21	
UP_A(10)		C22	
UP_A(9)		C23	
UP_A(8)		C24	
UP_A(7)		C25	
UP_A(6)		C26	
UP_A(5)		C27	
UP_A(4)		C28	
UP_A(3)		C29	
UP_A(2)		C30	
UP_A(1)		C31	
UP_A(0)		C32	
RDB_IN	Input	C7	Active Low read signal
WRB_IN	Input	C8	Active Low write signal.
AAL1_ACKB	Input	C1	Active Low acknowledge signal to uP.
AAL1_INTB	Output (to uP)	C5	Active low interrupt request to uP. from AAL1gator-8
IRQ2B	Output	C7	Active low interrupt request to uP from Framer
RSTB	Input	A1	Active low global reset.
AAL1_CS	Input	C2	Active low chip select. When asserted, the AAL1gator-8 is selected.

PIN NAME	PIN TYPE	PIN NUMBER	FUNCTION
CS2B	Input	C3	Active low chip select. When asserted the COMET is selected.
CS3B	Input	C4	Active low chip select. When asserted, the FPGA is selected.
GND	n/a	B1 – B26	GND. Ground Reference

Table 5 Interface Pinout for AAL1gator-8 w/COMET-QUADs

PIN NAME	PIN TYPE	PIN NUMBER	FUNCTION
UP_D(15)	I/O	A17	16 bit data bus
UP_D(14)		A18	
UP_D(13)		A19	
UP_D(12)		A20	
UP_D(11)		A21	
UP_D(10)		A22	
UP_D(9)		A23	
UP_D(8)		A24	
UP_D(7)		A25	
UP_D(6)		A26	
UP_D(5)		A27	
UP_D(4)		A28	
UP_D(3)		A29	
UP_D(2)		A30	
UP_D(1)		A31	
UP_D(0)		A32	
UP_A(21)		Input (from uP)	
UP_A(20)	C12		
UP_A(19)	C13		
UP_A(18)	C14		
UP_A(17)	C15		
UP_A(16)	C16		
UP_A(15)	C17		
UP_A(14)	C18		
UP_A(13)	C19		
UP_A(12)	C20		
UP_A(11)	C21		
UP_A(10)	C22		
UP_A(9)	C23		
UP_A(8)	C24		
UP_A(7)	C25		
UP_A(6)	C26		
UP_A(5)	C27		

PIN NAME	PIN TYPE	PIN NUMBER	FUNCTION
UP_A(4)		C28	
UP_A(3)		C29	
UP_A(2)		C30	
UP_A(1)		C31	
UP_A(0)		C32	
RDB_IN	Input	C7	Active Low read signal
WRB_IN	Input	C8	Active Low write signal.
AAL1_ACKB	Input	C1	Active Low acknowledge signal to uP.
AAL1_INTB	Output (to uP)	C5	Active low interrupt request to uP. from AAL1gator-8
IRQ2B	Output	C7	Active low interrupt request to uP from Framer
RSTB	Input	A1	Active low global reset.
AAL1_CSB	Input	C2	Active low chip select. When asserted, the AAL1gator-8 is selected.
CS2B	Input	C3	Active low chip select. When asserted, the COMET-QUAD is selected.
CS3B	Input	C4	Active low chip select. When asserted, the FPGA is selected.
GND	n/a	B1 – B26	GND. Ground Reference

Figures 4 and 5 indicate the usage of external address buffers and data transceivers. In order for the system to operate at the maximum frequency of 40.00 MHz, the address buffers must have a worst case propagation delay of 8ns, while the data transceivers must have a worst case delay of 10ns. For these reasons the IDT74FCT163827CT was chosen as the address buffer. This 20 bit device has a maximum propagation delay of 4.4ns (50pF, 500Ω load). The IDT74FCT163646 was chosen as the data transceiver. This 16-bit device has a worst case propagation delay of 5.4ns under the same loading conditions.

When the microprocessor wishes to communicate with a COMET device, it asserts an address as listed in the Table 6. When an appropriate address is driven onto the bus, the microprocessor simultaneously asserts CS2B. Since A23 is high, the decoder is then active. Address bits A[22..20] determine which output of the decoder is driven low. One decoder output connects to the CSB input of each COMET device. For example, if A[22..20] are 000, then decoder output Y0 is driven low, which also asserts CSB of COMET0. No other COMET

device is selected at this time. Address bits A[8..0] determine which register of the COMET the microprocessor is communicating with.

In order to meet the timing requirements of the COMET devices (refer to [2]), the 3-8 decoder (74HCT138) must have a maximum propagation delay of 10ns. With a 15pF load, the device has a typical delay of 13ns. At 50pf (VCC = 4.5), the delay increases to 38ns, and therefore will meet the specifications.

Table 6 Address Space for AAL1gator-8 w/COMETs

DEVICE	BASE ADDRESS	ADDRESS RANGE
AAL1gator-8	000000h	000000 – 0FFFFFFh
COMET0	800000h	800000 – 8001FFh
COMET1	900000h	900000 – 9001FFh
COMET2	A00000h	A00000 – A001FFh
COMET3	B00000h	B00000 – B001FFh
COMET4	C00000h	C00000 – C001FFh
COMET5	D00000h	D00000 – D001FFh
COMET6	E00000h	E00000 – E001FFh
COMET7	F00000h	F00000 – F001FFh

Table 7 shows the Address ranges of the devices used in the AAL1gator-8 with COMET-QUADs reference design.

Table 7 Address Space for AAL1gator-8 w/COMET-QUADs

DEVICE	BASE ADDRESS	ADDRESS RANGE
AAL1gator-8	000000h	000000 – 0FFFFFFh
COMET-QUAD0	200000h	200000 – 2007FFh
COMET-QUAD1	300000h	300000 – 3007FFh

Since the address and data buses are shared among many devices, a 20 bit buffer and transceiver is used. This insures that clean signals are present on the inputs of the devices, and that no data collisions occur. The buffer (FCT163827) is not only placed on the address lines, but the various control signals such as WRB and RDB as well. The 16-bit transceiver (FCT163646) is used in flow through mode to control data bus access. The transceivers output enable is controlled by the result of a logical AND of CS2B and CS3B. In this way, whenever the microprocessor needs to communicate with either a COMET/COMET-QUAD or the FPGA, either the CS2B, or CS3B signal must be driven low, which drives the active low output enable signal of the transceiver low. The transceivers' direction is controlled by the WRB signal.

6.6 Power Requirements

Table 8 provides the estimated power requirements for the AAL1gator-8 Reference Design with COMETs. Table 9 for AAL1gator-8 w/COMET-QUADs provides the maximum power requirements for the AAL1gator-8 Reference Design with COMET-QUADs.

Table 8 Power Consumption for AAL1gator-8 w/COMETs

5V Components	Quantity	Current (mA)	Power (mW)
74HCT138A (SOIC)	1	100	500
LEDs	3	15	225
74HCT08	1	3	15
Misc, pullups/downs	1	100	500
Total 5V Power			1240 (mW)

3.3V Components	Quantity	Current (mA)	Power (mW)
COMET	8	250	6600
AAL1gator-8	1	122	402.6
FPGA	1	360	1188
GSI NBT SRAM	1	210	693
Oscillators	5	40	660
LEDs	8	20	528
Buffers/Transceivers	4	5.5	72.6
Misc.	1	200	660
Total 3.3V Power			10804.(mW)

2.5V Components	Quantity	Current (mA)	Power (mW)
AAL1gator-8	1	240	600
Total 2.5V Power			600 (mW)

Total Power			12644 (mW)
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Table 9 Power for AAL1gator-8 w/COMET-QUADs

5V Components	Quantity	Current (mA)	Power (mW)
74HCT138A (SOIC)	1	100	500
LEDs	3	15	225
74HCT08	1	3	15
Misc, pullups/downs	1	100	500
Total 5V Power			1240 (mW)

3.3V Components	Quantity	Current (mA)	Power (mW)
COMET-QUAD	2	441	2910.6
AAL1gator-8	1	122	402.6
FPGA	1	360	1188
GSI NBT SRAM	1	210	693
Oscillators	5	40	660
LEDs	9	20	594
Buffers/Transceivers	4	5.5	72.6
Misc.	1	200	660
Total 3.3V Power			7181 (mW)

2.5V Components	Quantity	Current (mA)	Power (mW)
COMET-QUAD	2	38	190
AAL1gator-8	1	240	600
Total 2.5V Power			790 (mW)

Total Power			9211 (mW)
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7 IMPLEMENTATION DESCRIPTION

The AAL1gator-8 with COMETs and the AAL1gator-8 with COMET-QUADs reference design schematics were captured using Cadence software Concept Schematics Capture tool.

7.1 AAL1GATOR-8 with COMET Schematics

Sheet 1: ROOT DRAWING

This sheet provides an overview of the major functional blocks of the AAL1gator-8 plus COMET reference design. Also, it illustrates the interconnections among the various blocks in the design. Groups of signals have been combined into a bus type name format even though these signals are not typically made into buses. This is done to make the schematic less cluttered and more readable and to utilize the capabilities of the schematic capture tool. Some examples of such signals are the TXTIP<7..0>, TL_DATA<7..0>, and TL_CLK<7..0>.

Sheets 2-9: COMET BLOCK

These sheets show the COMET devices and their power circuitry. The power circuitry includes a schottky diode for protection while powering up the COMET device and separate filtering circuitry for the analog and digital power pins. In addition, the JTAG port is connected among the 8 COMET devices, and the AAL1gator-8.

Sheets 10-13: LINE INTERFACE

These schematics show the termination, magnetic and protection circuitry for the line interface. A Pulse T9021, a quad 1:2.42 transformer included with two Surge Protector Diode Array, is used to couple four COMETs' transmit and receive lines to the connectors. The LC01-6 transient voltage suppressor (TVS) and the Raychem PTC provide over voltage protection. A single footprint is provided for both the bantam and RJ48C connectors.

Sheet 14: FPGA BLOCK

This sheet shows the interconnection of the Actel 42MX36 FPGA between the AAL1gator-8 and the COMET devices. The 1.544 MHz and 2.048 MHz oscillators are present to supply the XCLK signal to the COMET devices. The 38.88 MHz oscillator is present to supply the AAL1gator-8 system clock (SYSCLK) and the AAL1gator-8's ZBT RAM clock (RAM_CLK). The ATM

Network clock is used by the FPGA to generate the 2.43 MHz NCLK. 0.1uF bulk capacitors are specified, and should be placed at the corners of the FPGA.

The AAL1gator-8's clock synthesizer's interfaces are optionally provided to the FPGA in order to provide customization of SRTS or adaptive recovery algorithms.

Note that the FPGA Mode pin is set to low except during the device programming and debugging.

Note that the actual design of the FPGA has not been performed in this paper reference design. The FPGA design can be implemented with schematics or a hardware definition language.

Sheet 15: MEMORY SYSTEM BLOCK

This sheet indicates the connections between the system microprocessor, and the AAL1gator-8, COMET devices, and FPGA. 20 bit buffers and 16 bit data transceivers are present.

Sheets 16-18: AAL1GATOR-8 BLOCK

These sheets show how the AAL1gator-8 is connected into the system.

Page 16 illustrates the AAL1gator-8's line interface, microprocessor interface, JTAG connections, power supply signal connections, and the decoupling capacitors. Note that the TLCLK_OE input pin is set high to make the TL_CLK pins as outputs between the time of hardware reset and when the CLK_SOURCE_TX bits are read. In the Direct mode, the Line_Mode pins are grounded.

Page 17 shows the AAL1gator-8's RAM interface with a 256k x 18-bit pipelined GS841Z18 NBT SRAM. Since the RAM interface of the AAL1gator-8 is limited to 128k, the most significant bit of the SRAM is grounded. Bits 8 and 17 indicate odd parity for the lower and upper bytes, respectively.

Page 18 shows the AAL1gator-8's UTOPIA connection to a UTOPIA L2 connector to provide access to the UTOPIA bus externally.

Sheet 19: MICRO INTERFACE / POWER

This page shows the connections between the system microprocessor and the reference design board. The LT1528 low drop out voltage regulator provides up to 3A at 3.3V to the board. The LT1118CST voltage regulator provides up to 0.500A at 2.5V to the AAL1gator-8 reference design. Both regulators should be in the DD package, so that no additional heat sink is required. Also, a pushbutton

switch is included in the Reset circuitry to provide the hardware reset. This page is also included the JTAG port, the power and interrupt status LED circuitry.

7.2 AAL1GATOR-8 with COMET-QUAD Schematics

Sheet 1: ROOT DRAWING

This sheet provides an overview of the major functional blocks of the AAL1gator-8 plus COMET-QUAD reference design. Also, it illustrates the interconnections among the various blocks in the design.

Sheets 2-3: COMET-QUAD BLOCK

These pages show the COMET-QUAD devices and their power circuitry. Separate filtering circuitry for the analog and digital power pins is included. In addition, the JTAG port is connected among the 2 COMET-QUAD devices, and the AAL1gator-8. The H-MVIP signal interface is also provided for the optional use.

Sheets 4-7: LINE INTERFACE

These schematic diagrams are the same as those for the COMET version.

Sheet 8: FPGA BLOCK

This sheet shows the interconnection of the FPGA between the AAL1gator-8 and the COMET-QUAD devices. The 1.544 MHz and 2.048 MHz oscillators are present to supply the XCLK signal to the COMET-QUAD devices. The 38.88 MHz oscillator is present to supply the AAL1gator-8 system clock (SYSCLK) and the AAL1gator-8's ZBT RAM clock (RAM_CLK). The ATM network clock is used by the FPGA to generate the 2.43 MHz NCLK. The 4.096 MHz and 16.384 MHz oscillators are provided for H-MVIP mode's common clock and frame pulses. 0.1uF bulk capacitors are specified, and should be placed at the corners of the FPGA.

Sheet 9: MEMORY SYSTEM BLOCK

This sheet indicates the connections between the system microprocessor, and the AAL1gator-8, COMET-QUAD devices, and FPGA. 20 bit buffers and 16 bit data transceivers are present.

Sheets 10-12: AAL1GATOR-8 BLOCK

These schematic diagrams are the same as those for the COMET version, except the Line_Mode0 pin can be set to low for the Direct mode or high for the H-MVIP mode.

Sheet 13: MICRO INTERFACE / POWER

This page shows the connections between the system microprocessor and the reference design board. The LT1528 low drop out voltage regulator provides up to 3A at 3.3V to the board. The LT1118CST voltage regulator provides up to 0.750A at 2.5V to the AAL1gator-8 and COMET-QUAD devices. Both regulators should be in the DD package, so that no additional heat sink is required. Also, a pushbutton switch is included in the Reset circuitry to provide the hardware reset. This sheet is also included the JTAG port, the power and interrupt status LED circuitry.

8 GLOSSARY

AAL1	ATM Adaptation Layer 1
Any-PHY	Interoperable version of UTOPIA and SCI-PHY
ATM	Asynchronous Transfer Mode
CBR	Constant Bit Rate
CES	Circuit Emulation Services
COS	Class of Service
PHY	Physical Layer
SAR	Segmentation and Re-assembly
SCI-PHY	PMC-Sierra enhanced UTOPIA bus
SRTS	Synchronous Residual Time Stamp
UTOPIA	Universal Test & Operations PHY Interface for ATM
VBR	Variable Bit Rate
VC	Virtual Circuit
VCC	Virtual Channel Connection
VCI	Virtual Circuit Identifier
VP	Virtual Path
VPC	Virtual Path Connection
VPI	Virtual Path Identifier
WAN	Wide Area Network
ZBT	Zero Bus Turnaround

9 DEFINITIONS

AAL (ATM Adaptation Layer) – The layer above the ATM layer that allows users to send packets larger than a cell. The ATM interface segments these packets, transmits the cells individually, and reassembles them at the other end. The AAL consists of two sub-layers: Convergence Sub-layer (CS) and Segmentation and Reassembly (SAR). The AAL supports many kinds of services with different traffic characteristics and system requirements.

AAL1 (ATM Adaptation Layer 1) – The layer above the ATM Layer in the ATM Protocol Model that handles adapting CBR traffic to an ATM network. Supports connection-oriented services that require constant bit rates and have specific timing and delay requirements. Examples are constant bit rate services like DS1 or DS3 transport.

CBR (Constant Bit Rate) – Constant Bit Rate (CBR) is one of the five service categories of the ATM Layer. This service type allows a user to define a specific cell delay, cell delay variation (CDV), and reserves a specific and fixed bandwidth on the network. The CBR traffic includes voice, video, and circuit emulation (e.g., T1 Circuit emulation). Voice and video that has been compressed may have a variable transmission rate and therefore would not fit into this service class.

CES (Circuit Emulation Service) – A service provided by ATM to emulate TDM circuits by not only passing bits through an ATM network but maintaining synchronization by providing end to end timing.

SAR (Segmentation and Reassembly) – The Segmentation and Reassembly Layer is the lower of two sublayers (Convergence Sublayer (CS) and SAR) that make up the ATM Adaptation Layer (AAL) as shown in the diagram below. The SAR is responsible for mapping data from the AAL Convergence Sublayer into the cell payloads of an ATM cell stream.

TDM (Time Division Multiplexing) – A method of multiplexing by which a transmission channel is divided into discrete time intervals

10 REFERENCES

1. PMC-Sierra Inc., PMC-1970624, "Combined E1/T1 Transceiver Standard Product Data Sheet", November 2000, Issue 10.
2. PMC-Sierra Inc., PMC-1990315, "COMET-QUAD Data Sheet", May 2001, Issue 6.
3. PMC-Sierra Inc., PMC-2000097, "AAL1gator-8 Data Sheet", January 2000, Issue 1.

11 DISCLAIMER

This document is a paper reference design, and as such, has not been built or tested as of this date.

12 APPENDIX A: BILL OF MATERIALS (COMET VERSION)

Table 10 Major Components List 1

Ref. No	Component	Manufacture	Package Type	Quantity
U1	PM73123 AAL1gator-8	PMC-Sierra Inc.	PBGA	1
U2-9	PM4351 COMET	PMC-Sierra Inc.	CABGA	8
U28-47	LC01-6	SEMTECH	SMD	16
U15-16	T9021 1:2.42 Transformer	Pulse Inc.	SMD	2
U12	A42MX36 PQ208 FPGA	ACTEL	PQFP	1
U55	GS841Z18 NBT SRAM	GSI Technology	TQFP	1
U14	MAX700 Power Supply Monitor	MAXIM	SOIC	1
U51, U53	74FCT163827 FAST 20 Bit Buffer	IDT	SOP	2
U52, U54	74FCT163646 FAST 16 Bit Transceiver	IDT	SOP	2
U11	MC74HCT138AD 3-to-8 Decoder	Motorola	SOIC	1
U10	MCHCT541 8 Bit Buffer	Motorola	SOIC	1
U56	LT1528 Voltage Regulator	Linear Technology	DD	1
U57	LT1118CST Voltage Regulator	Linear Technology	DD	1
Y1	HCMOS 38.880MHz, 50ppm Oscillator	MMD Components	Half-size DIP	1

Y2	HCMOS 1.544MHz, 50ppm Oscillator	MMD Components	Half-size DIP	1
Y3	HCMOS 2.048MHz, 50ppm Oscillator	MMD Components	Half-size DIP	1
F1	3.000A NANO	Littlefuse	SMD Socket	1
F2	0.500A NANO	Littlefuse	SMD Socket	1
SW1	Pushbutton switch		PBS	1
TR1-32	TR250-180U Thermistor	Raychem	PTC	32
J1, J3, J4, J6, J7, J9, J10, J12, J13, J15, J16, J18, J19, J21, J22, J24	PC-834-C-Black Bantam Covers	ADC Telecomm.		16

13 APPENDIX B: BILL OF MATERIALS (COMET-QUAD VERSION)

Table 11 Major Components List 2

Ref. No	Component	Manufacture	Package Type	Quantity
U1	PM73123 AAL1gator-8	PMC-Sierra Inc.	PBGA	1
U2-3	PM4354 COMET-QUAD	PMC-Sierra Inc.	PBGA	8
U20-23, U26-29, U32-35, U38-41	LC01-6	SEMTECH	SMD	16
U5-6	T9021 1:2.42 Transformer	Pulse Inc.	SMD	2
U9	A42MX36 PQ208 FPGA	ACTEL	PQFP	1
U7	GS841Z18 NBT SRAM	GSI Technology	TQFP	1
U14	MAX700 Power Supply Monitor	MAXIM	SOIC	1
U44, U46	74FCT163827 FAST 20 Bit Buffer	IDT	SOP	2
U45, U47	74FCT163646 FAST 16 Bit Transceiver	IDT	SOP	2
U4	MCHCT541 8 Bit Buffer	Motorola	SOIC	1
U11	MC74HCT138AD 3-to-8 Decoder	Motorola	SOIC	1
U42	LT1528 Voltage Regulator	Linear Technology	DD	1
U43	LT1118CST Voltage Regulator	Linear Technology	DD	1
Y1	HCMOS 38.880MHz, 50ppm	MMD	Half-size	1

	Oscillator	Components	DIP	
Y2	HCMOS 1.544MHz, 50ppm Oscillator	MMD Components	Half-size DIP	1
Y3	, HCMOS 2.048MHz, 50ppm Oscillator	MMD Components	Half-size DIP	1
Y4	HCMOS 16.384MHz, 50ppm Oscillator	MMD Components	Half-size DIP	1
Y5	HCMOS 4.096MHz, 50ppm Oscillator	MMD Components	Half-size DIP	1
F2	Littlefuse, 3.000A NANO	Littlefuse	SMD Socket	1
F1	Littlefuse, 0.750A NANO	Littlefuse	SMD Socket	1
SW1	Pushbutton switch	.	PBS	1
TR1-32	Raychem, TR250-180U Thermistor	Raychem	PTC	32
J1, J3, J4, J6, J7, J9, J10, J12, J13, J15, J16, J18, J19, J21, J22, J24	PC-834-C-Black Bantam Covers	ADC Telecomm		16

PRELIMINARY

REFERENCE DESIGN

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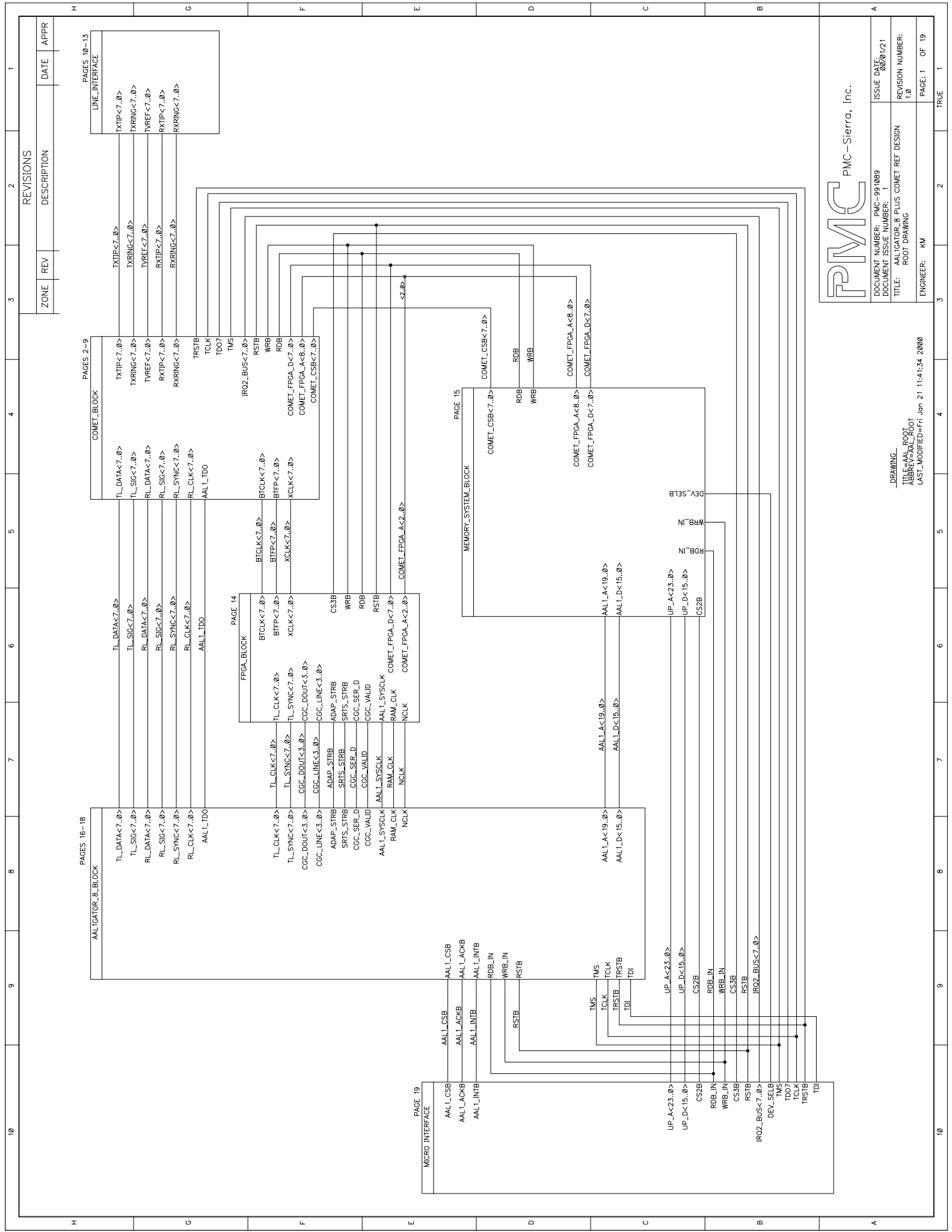
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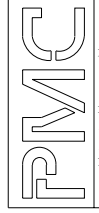
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AAL1GATOR-8 REFERENCE DESIGN

14 APPENDIX C: AAL1GATOR-8 W/COMETS SCHEMATICS



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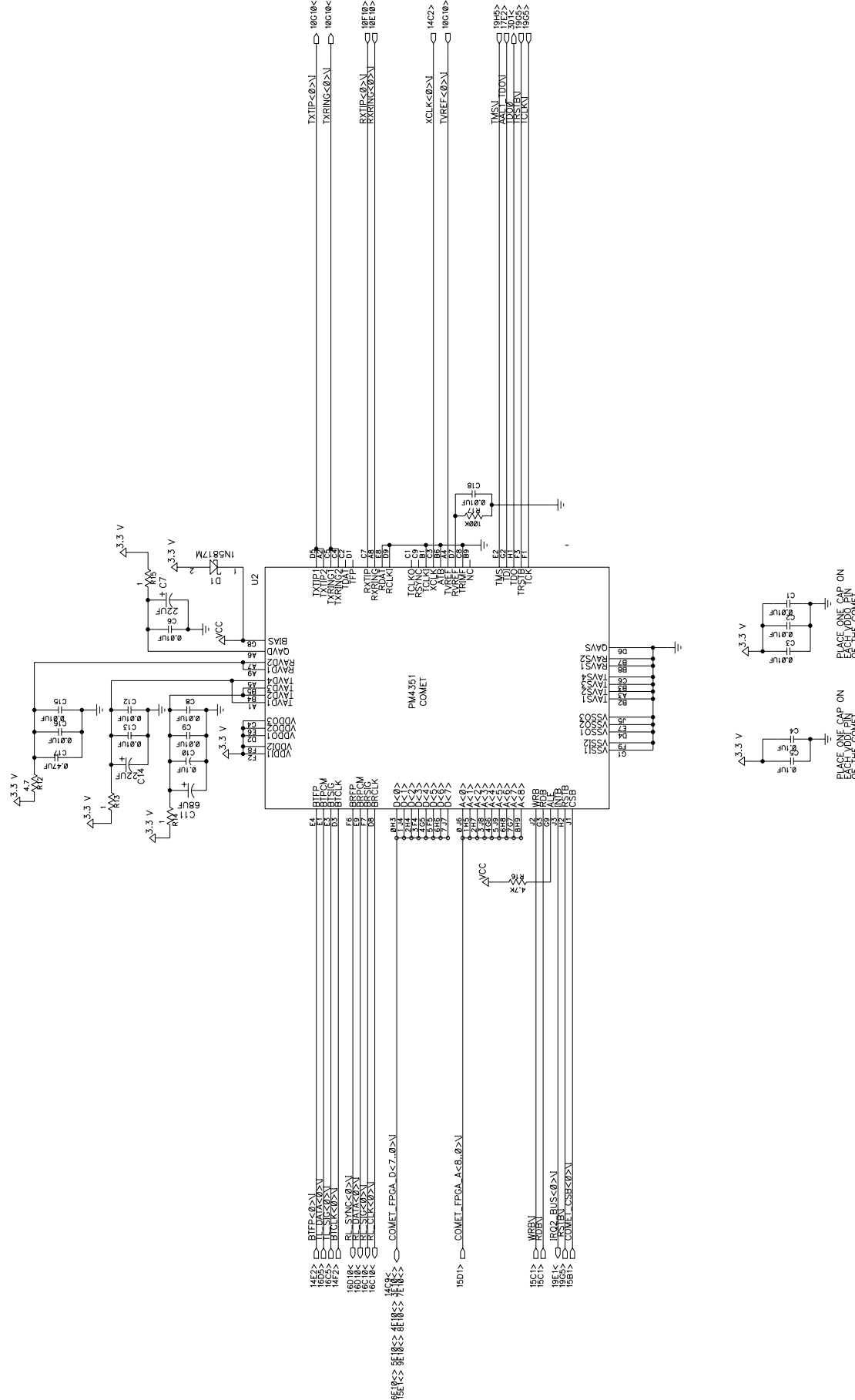
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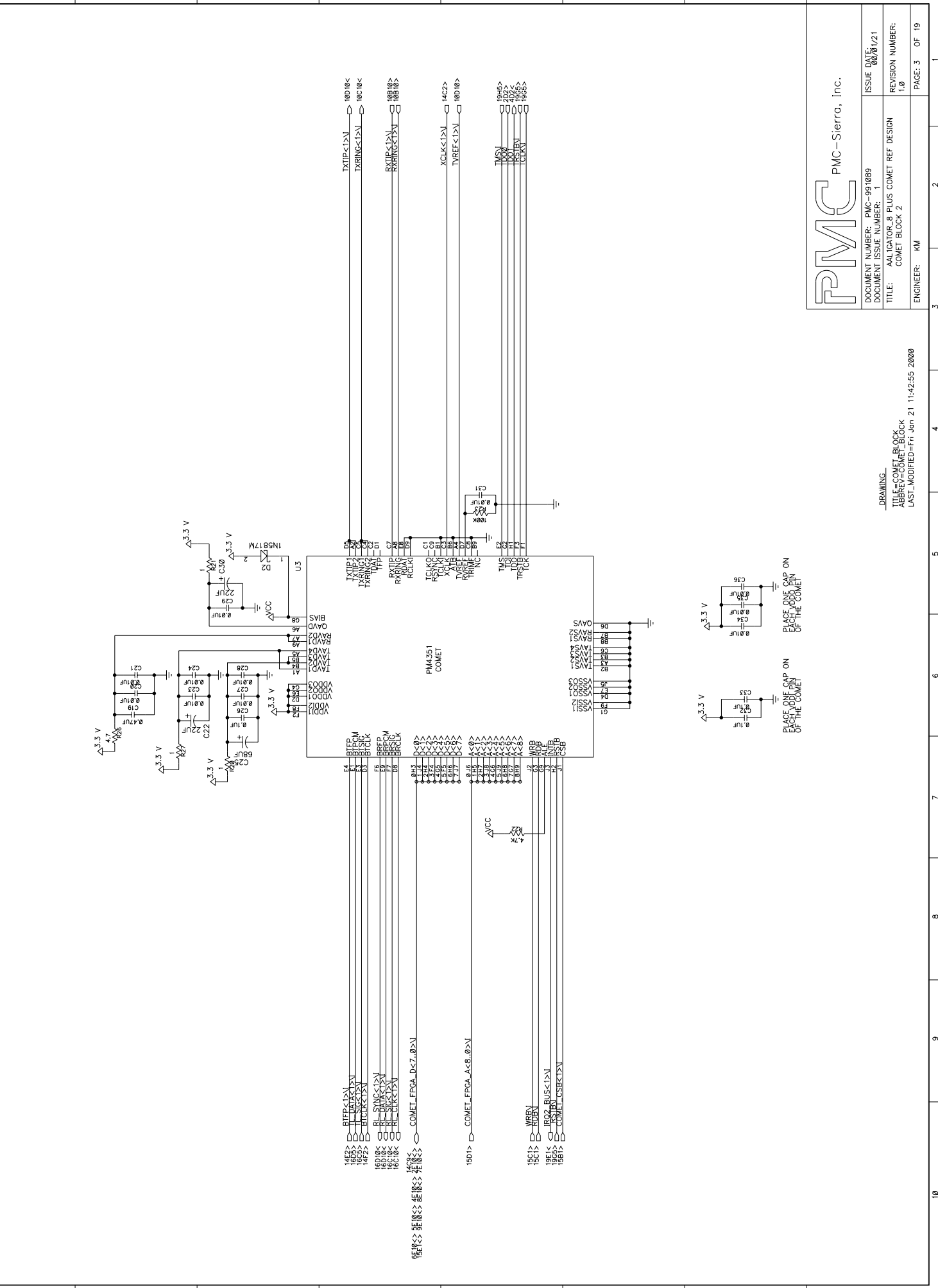
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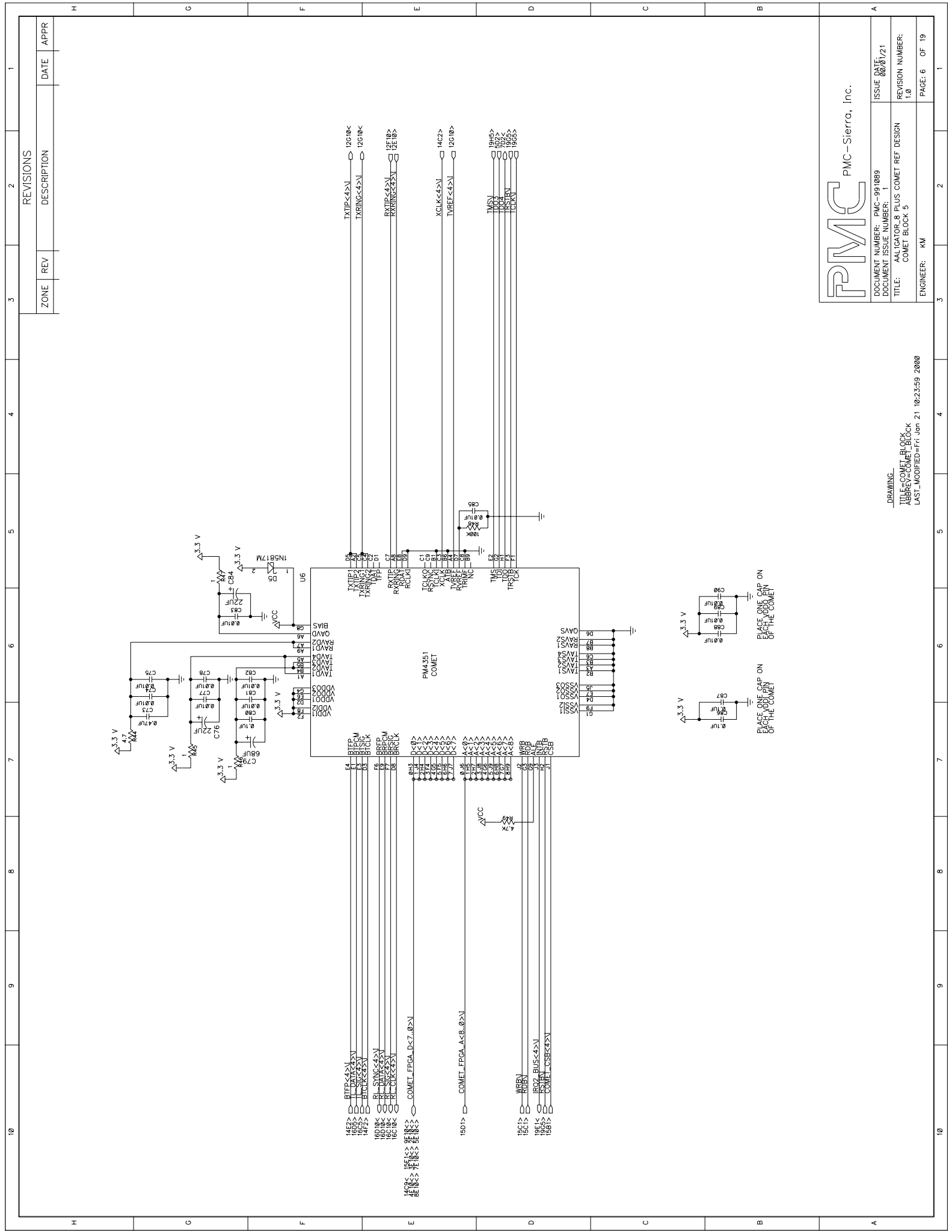
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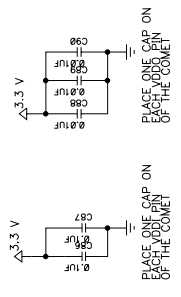
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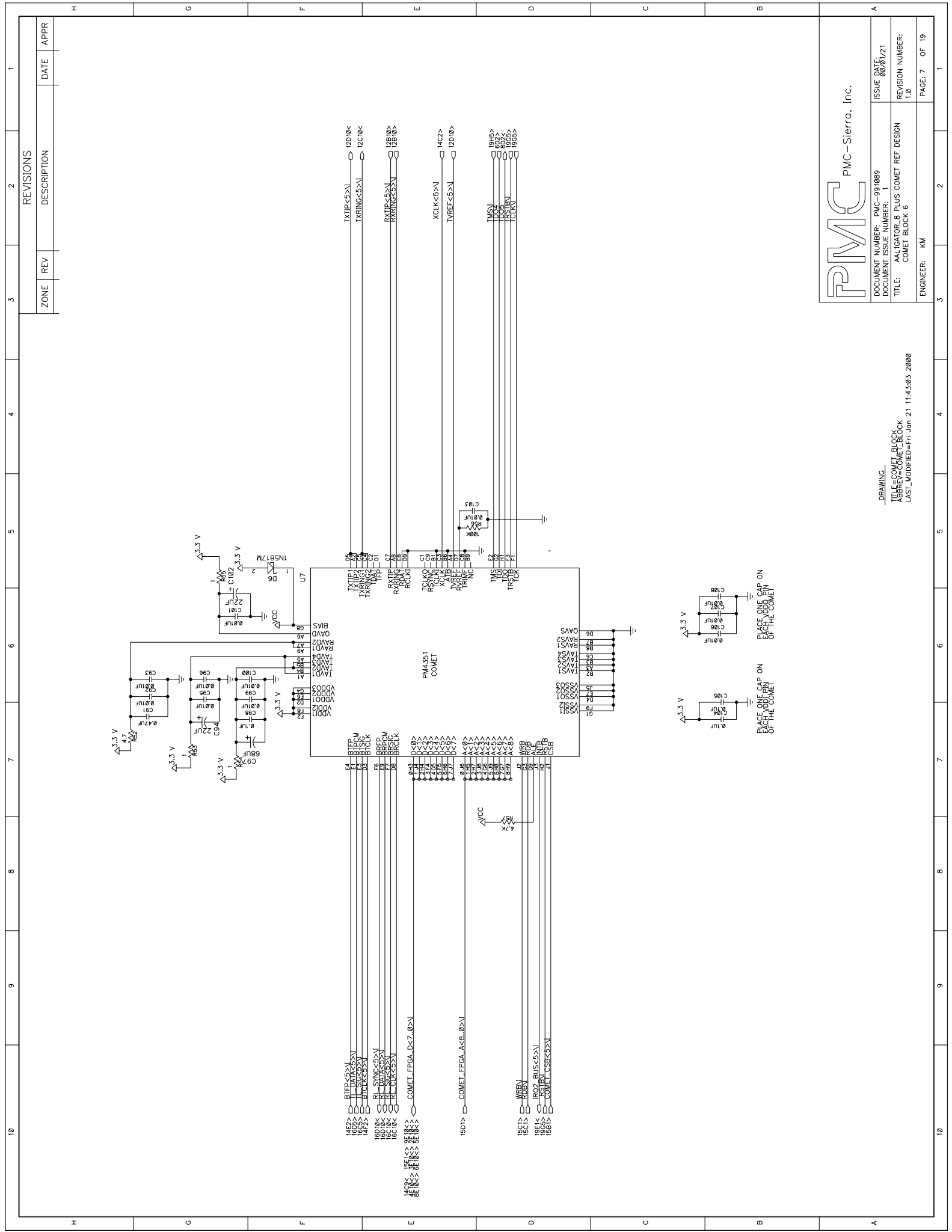
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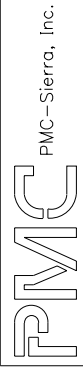
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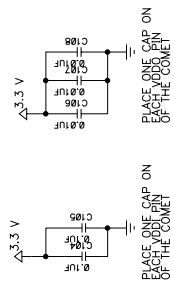
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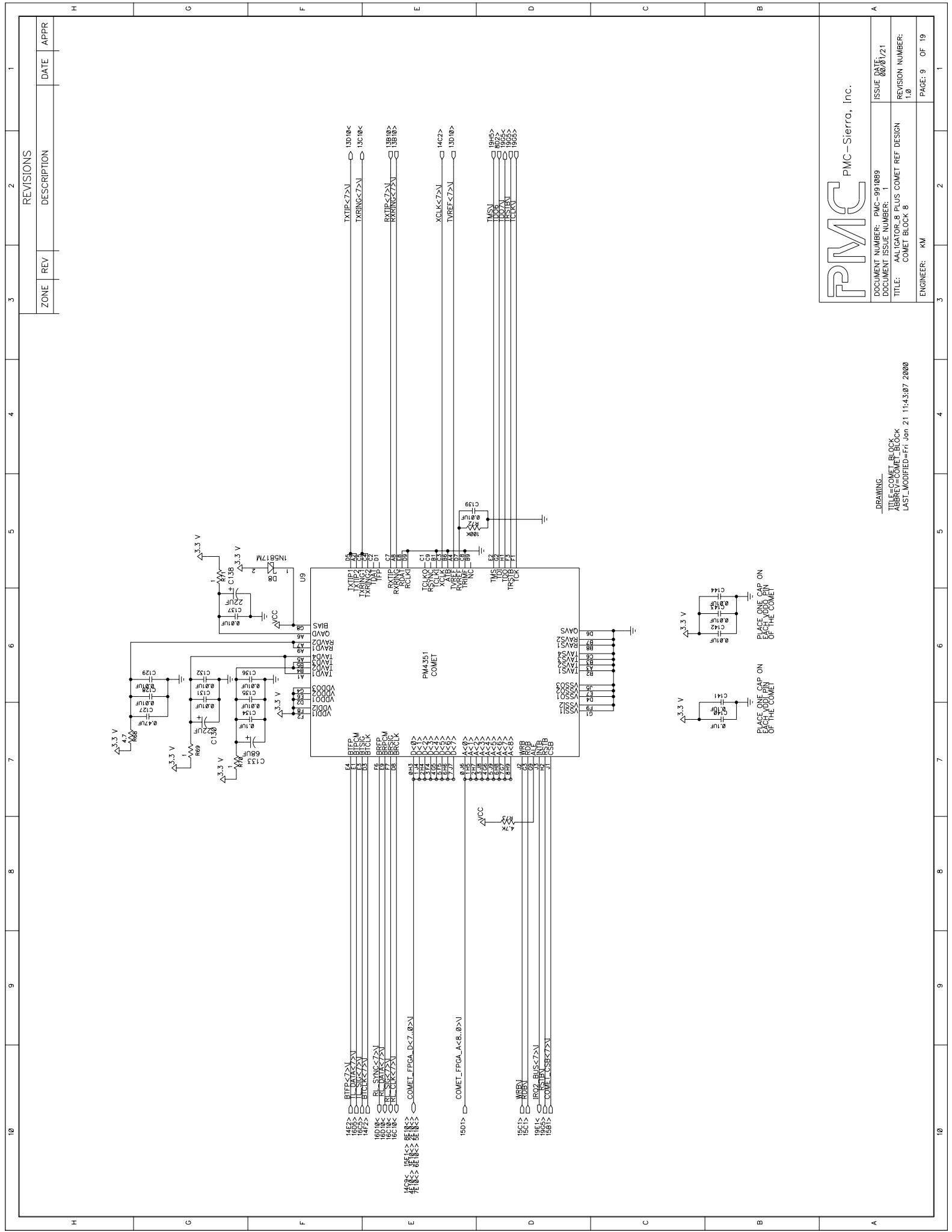


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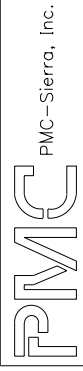
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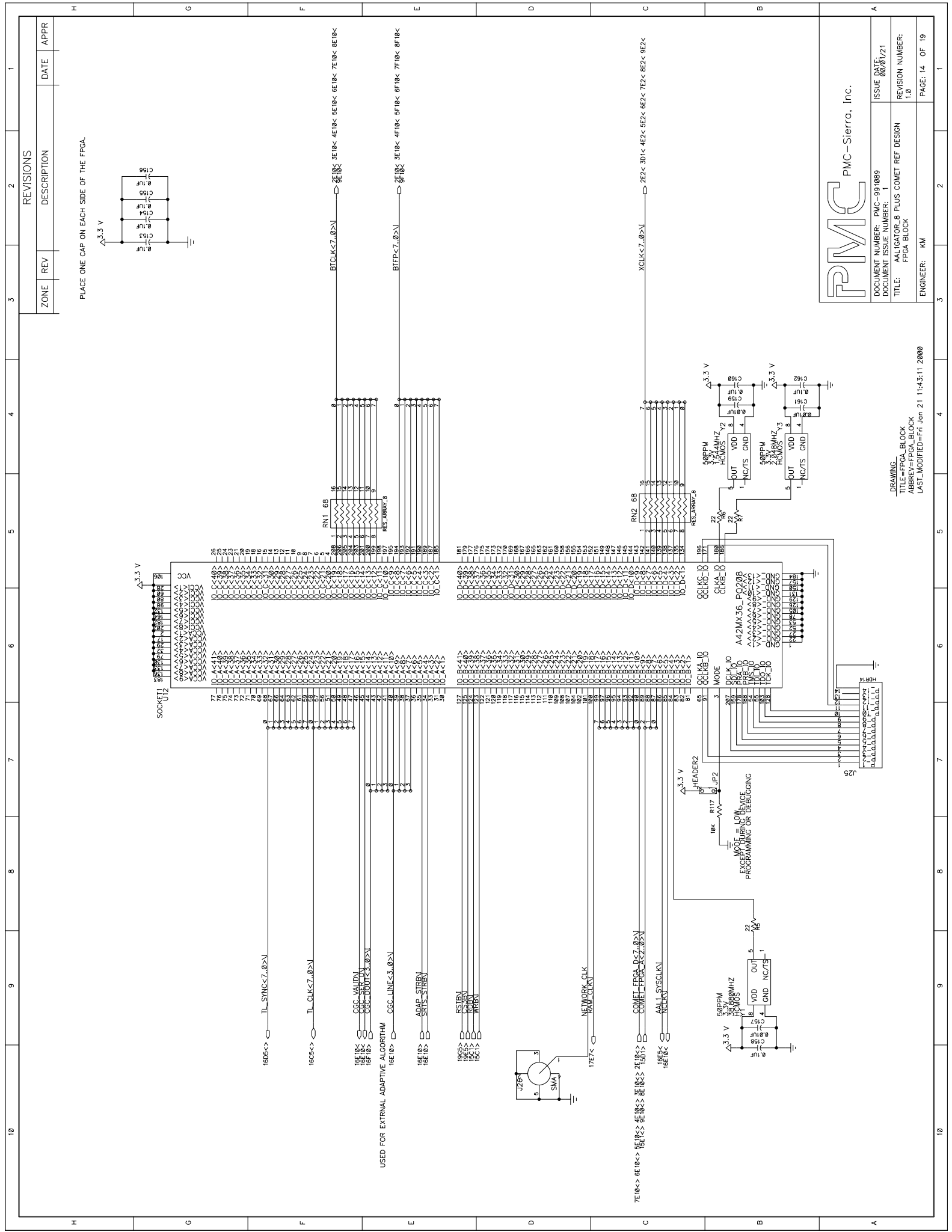
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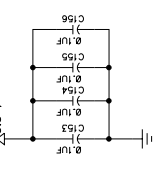
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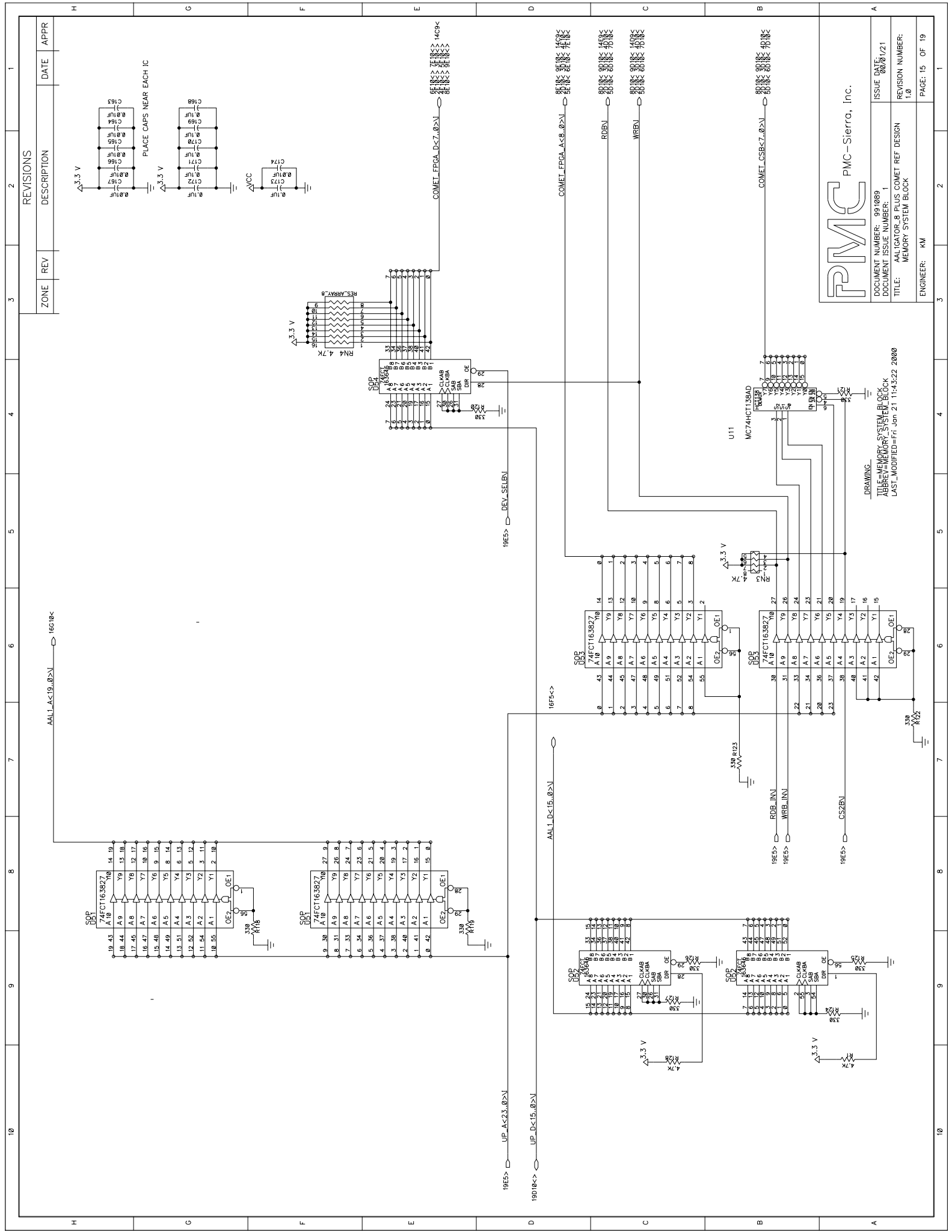


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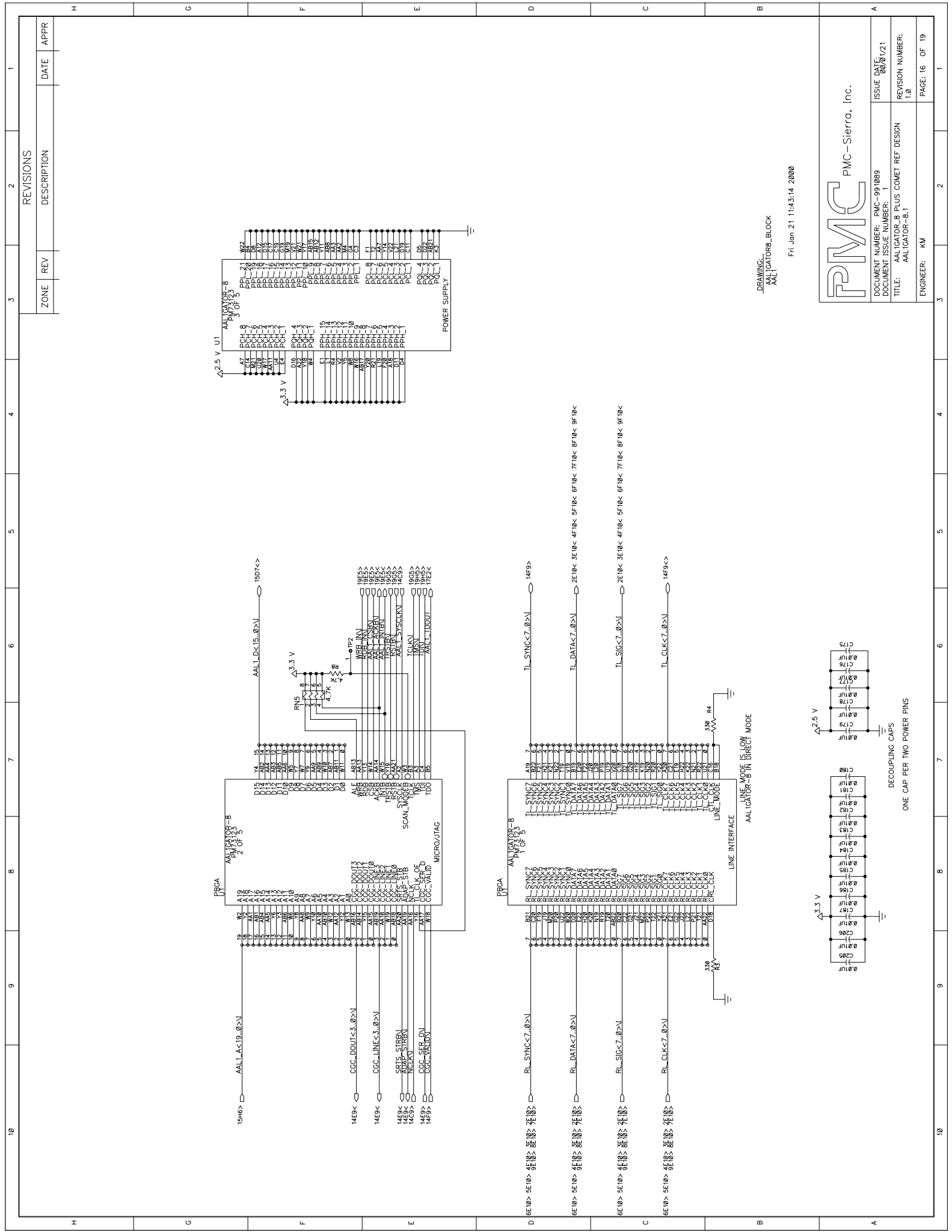
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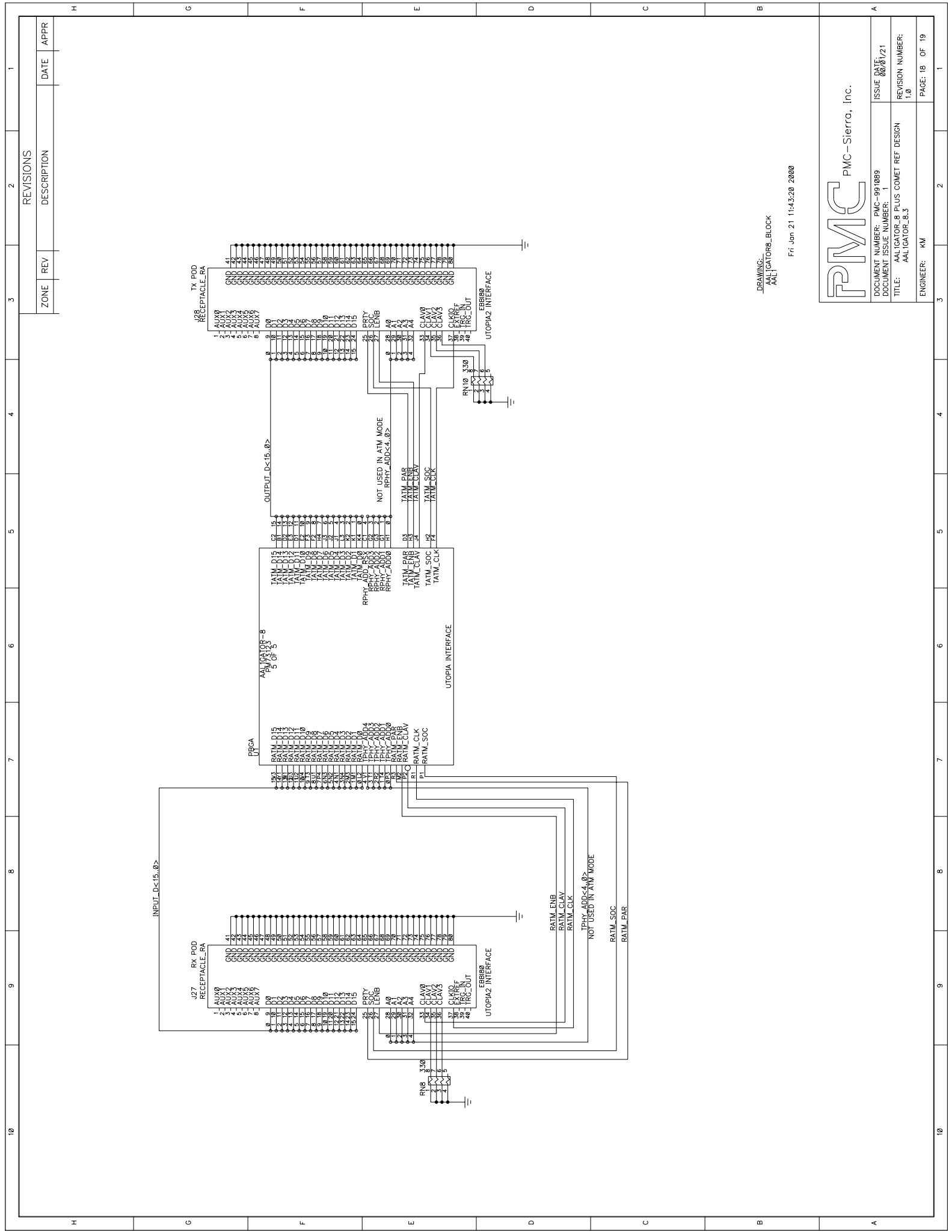
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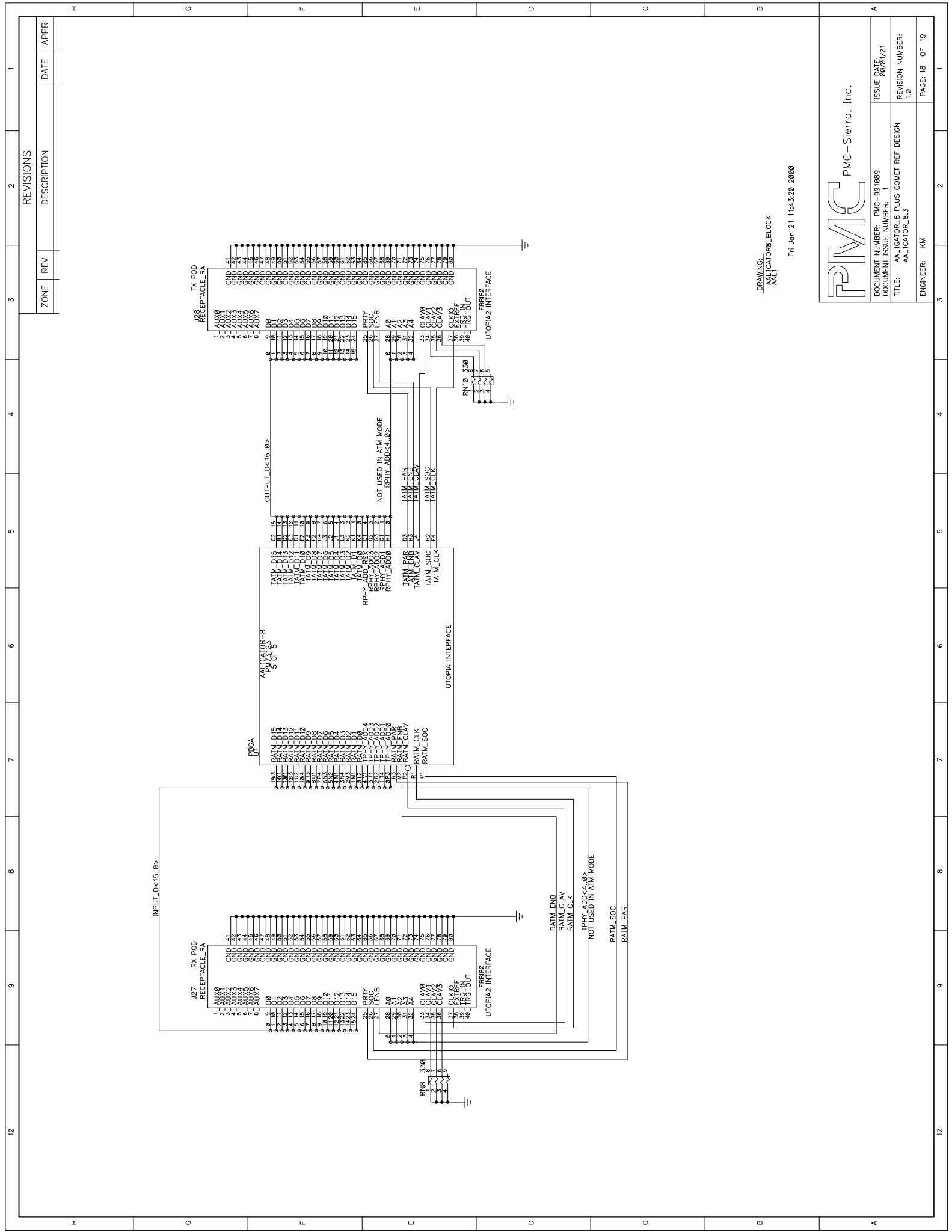
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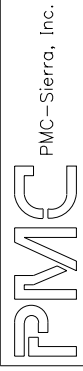


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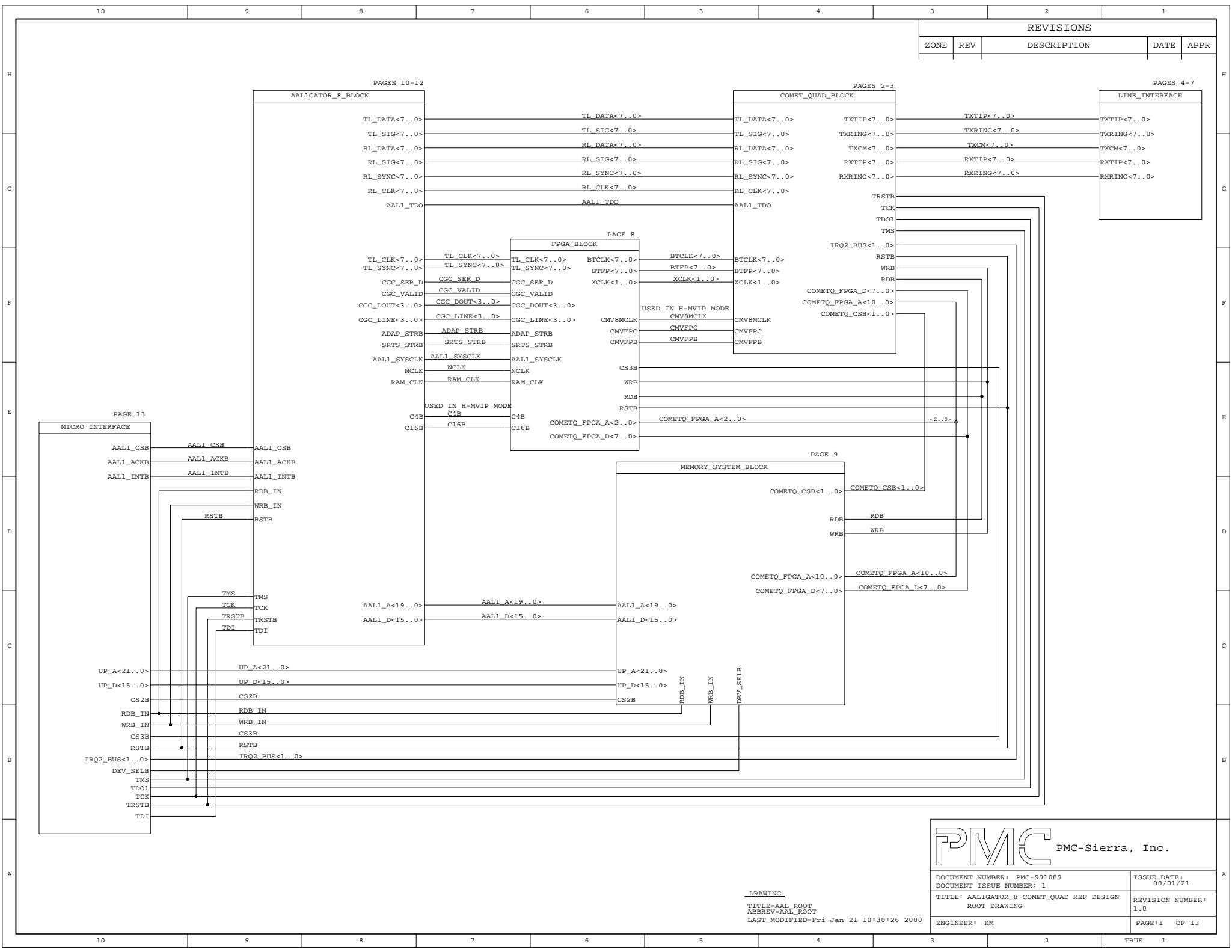
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AAL1GATOR-8 REFERENCE DESIGN

15 APPENDIX D: AAL1GATOR-8 W/COMET-QUADS SCHEMATICS

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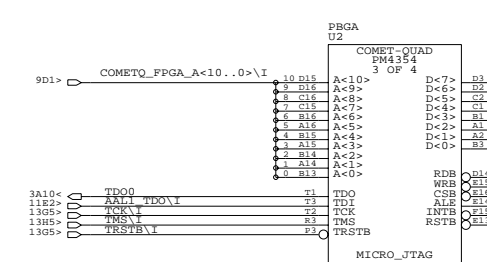
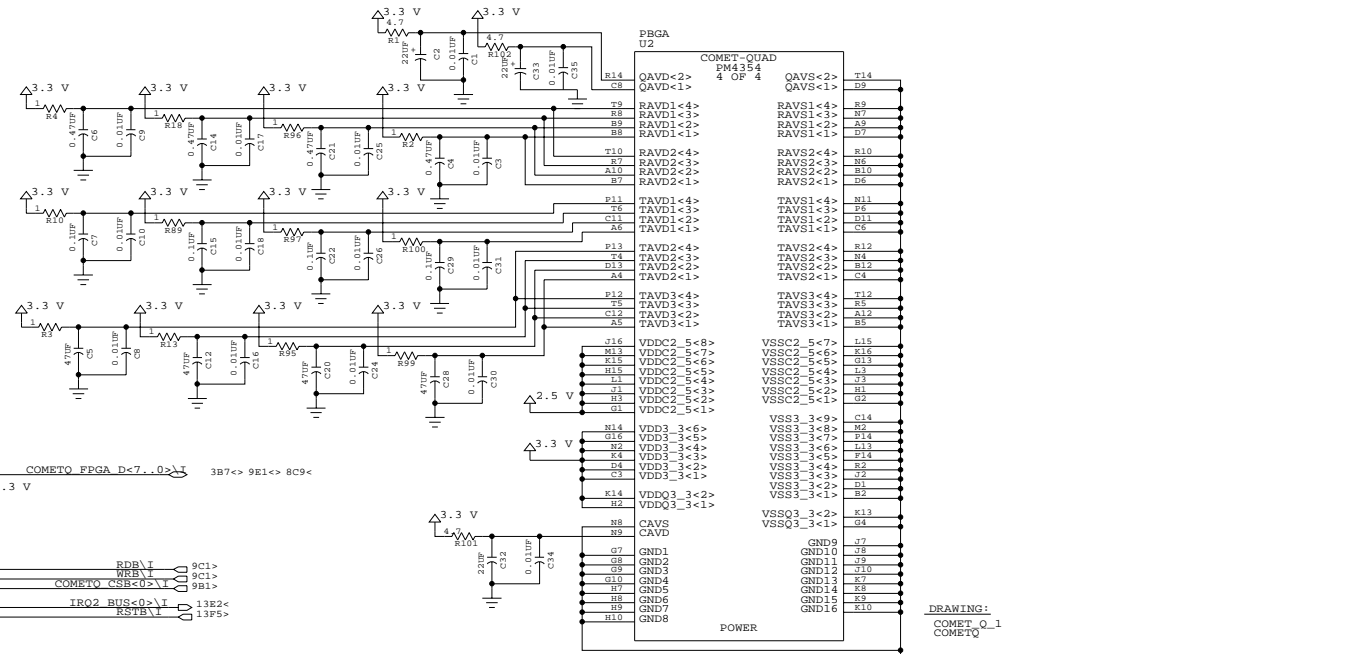
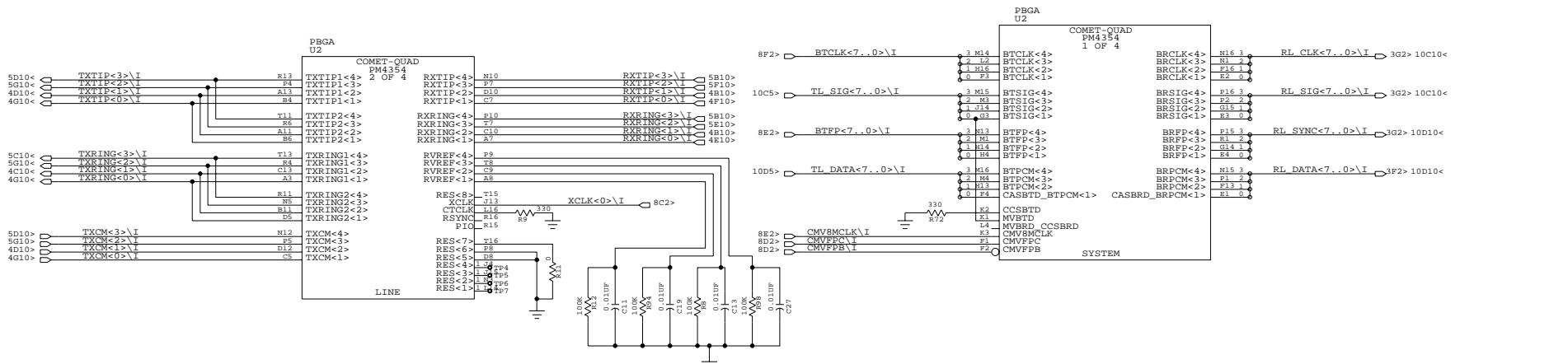
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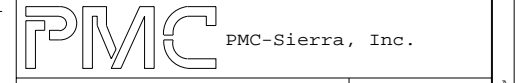
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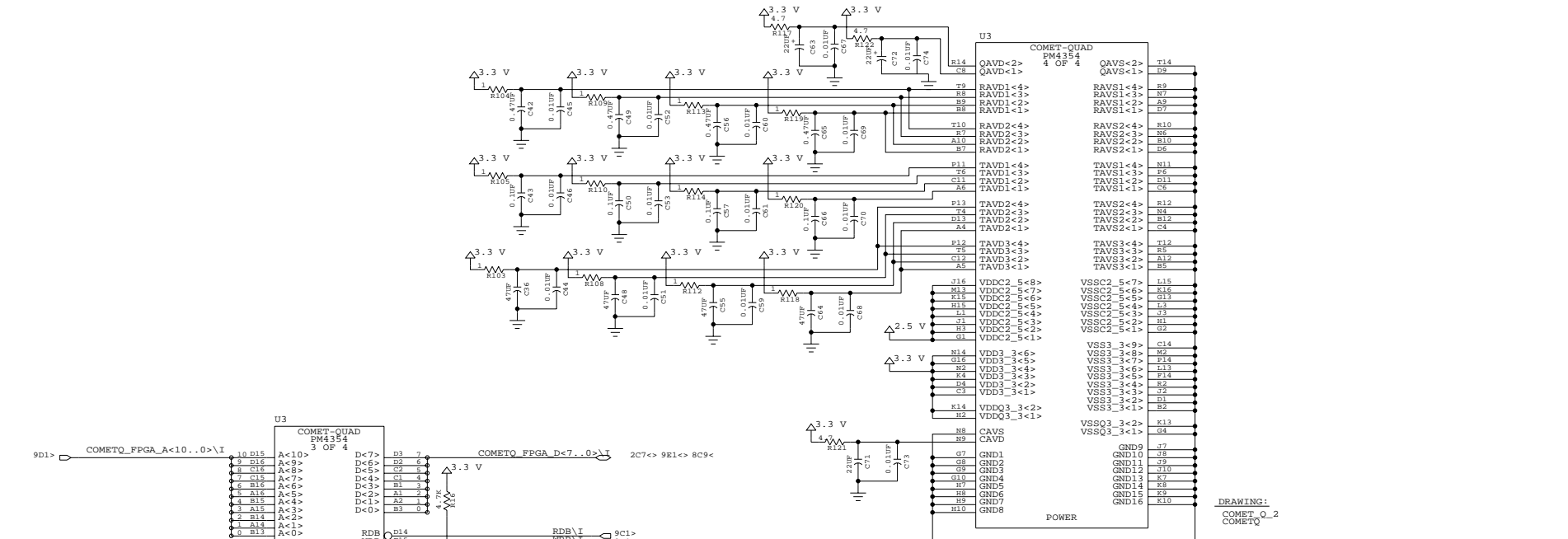
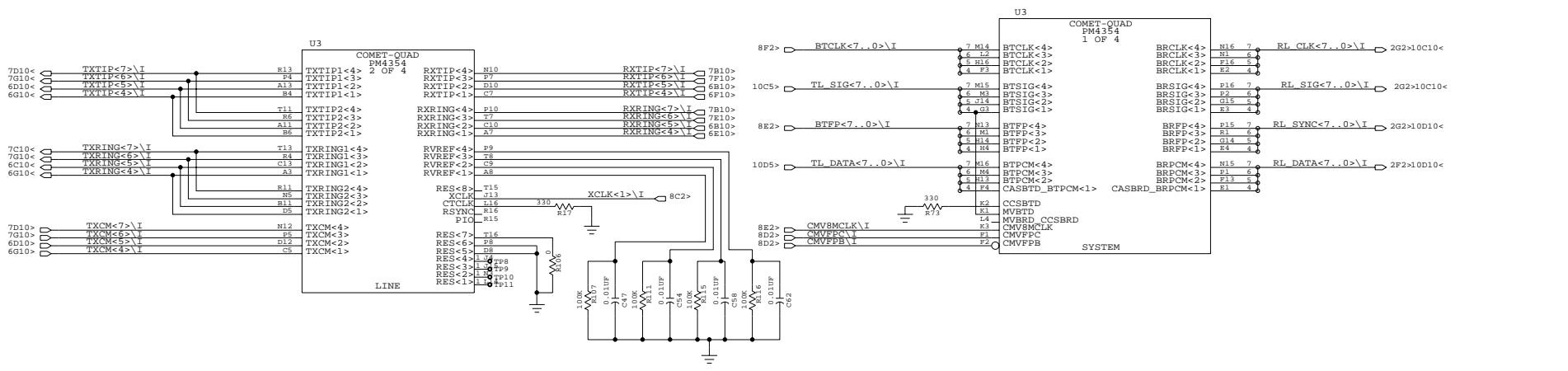


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REVISIONS

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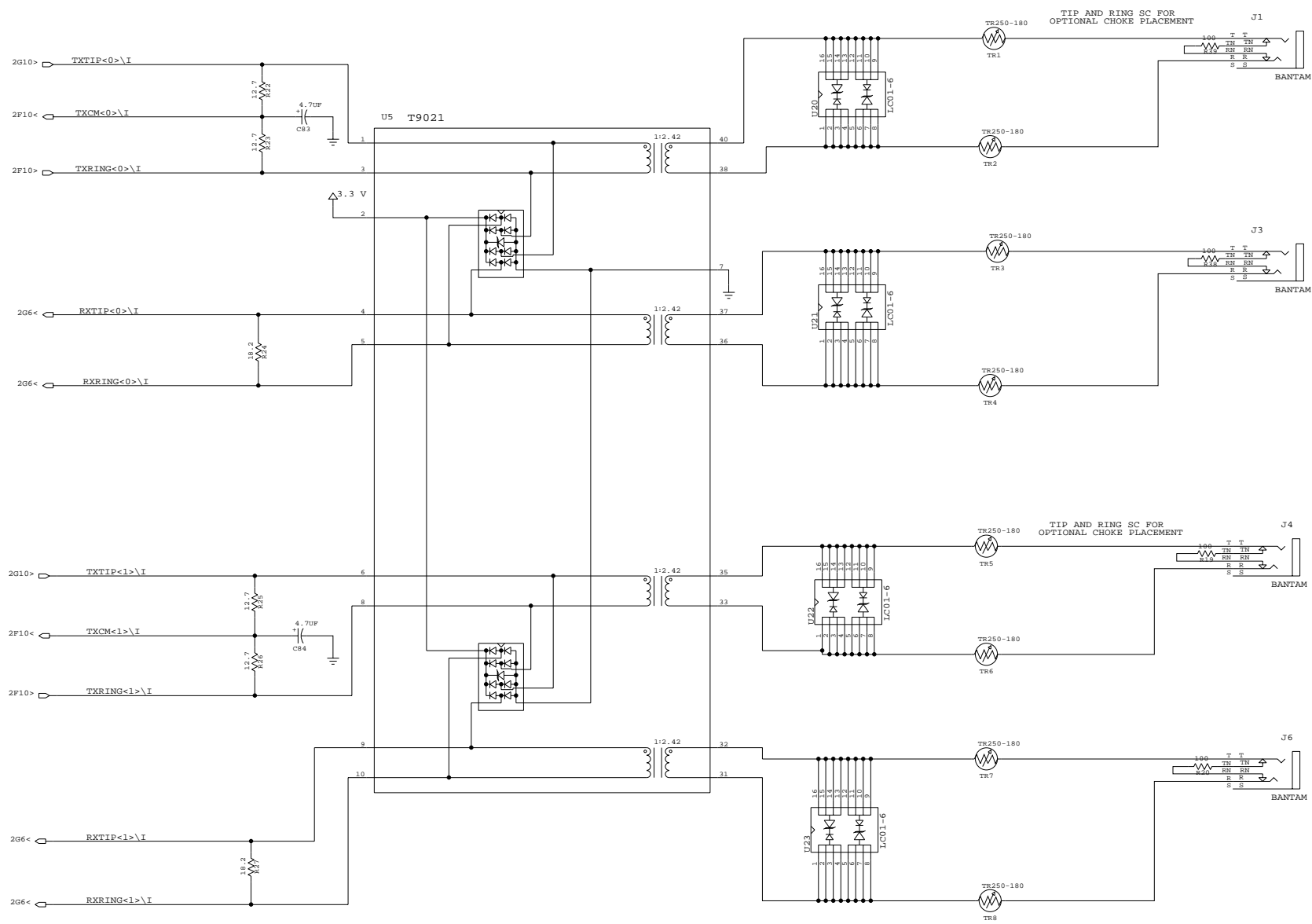
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REVISIONS

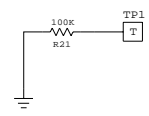
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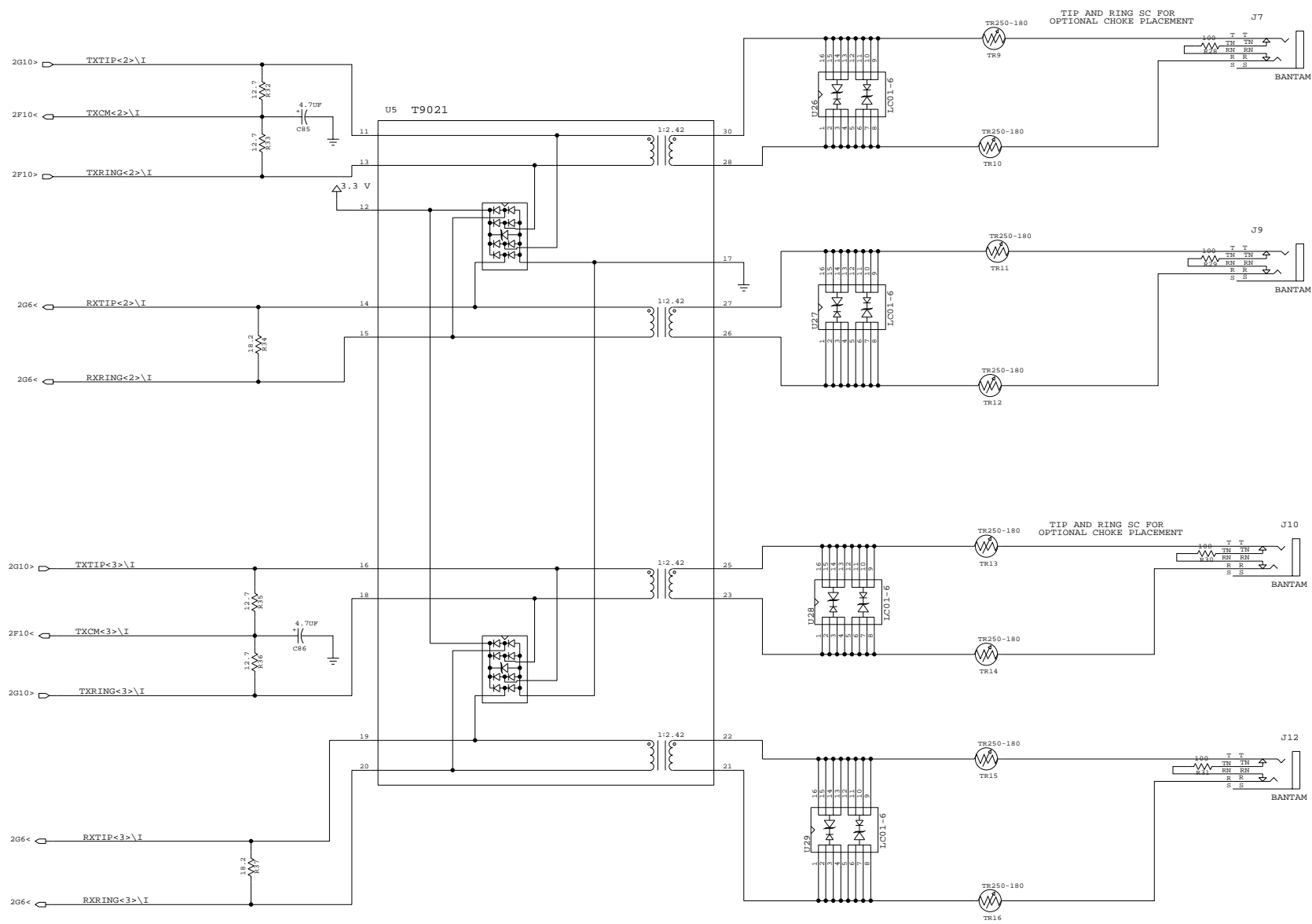


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REVISIONS

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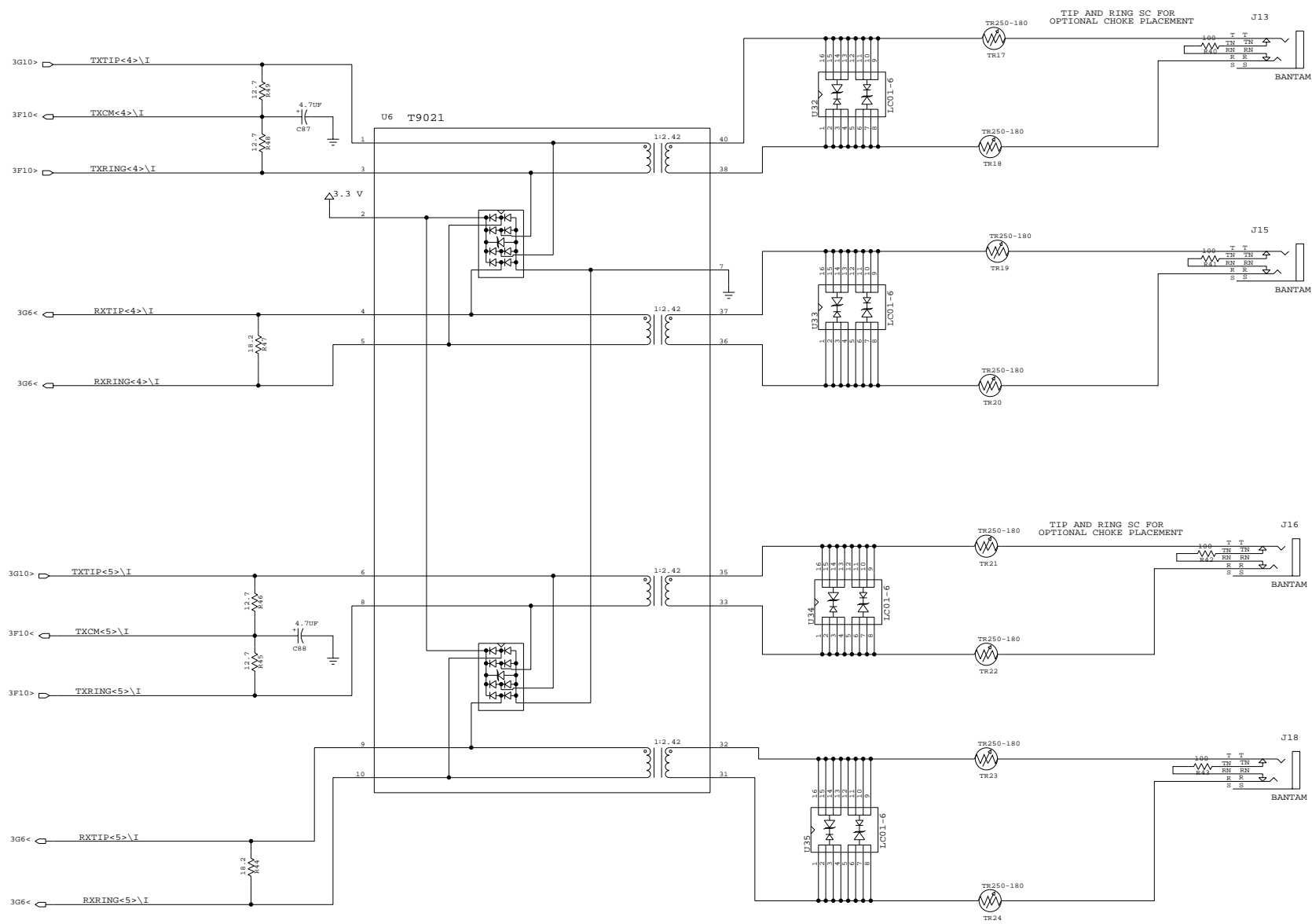


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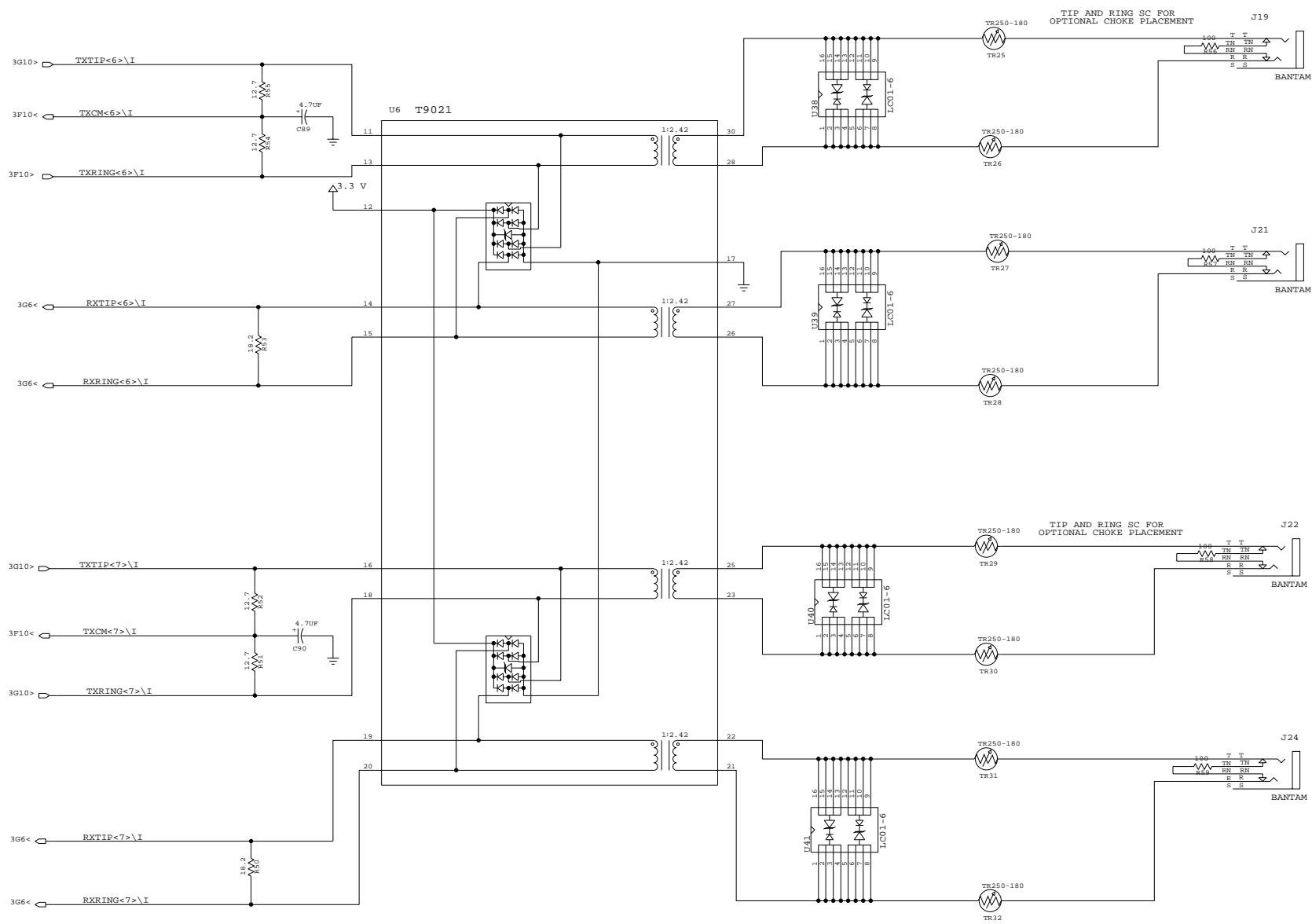


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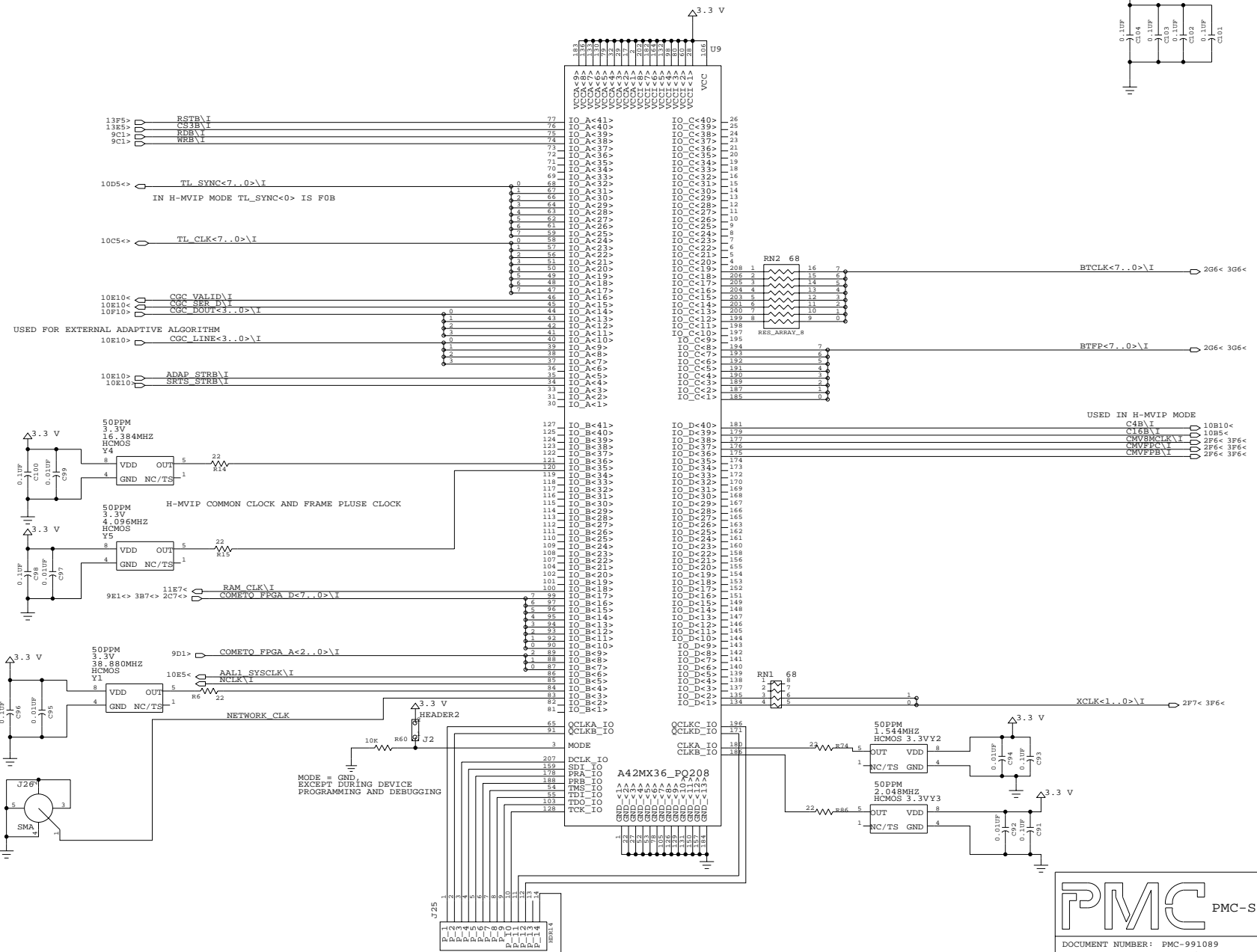
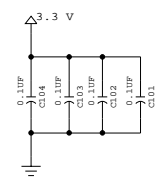
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 LAST_MODIFIED=Thu May 17 11:12:09 2001

DOCUMENT NUMBER: PMC-991089	ISSUE DATE: 00/01/21
DOCUMENT ISSUE NUMBER: 1	REVISION NUMBER: 1.0
TITLE: AALIGATOR_8 COMET_QUAD REF DESIGN LINE INTERFACE 4	PAGE: 7 OF 13
ENGINEER: KM	

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPR
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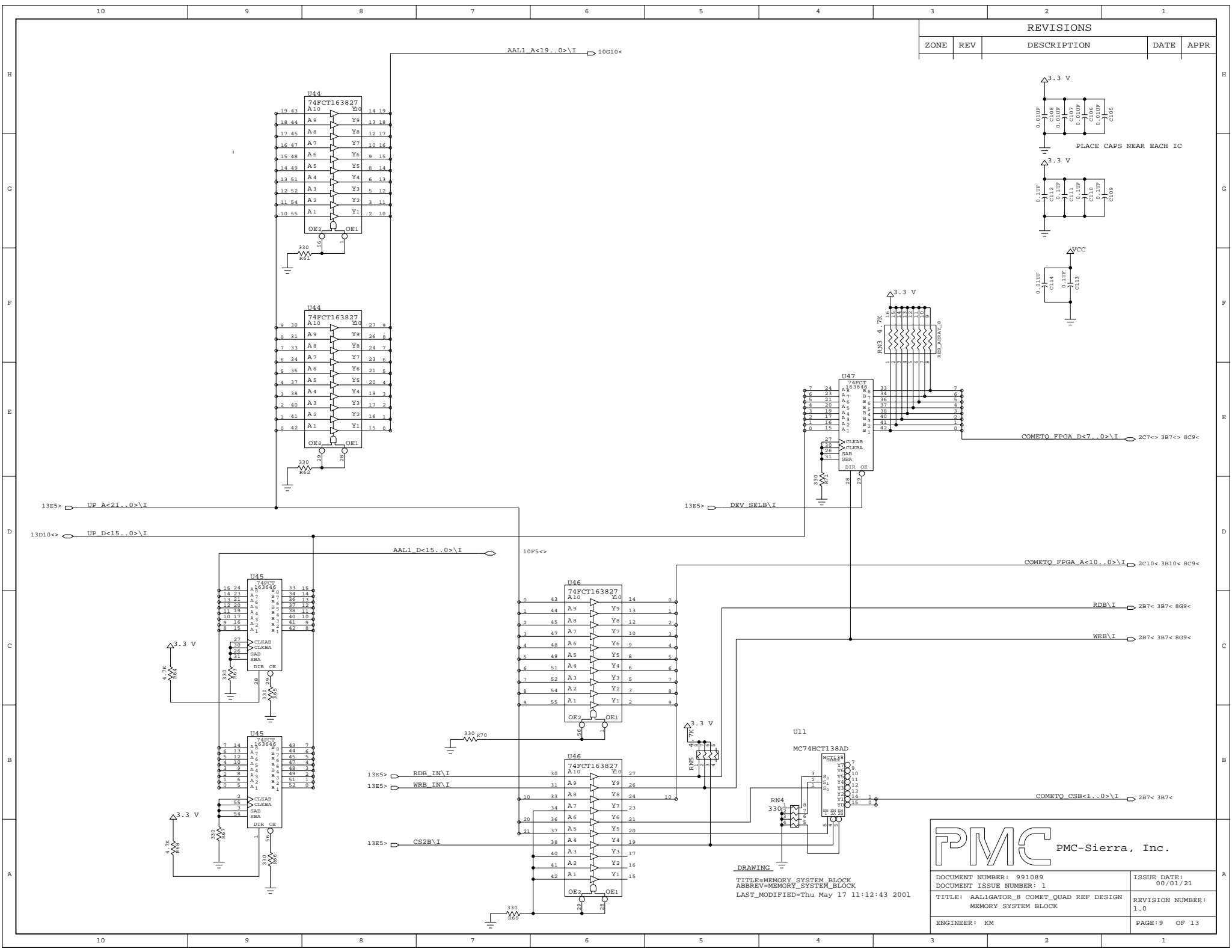
PLACE ONE CAP ON EACH SIDE OF THE FPGA.



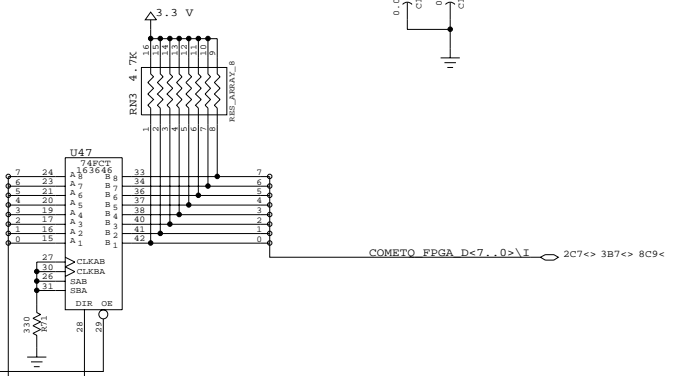
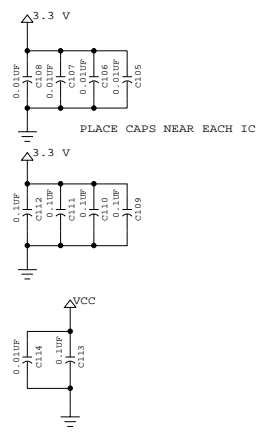
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 ABBREV=FPGA_BLOCK
 LAST_MODIFIED=Thu May 17 11:12:30 2001

PMC PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991089	ISSUE DATE: 00/01/21
DOCUMENT ISSUE NUMBER: 1	REVISION NUMBER: 1.0
TITLE: AALIGATOR_8 COMET_QUAD REF DESIGN FPGA BLOCK	ENGINEER: KM
PAGE: 8 OF 13	



REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

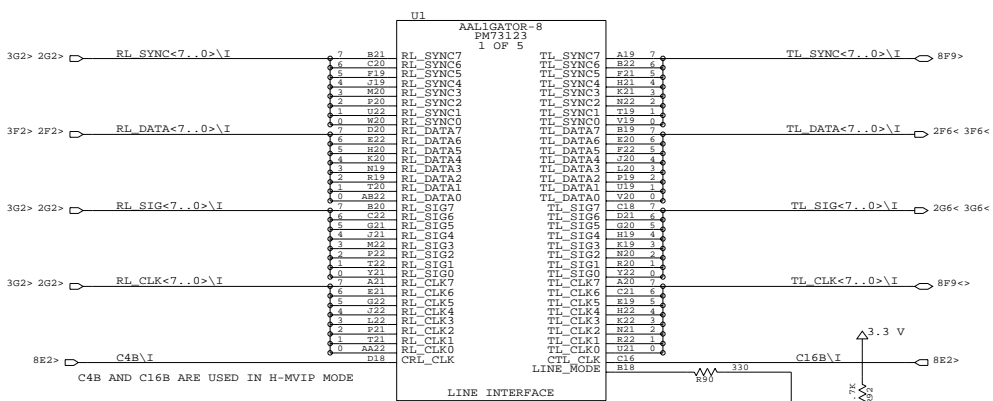
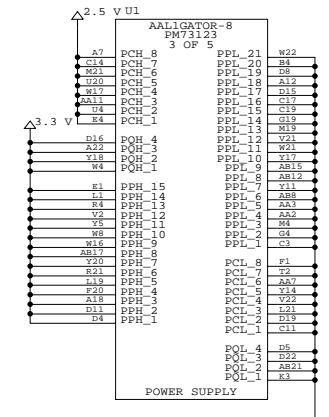
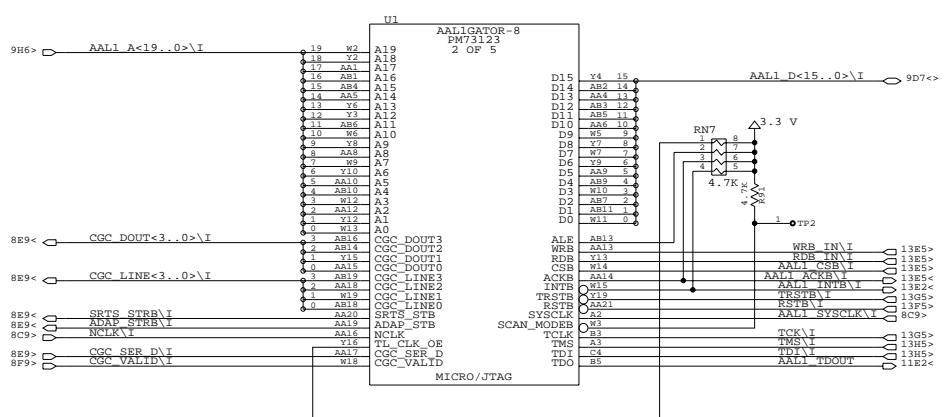


DRAWING
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 ABBREV: MEMORY_SYSTEM_BLOCK
 LAST_MODIFIED: Thu May 17 11:12:43 2001

DOCUMENT NUMBER: 991089	ISSUE DATE: 00/01/21
DOCUMENT ISSUE NUMBER: 1	
TITLE: AALLIGATOR_8 COMETO_QUAD REF DESIGN MEMORY_SYSTEM_BLOCK	REVISION NUMBER: 1.0
ENGINEER: KM	PAGE: 9 OF 13

REVISIONS

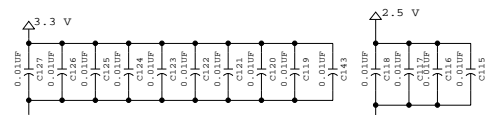
ZONE	REV	DESCRIPTION	DATE	APPR
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LINE_MODE0 = 'GND' WHEN DIRECT MODE
'HIGH' WHEN H-MVIP MODE

DRAWING:
AALIGATOR_8_1.1
AAL1

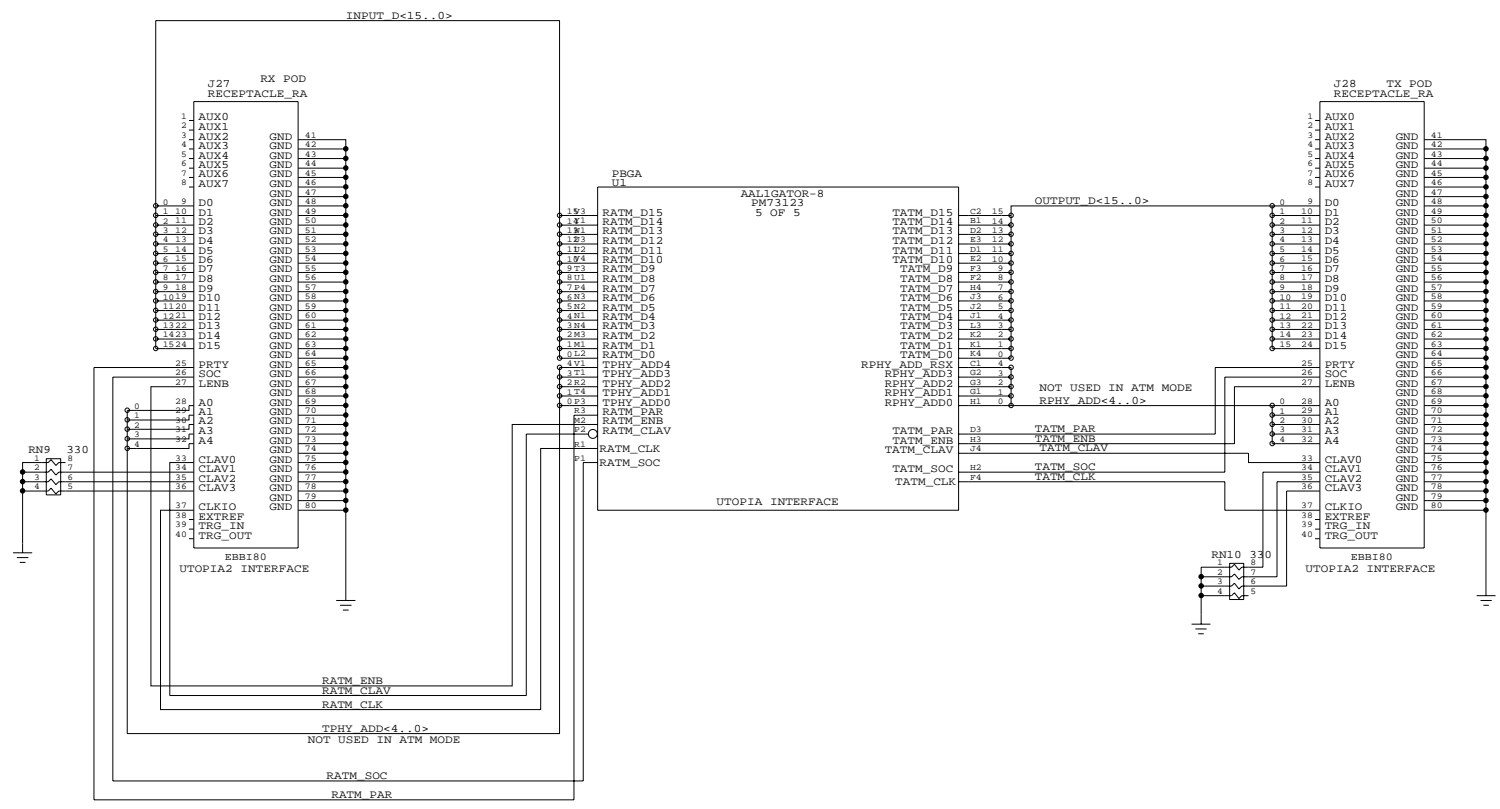
Thu May 17 11:12:34 2001



DOCUMENT NUMBER: PMC-991089	ISSUE DATE: 00/01/21
DOCUMENT ISSUE NUMBER: 1	REVISION NUMBER: 1.0
TITLE: AALIGATOR_8 COMET_QUAD REF DESIGN	PAGE: 10 OF 13
ENGINEER: KM	

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPR



DRAWING:
AALIGATOR_8_1.3
AAL1

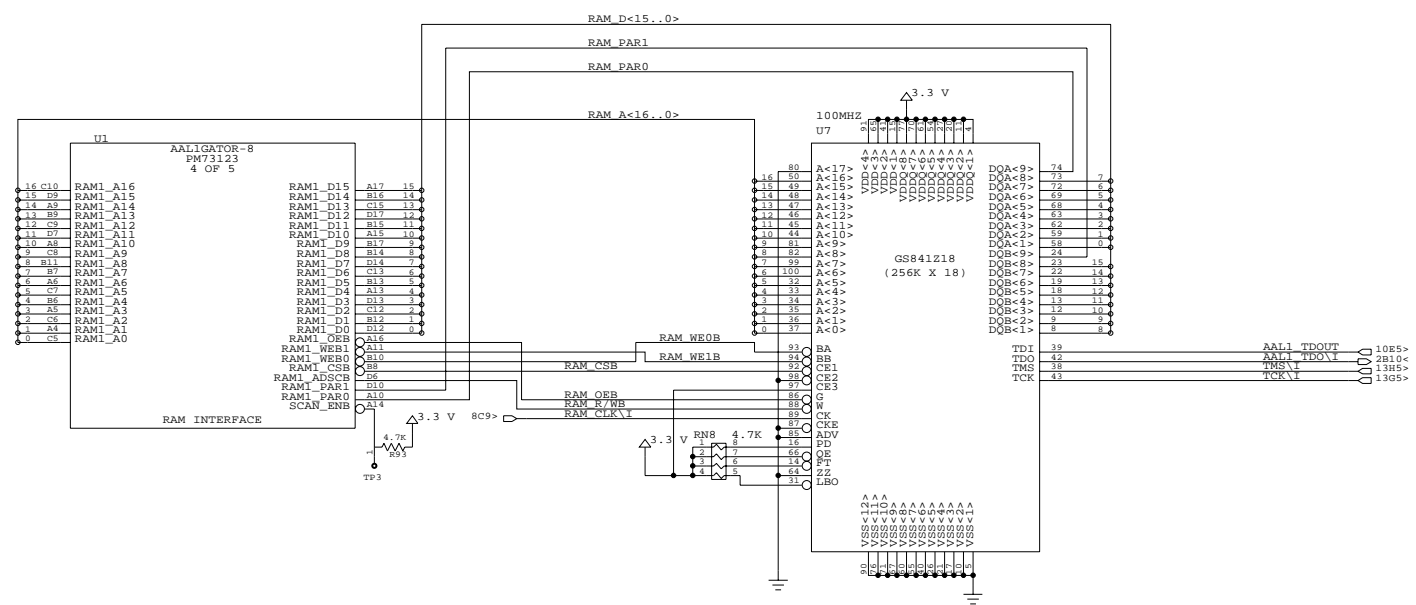
Thu May 17 11:12:40 2001



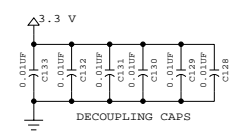
DOCUMENT NUMBER: PMC-991089	ISSUE DATE: 00/01/21
DOCUMENT ISSUE NUMBER: 1	REVISION NUMBER: 1.0
TITLE: AALIGATOR_8 COMET_QUAD REF DESIGN AALIGATOR_8.3	PAGE: 12 OF 13
ENGINEER: KM	

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPR



DRAWING:
 AALIGATOR_8.1.2
 AAL1
 Thu May 17 11:12:37 2001

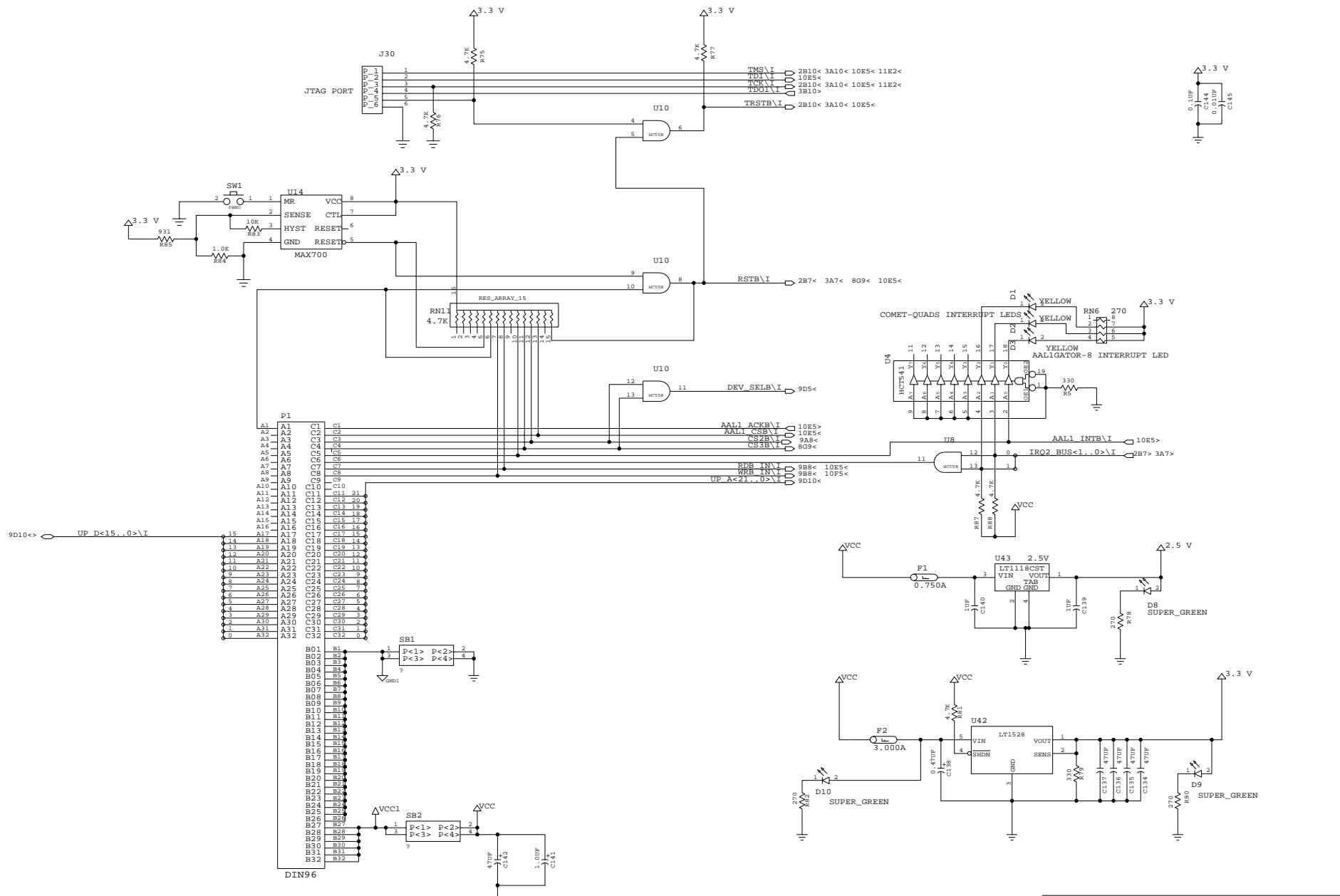


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DOCUMENT NUMBER: PMC-991089	ISSUE DATE: 00/01/21
DOCUMENT ISSUE NUMBER: 1	REVISION NUMBER: 1.0
TITLE: AALIGATOR_8 COMET_QUAD REF DESIGN	ENGINEER: KM
AALIGATOR-8.2	PAGE: 11 OF 13

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPR



CONNECT UNUSED INPUTS TO GND
U10

DRAWING
TITLE=MICRO_INTERFACE
ABBREV=MICRO
LAST_MODIFIED=Thu May 17 11:12:14 2001

PMC PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991089	ISSUE DATE: 00/01/21
DOCUMENT ISSUE NUMBER: 1	REVISION NUMBER: 1.0
TITLE: AALIGATOR_8 COMET_QUAD REF DESIGN	
MICRO_INTERFACE	
ENGINEER: KM	PAGE: 13 OF 13

PRELIMINARY

REFERENCE DESIGN

PMC-1991089



PM73123 AAL1GATOR-8
PM4354 COMET-QUAD

ISSUE 2

AAL1GATOR-8 REFERENCE DESIGN

NOTES

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