TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9490F, TC9490FA

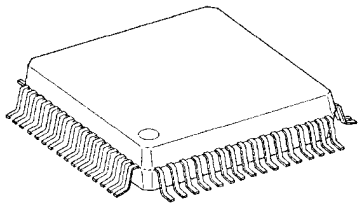
Digital Servo Single-Chip Processor for Use in CD Player

TC9490F/FA is a single-chip processor which incorporates the following functions: sync separation protection, interpolation, EFM decoder, error correction, microcontroller interface, digital equalizer for use in servo LSI, and servo control circuit.

TC9490F/FA also incorporates a 1-bit DA converter.

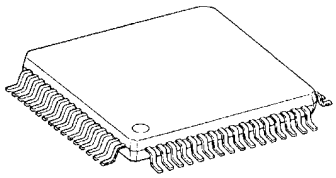
Combining TC9490F with digital servo head amp TA2147F enables very simple and completely adjustment-free CD player systems.

TC9490F



QFP64-P-1414-0.80A

TC9490FA



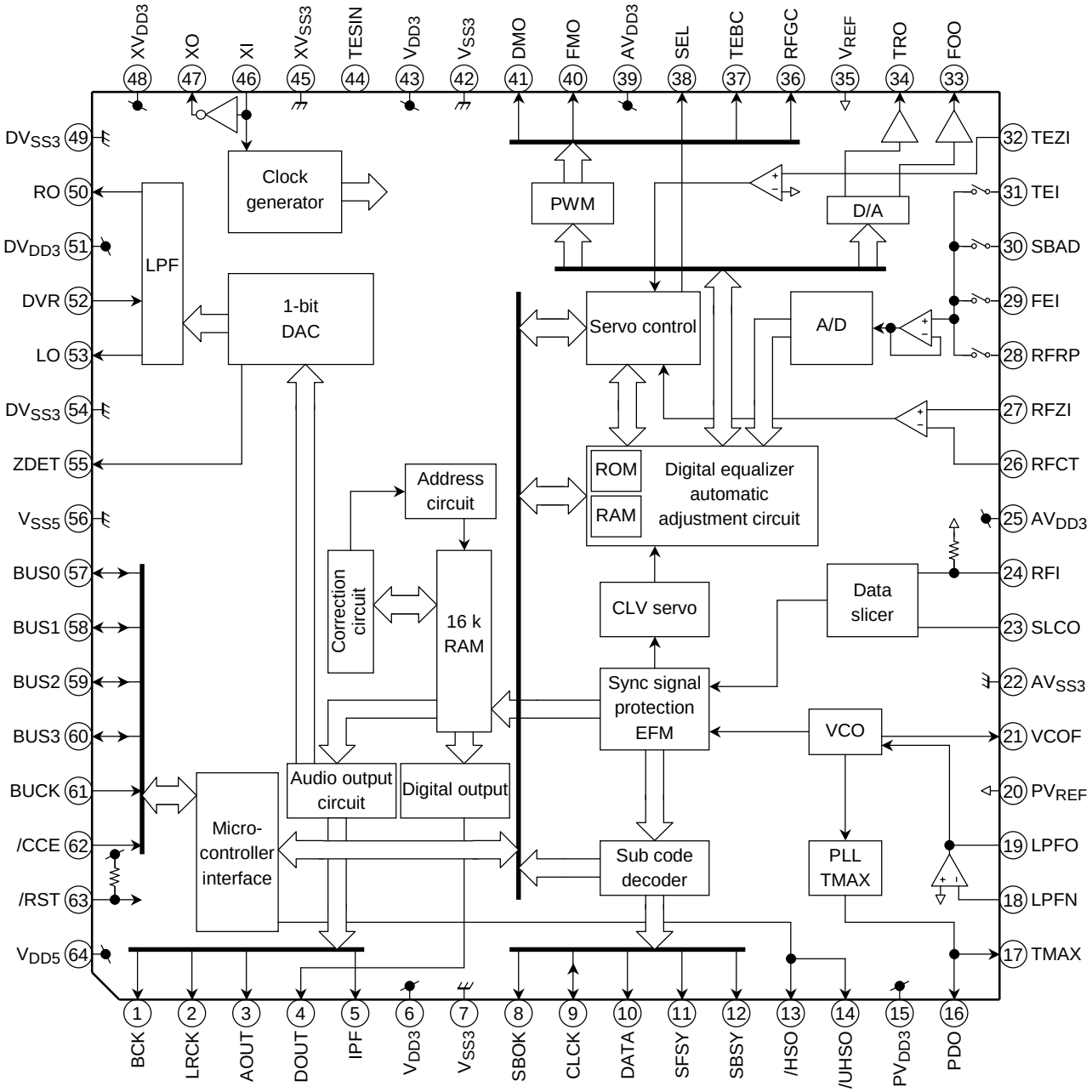
LQFP64-P-1010-0.50

Weight:
QFP64-P-1414-0.80A: 0.5 g (typ.)
LQFP64-P-1010-0.50: 0.4 g (typ.)

Features

- Capable of decoding the text data.
- Sync pattern detection, sync signal protection, and synchronization can be made correctly.
- Built-in EFM demodulation circuit and subcode demodulation.
- Capable of correcting dual C1 correction and quadruple C2 correction using the CIRC correction theoretical format.
- The TC9490F respond to variable playback system.
- Jitter absorbing capacity of ±6 frame.
- Built-in 16 k RAM.
- Built-in digital out circuit.
- Built-in L/R independent digital attenuator.
- Audio output responds to bilingual function.
- Output format for audio out can be selected 32fs, 48fs or 64fs modes.
- Read-timing-free subcode Q data and capable of synchronous output with audio data.
- Built-in data slicer and analog PLL (adjustment-free VCO).
- Capable of automatic adjustment function of focus and tracking servos for loop gain, offset and balance.
- Built-in RF gain automatic adjustment circuit.
- Built-in digital equalizer for phase compensation.
- Built-in RAM for digital equalizer for coefficient, and capable of variable pickup.
- Built-in focus and tracking servo control circuit.
- Search control corresponds to every mode and can realize high speed and stable search.
- Lens-kick and feed-kick are using speed controlled form.
- Built-in AFC and APC circuits for CLV servo of disc motor.
- Built-in anti-defect and anti-shock circuit.
- Built-in 8 times oversampling digital filter and 1-bit DA converter.
- Built-in analog filter for 1-bit DA converter.
- Built-in zero data detection output circuit.
- The TC9490F/FA capable of 4 times speed operation.
- Built-in microcontroller interface circuit.
- CMOS silicon structure and high speed, low power consumption.
- 64-pin flat package.

Block Diagram (top view)



Pin Functions

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Function Description</th><th>Remarks</th></tr>
<tr><td>1</td><td>BCK</td><td>O
3-5I/F</td><td>Bit clock output pin. 32fs, 48fs, or 64fs selectable by command.</td><td>Normal speed:
32fs = 1.4112 MHz</td></tr>
<tr><td>2</td><td>LRCK</td><td>O
3-5I/F</td><td>L/R channel clock output pin. “L” for L channel and “H” for R channel. Output polarity can be inverted by command.</td><td>Normal speed: 44.1 kHz</td></tr>
<tr><td>3</td><td>AOUT</td><td>O
3-5I/F</td><td>Audio data output pin. MSB-first or LSB-first selectable by command.</td><td>—</td></tr>
<tr><td>4</td><td>DOUT</td><td>O
3-5I/F</td><td>Digital data output pin. Outputs up to double-speed playback.</td><td>Based on CP-1201</td></tr>
<tr><td>5</td><td>IPF</td><td>O
3-5I/F</td><td>Correction flag output pin. When set to “H”, AOUT output cannot be corrected by C2 correction processing.</td><td>Alias: C2PO</td></tr>
<tr><td>6</td><td>V_{DD3}</td><td>—</td><td>Digital 3.3 V power supply voltage pin.</td><td>—</td></tr>
<tr><td>7</td><td>V_{SS3}</td><td>—</td><td>Digital GND pin.</td><td>—</td></tr>
<tr><td>8</td><td>SBOK</td><td>O
3-5I/F</td><td>Subcode Q data CRCC result output pin. “H” level when result is OK.</td><td>—</td></tr>
<tr><td>9</td><td>CLCK</td><td>I/O
3-5I/F</td><td>Subcode P-W data read clock I/O pin. I/O polarity selectable by command.</td><td>Schmit input</td></tr>
<tr><td>10</td><td>DATA</td><td>O
3-5I/F</td><td>Subcode P-W data output pin.</td><td>—</td></tr>
<tr><td>11</td><td>SFSY</td><td>O
3-5I/F</td><td>Playback frame sync signal output pin.</td><td>—</td></tr>
<tr><td>12</td><td>SBSY</td><td>O
3-5I/F</td><td>Subcode block sync signal output pin. “H” level at S1 when subcode sync is detected.</td><td>—</td></tr>
<tr><td>13</td><td>/HSO</td><td>O
3-5I/F</td><td rowspan="2">Playback speed mode flag output pins.
<table>
<tr><th>/UHSO</th><th>/HSO</th><th>Playback Speed</th></tr>
<tr><td>H</td><td>H</td><td>Normal</td></tr>
<tr><td>H</td><td>L</td><td>Double</td></tr>
<tr><td>L</td><td>L</td><td>4 times</td></tr>
<tr><td>—</td><td>—</td><td>—</td></tr>
</table></td><td>—</td></tr>
<tr><td>14</td><td>/UHSO</td><td>O
3-5I/F</td><td>—</td></tr>
<tr><td>15</td><td>P_{VDD3}</td><td>—</td><td>PLL-only 3.3 V power supply voltage pin.</td><td>—</td></tr>
<tr><td>16</td><td>PDO</td><td>O
AI/F</td><td>EFM and PLCK phase difference signal output pin.</td><td>3-state output
(PV_{DD3}, PV_{REF}, AV_{SS3})</td></tr>
<tr><td>17</td><td>TMAX</td><td>O
AI/F</td><td>TMAX detection result output pin.
<table>
<tr><th>TMAX Detection Result</th><th>TMAX Output</th></tr>
<tr><td>Longer than fixed period</td><td>“PV_{DD3}”</td></tr>
<tr><td>Within fixed period</td><td>“HiZ”</td></tr>
<tr><td>Shorter than fixed period</td><td>“AV_{SS3}”</td></tr>
</table></td><td>3-state output
(PV_{DD3}, HiZ, AV_{SS3})</td></tr>
<tr><td>18</td><td>LPFN</td><td>I
AI/F</td><td>inverted input pin for PLL LPF amp.</td><td>Analog input</td></tr>
<tr><td>19</td><td>LPFO</td><td>O
AI/F</td><td>Output pin for PLL LPF amp.</td><td>Analog output</td></tr>
<tr><td>20</td><td>P_{VREF}</td><td>—</td><td>PLL-only V_{REF} pin.</td><td>—</td></tr>
<tr><td>21</td><td>VCOF</td><td>O
AI/F</td><td>VCO filter pin.</td><td>Analog output</td></tr>
</table>

Pin No.	Symbol	I/O	Function Description	Remarks
22	AV_{SS3}	—	Analog GND pin.	—
23	SLCO	O AI/F	DAC output pin for data slice level generation.	Analog output
24	RFI	I AI/F	RF signal input pin. Zin selectable by command.	Analog input
25	A_{VDD3}	—	Analog 3.3 V power supply voltage pin.	—
26	RFCT	I AI/F	RFRP signal center level input pin.	Analog input: Zin = 33 kΩ
27	RFZI	I AI/F	RFRP signal zero-cross input pin.	Analog input
28	RFRP	I AI/F	RF ripple signal input pin.	Analog input
29	FEI	I AI/F	Focus error signal input pin.	Analog input
30	SBAD	I AI/F	Sub-beam adder signal input pin.	Analog input
31	TEI	I AI/F	Tracking error input pin. Inputs when tracking servo is on.	Analog input
32	TEZI	I AI/F	Tracking error signal zero-cross input pin.	Analog input: Zin = 10 kΩ
33	FOO	O	Focus equalizer output pin.	Analog output (AV_{SS3}~AV_{DD3})
34	TRO	O AI/F	Tracking equalizer output pin.	
35	V_{REF}	—	Analog reference power supply voltage pin.	—
36	RFGC	O AI/F	RF amplitude adjustment control signal output pin.	3-state output (PWM carrier = 88.2 kHz) (AV_{DD3}, V_{REF}, AV_{SS3})
37	TEBC	O AI/F	Tracking balance control signal output pin.	
38	SEL	O AI/F	APC circuit ON/OFF signal output pin. At laser on, high impedance with UHS = “L”, H output with UHS = “H”.	3-state output
39	A_{VDD3}	—	Analog 3.3 V power supply voltage pin.	—
40	FMO	O AI/F	Feed equalizer output pin.	3-state output (PWM carrier = 88.2 kHz) (AV_{DD3}, V_{REF}, AV_{SS3})
41	DMO	O AI/F	Disc equalizer output pin.	
42	V_{SS3}	—	Digital GND pin.	—
43	V_{DD3}	—	Digital 3.3 V power supply voltage pin.	—
44	TESIN	I 3I/F	Test input pin. Normally, fixed to “L”.	—
45	XV_{SS3}	—	System clock oscillator GND pin.	—
46	XI	I AI/F	System clock oscillator input pin.	—
47	XO	O AI/F	System clock oscillator output pin.	—
48	XV_{DD3}	—	System clock oscillator 3.3 V power supply voltage pin.	—
49	DV_{SS3}	—	DA converter GND pin.	—
50	RO	O AI/F	R-channel data forward output pin.	—
51	DV_{DD3}	—	DA converter 3.3 V power supply pin.	—
52	DVR	—	Reference voltage pin.	—
53	LO	O AI/F	L-channel data forward output pin.	—

Pin No.	Symbol	I/O	Function Description	Remarks
54	D_{VSS3}	—	DA converter GND pin.	—
55	ZDET	O 3-5I/F	1 bit DA converter zero data detection flag output pin.	—
56	V_{SS5}	—	Microcontroller interface GND pin.	—
57	BUS0	I/O 3-5I/F	Microcontroller interface data I/O pins.	Schmit input CMOS ports
58	BUS1			
59	BUS2			
60	BUS3			
61	BUCK	I 3-5I/F	Microcontroller interface clock input pin.	Schmit input
62	/CCE	I 3-5I/F	Microcontroller interface chip enable signal input pin. At “L”, BUS0 to BUS3 are active.	Schmit input
63	/RST	I 3-5I/F	Reset signal input pin. At reset, “L”.	Built-in pull-up resistor
64	V_{DD5}	—	Microcontroller interface 5 V power supply pin.	—

Note: AI/F: analog input/output pin
3-5I/F: 3-5 interface built-in pin (5 V input/output pin)
3I/F: 3 V input/output pin

Maximum Ratings (unless otherwise specified, GND reference, Ta = 25°C)

Characteristics	Symbol	Rating	Unit	Remarks
Power supply voltage	V_{DD5}	−0.3~6.0	V	64-56 pin
	V_{DD3}	−0.3~4.5		6-7 pin 15, 25, 39-22 pin 43-42 pin 48-45 pin 51-49, 54 pin
Input voltage	V_{IN5}	−0.3~ V_{DD5} + 0.3	V	57~63, (9) pin
	V_{IN3}	−0.3~ V_{DD3} + 0.3		18, 24, 26, 27, 28, 29, 30, 31, 32, 44 pin
Power dissipation	P_D	1250	mW	TC9490F
		1170		TC9490FA
Operating temperature	T_{opr}	−40~+85	°C	—
Storage temperature	T_{stg}	−55~+150	°C	—

Electrical Characteristics (unless otherwise specified, V_{DD5} = 5 V, V_{DD3} = AV_{DD3} = DV_{DD3} = XV_{DD3} = PV_{DD3} = 3.3 V, Ta = 25°C)

DC Characteristics

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Operating power supply voltage		V_{DD5}	—	—		4.5	5.0	5.5	V
		V_{DD3}	—	—		3.0	3.3	3.6	
		AV_{DD3}	—	—					
		DV_{DD3}	—	—					
		XV_{DD3}	—	—					
		PV_{DD3}	—	—					
Operating power supply current	Normal speed	I_{DD5}	—	XI = 16.9344 MHz		—	2	5	mA
		I_{DD3}	—			—	30	50	
	Double speed	I_{DD5}	—			—	2.5	6	
		I_{DD3}	—			—	35	60	
	4 times speed	I_{DD5}	—			—	3	7	
		I_{DD3}	—			—	40	70	
Input voltage 1	"H" level	V_{IH5}	—	CMOS input pins except for analog input pins (5 V)		3.5	—	—	V
	"L" level	V_{IL5}	—			—	—	1.5	
Input current 1	"H" level	I_{IH5}	—	V_{IH5} = 5 V		—	—	1.0	μA
	"L" level	I_{IL5}	—	V_{IL5} = 0 V		−1.0	—	—	
Tri-state leak current 1	"H" level	I_{TLH5}	—	V_{IH5} = 5 V	Pins grouped as 1, 2, 3 in the following table	—	—	1.0	μA
	"L" level	I_{TLL5}	—	V_{IL5} = 0 V		−1.0	—	—	
Output current 1	"H" level	I_{OH5}	—	V_{OH5} = 4.6 V	Pins grouped as 1 in the following table	—	—	−2.0	mA
	"L" level	I_{OL5}	—	V_{OL5} = 0.4 V		2.0	—	—	
	"H" level	I_{OH5}	—	V_{OH5} = 4.6 V	Pins grouped as 2 and 3 in the following table	—	—	−4.0	
	"L" level	I_{OL5}	—	V_{OL5} = 0.4 V		4.0	—	—	
Input voltage 2	"H" level	V_{IH3}	—	CMOS input pins except for analog input pins (3 V)		2.3	—	—	V
	"L" level	V_{IL3}	—			—	—	1.0	
Input current 2	"H" level	I_{IH3}	—	V_{IH3} = 3.3 V		—	—	1.0	μA
	"L" level	I_{IL3}	—	V_{IL3} = 0 V		−1.0	—	—	
Tri-state leak current 2	"H" level	I_{TLH3}	—	V_{IH3} = 3.3 V	Pins grouped as 4 and 5 in the following table	—	—	1.0	μA
	"L" level	I_{TLL3}	—	V_{IL3} = 0 V		−1.0	—	—	
Output current 2	"H" level	I_{OH3}	—	V_{OH3} = 2.9 V	Pins grouped as 4 in the following table	—	—	−2.0	mA
	"L" level	I_{OL3}	—	V_{OL3} = 0.4 V		2.0	—	—	
	"H" level	I_{OH3}	—	V_{OH3} = 2.9 V	Pins grouped as 5 in the following table	—	−80	—	μA
	"L" level	I_{OL3}	—	V_{OL3} = 0.4 V		—	80	—	
	"H" level	I_{OH3}	—	V_{OH3} = 2.9 V	Pins grouped as 6 in the following table	—	−121	—	
	"L" level	I_{OL3}	—	V_{OL3} = 0.4 V		—	121	—	
V_{REF} output on resistance		R_{ON}	—	—		—	—	500	Ω
Pull-up resistance		R_{UP}	—	Pins grouped as 8 in the following table		25	50	75	kΩ
Pin built-in output resistance		R_{O1}	—	Pins grouped as 5 in the following table		—	5.0	—	kΩ
		R_{O2}	—	Pins grouped as 6 and 7 in the following table		—	3.3	—	

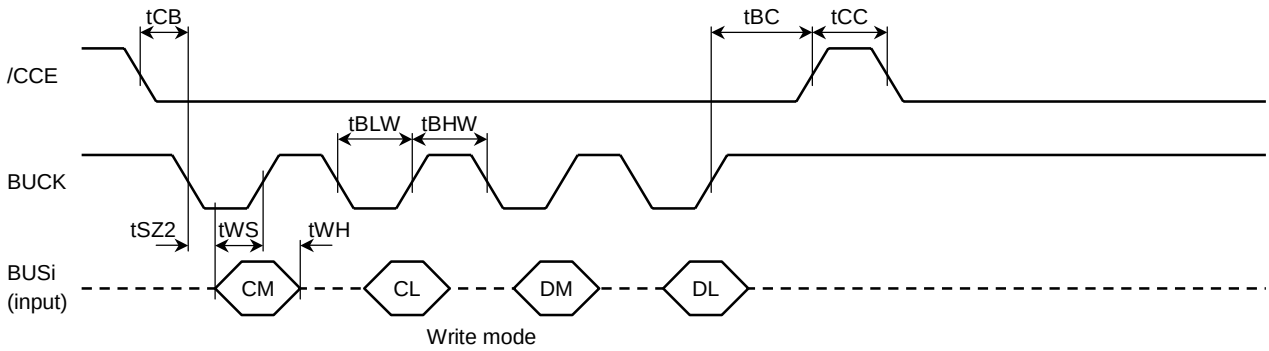
Pin Group	Pin Name
1	SBOK, SFSY, SBSY, /HSO, /UHSO, ZDET
2	BCK, LRCK, AOUT, DOUT, IPF, CLCK, DATA
3	BUS3, BUS2, BUS1, BUS0
4	SEL, TMAX
5	PDO
6	RFGC, TEBC, FMO, DMO
7	FOO, TRO
8	/RST

AC Characteristics

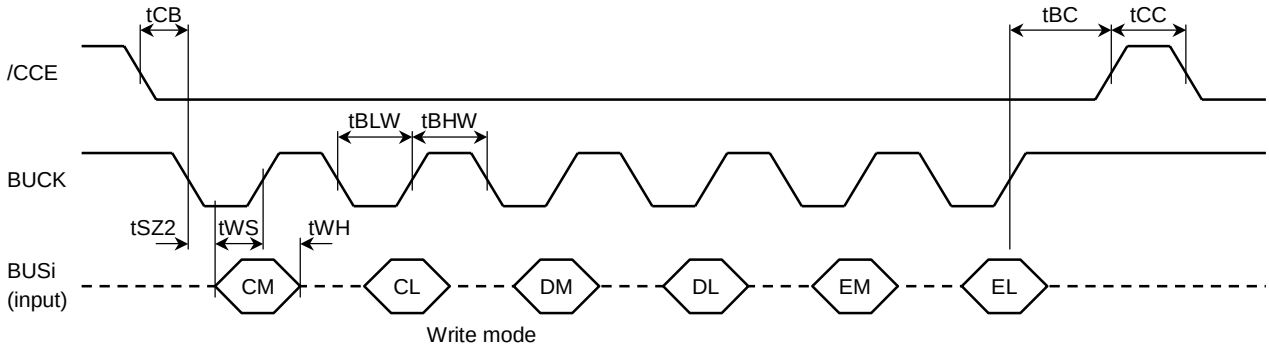
1. Microcontroller Interface Timing

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
/CCE = "H" pulse width	tCC	—	—	120	—	—	ns
Data disable time	tSZ1	—	BUCK rise reference	0	—	—	
/CCE, BUCK delay time	tCB	—	/CCE fall reference	0	—	—	
BUCK, /CCE delay time	tBC	—	BUCK rise reference	0	—	—	
BUCK = "L" pulse width	tBLW	—	Write, SRC mode	120	—	—	
	tBLW	—	QDRC mode	240	—	—	
BUCHK = "H" pulse width (1)	tBHW	—	Write, SRC mode	120	—	—	
BUCHK = "H" pulse width (2)	tBHW	—	QDRC mode (normal speed)	3000	—	—	
BUCHK = "H" pulse width (3)	tBHW	—	QDRC mode (double speed)	1500	—	—	
BUCHK = "H" pulse width (4)	tBHW	—	QDRC mode (×4 speed)	800	—	—	
Write data setup time	tWS	—	BUCK rise reference	60	—	—	
Write data hold time	tWH	—	BUCK rise reference	20	—	—	
Data disable time	tSZ2	—	BUCK fall reference	0	—	—	
Read data access time	tRD	—	BUCK fall reference	0	—	—	

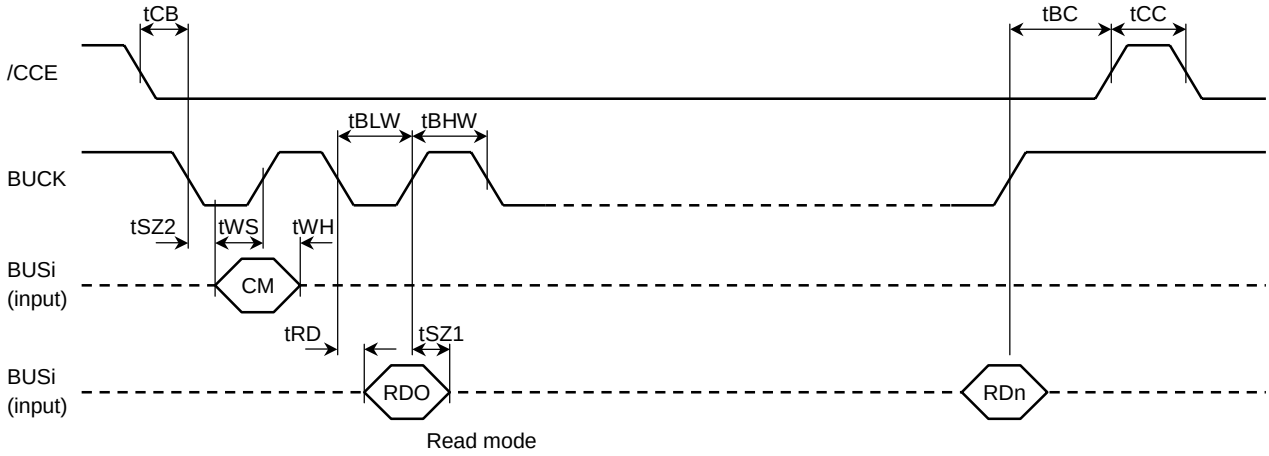
(1) Write command mode



(2) Write command mode: Bxxxxx, Fxxxxx commands

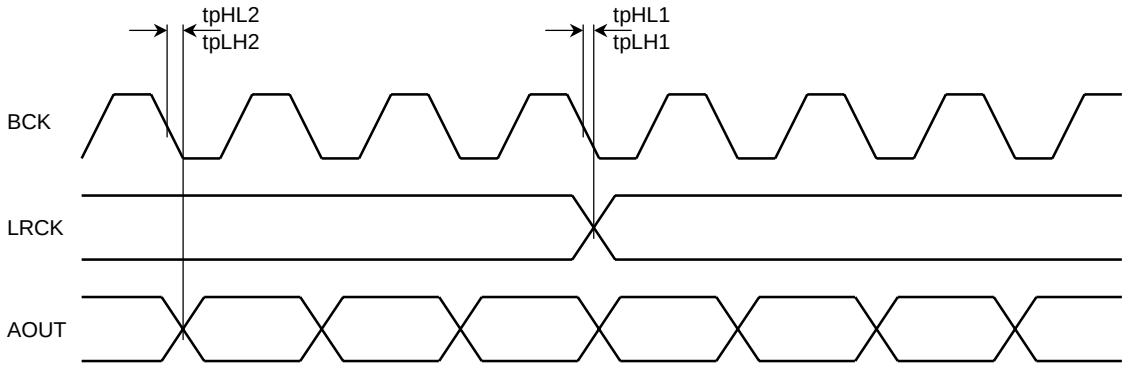


(3) Read command mode



2. AOUT Data Output Timing

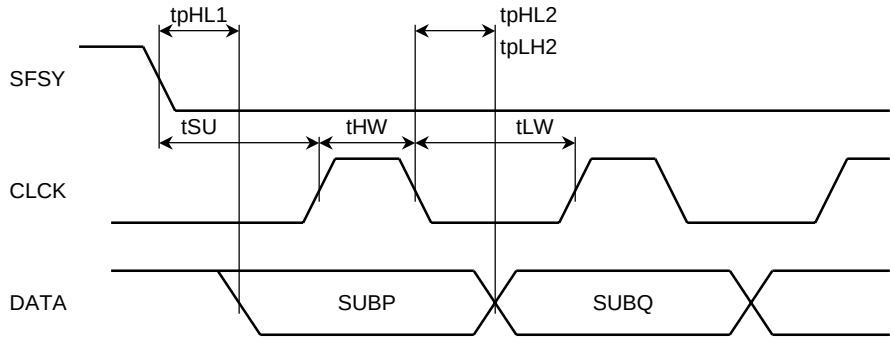
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Transfer time (1)	"H" level	tpLH1	—	LRCK	—	—	5	ns
	"L" level	tpHL1	—		—	—	5	
Transfer time (2)	"H" level	tpLH2	—	AOUT	—	—	5	
	"L" level	tpHL2	—		—	—	5	



3. DATA, CLCK Input/Output Timing

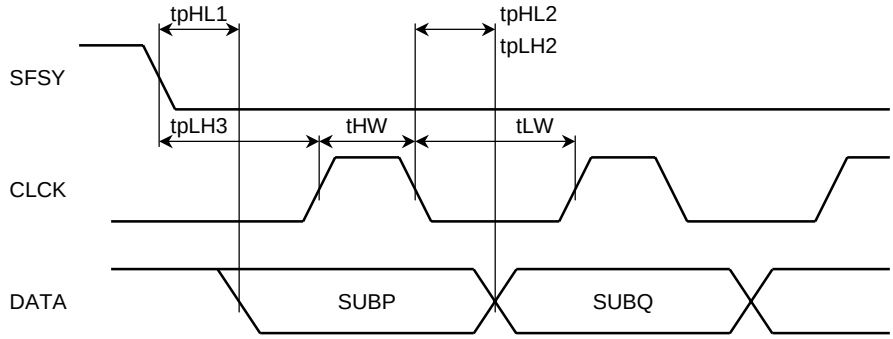
(1) CLCK input mode (regardless of setting of HS and UHS bits of SPEED command)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Clock pulse width	"H" level	tHW	—	CLCK input mode	50	—	—	ns
	"L" level	tLW	—		50	—	—	
Input setup time		tSU	—		400	—	—	
Transfer time (1)	"L" level	tpHL1	—		—	—	5	
Transfer time (2)	"H" level	tpLH2	—		—	—	15	
	"L" level	tpHL2	—		—	—	15	



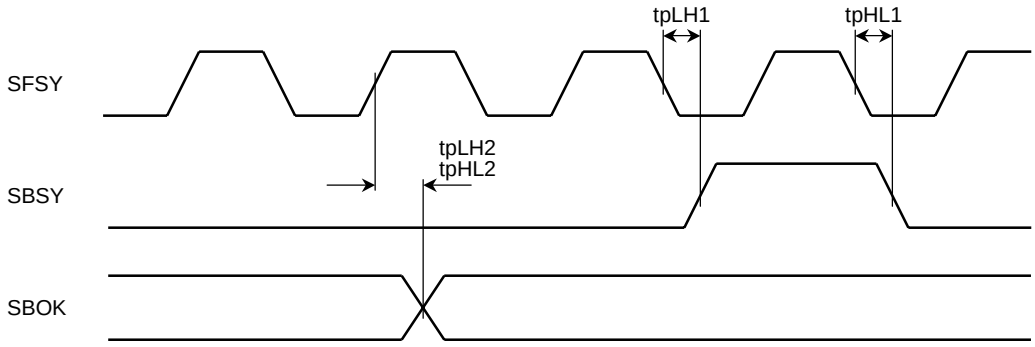
(2) CLCK output mode (tHW, tLW, tpLH3 only, × 1/n at ×n speed)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Clock pulse width	"H" level	tHW	—	CLCK output mode	—	—	950	ns
	"L" level	tLW	—		—	—	950	
Transfer time (1)	"L" level	tpHL1	—		—	—	5	
Transfer time (2)	"H" level	tpLH2	—		—	—	15	
	"L" level	tpHL2	—		—	—	15	
Transfer time (3)	"H" level	tpLH3	—		—	—	850	



4. SBSY, SBOK Input/Output Timing

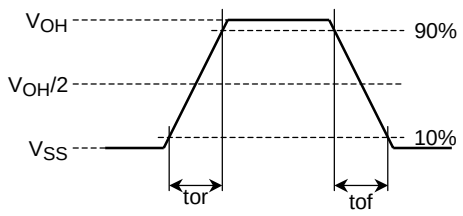
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Transfer time (1)	"H" level	tpLH1	—	SBSY	—	—	5	ns
	"L" level	tpHL1	—		—	—	10	
Transfer time (2)	"H" level	tpLH2	—	SBOK	—	—	15	
	"L" level	tpHL2	—		—	—	20	



5. Output Pin Timing

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output rise time (1)	tor1	—	Pins grouped as 1 below	—	—	7	ns
Output fall time (1)	tof1	—		—	—	12	
Output rise time (2)	tor2	—	Pins grouped as 2 below	—	—	7	
Output fall time (2)	tof2	—		—	—	7	
Output rise time (3)	tor3	—	Pins grouped as 3 below	—	—	7	
Output fall time (3)	tof3	—		—	—	7	
Output rise time (4)	tor4	—	Pins grouped as 4 below	—	—	10	
Output fall time (4)	tof4	—		—	—	10	

Pin Group	Pin Name
1	SBOK, SFSY, SBSY, /HSO, /UHSO, ZDET
2	BCK, LRCK, AOUT, DOUT, IPF, CLCK, DATA
3	BUS3, BUS2, BUS1, BUS0
4	TMAX, SEL



Analog Circuit Characteristics

1. AD Converter

Characteristics		Test Circuit	Test Condition	Min	Typ.	Max	Unit
Resolution		—	—	—	8	—	bit
Sampling frequency	FE	—	—	—	88.2	—	kHz
	TE	—		—	88.2	—	
	SBAD	—		—	88.2	—	
	RFRP	—		—	88.2	—	
Conversion input range		—	AV_{SS} = 0 V, AV_{DD3} = 3.3 V	0.2 × AV_{DD3}	—	0.8 × AV_{DD3}	V

2. DA Converter (focus and tracking equalizer output)

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Number of bits	—	—	—	—	5	bit
Sampling frequency	—	—	—	—	2.8	MHz
Signal output range	—	AV_{SS} = 0 V, AV_{DD3} = 3.3 V	AV_{SS3}	—	AV_{DD3}	V

3. PLL Filter Amp

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
I/O signal range	—	—	AV_{SS3}	—	PV_{DD3}	V
Frequency characteristic	—	−3 dB point (Gain = 1)	—	8	—	MHz

4. VCO (PLL)

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Center oscillation frequency	—	LPFO = V_{REF}	—	34	—	MHz
Frequency variable range	—	[VCOGSL] bit = “L”	−55	—	+55	%
	—	[VCOGSL] bit = “H”	−65	—	+65	

5. TEZI Signal Comparator

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input range	—	—	AV_{SS3}	—	AV_{DD3}	V
Hysteresis voltage	—	V_{REF} reference	−50	—	+50	mV

6. RFZI Signal Comparator

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input range	—	—	AV_{SS3}	—	AV_{DD3}	V
Hysteresis voltage	—	V_{REF} reference	−50	—	+50	mV

7. Data Slicer Circuit

(1) Comparator

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input amplitude	—	V_{REF} refenence	0.6	1.2	2.0	V_{pp}

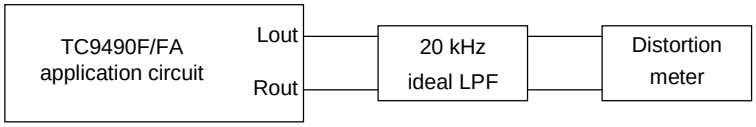
(2) R-2R DAC (digital slicer DAC)

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output conversion range	—	—	AV_{SS3}	—	AV_{DD3}	V
Output impedance	—	—	—	2.5	—	kΩ

8. Audio DAC Characteristics

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Total harmonic distortion + noise	THD + N	1	1 kHz sine wave, full-scale input	—	−85	−80	dB
S/N ratio	S/N	1	—	87	92	—	dB
Dynamic range	DR	1	1 kHz sine wave, −60 dB input conversion	85	90	—	dB
Crosstalk	CT	1	1 kHz sine wave, full-scale input	—	−90	−85	dB
Analog output amplitude	DACout	1	1 kHz sine wave, full-scale input	810	860	910	mV_{rms}

Test Circuit 1: Application circuit is used.

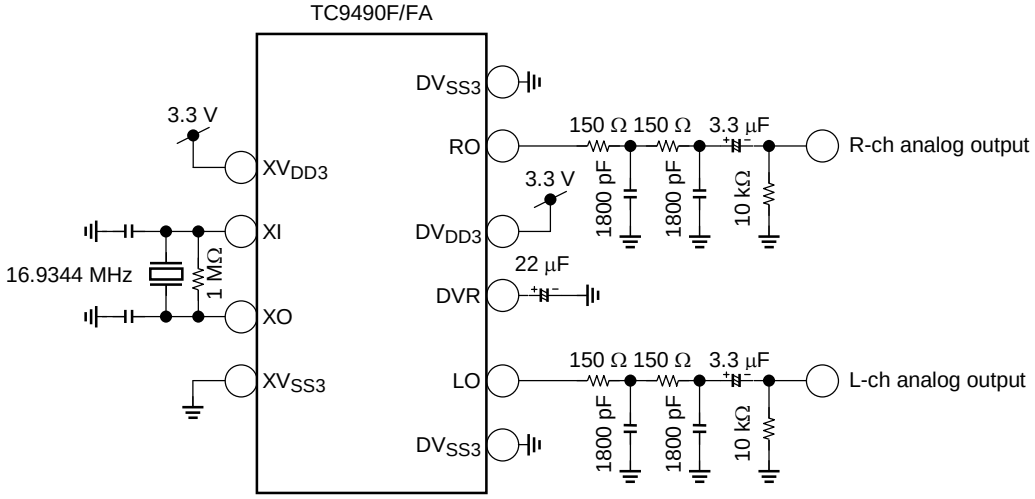


LPF: Filter with built-in Shibasoku 725C
Distortion meter: Shibasoku 725 equivalent

Characteristic	Distortion Filter Setting A-weight
THD + N, CT	OFF
S/N, DR	ON

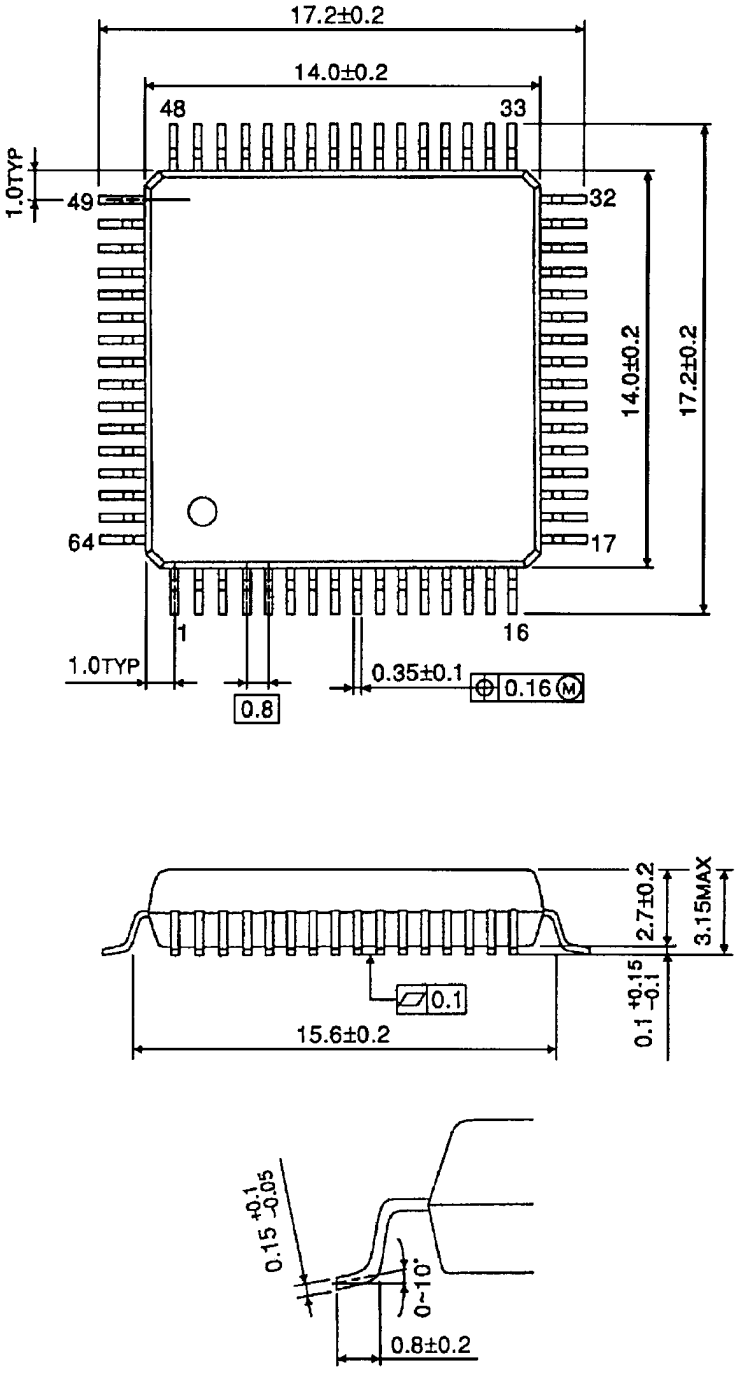
A-weight: IEC-A equivalent

Application Circuit



Package Dimensions

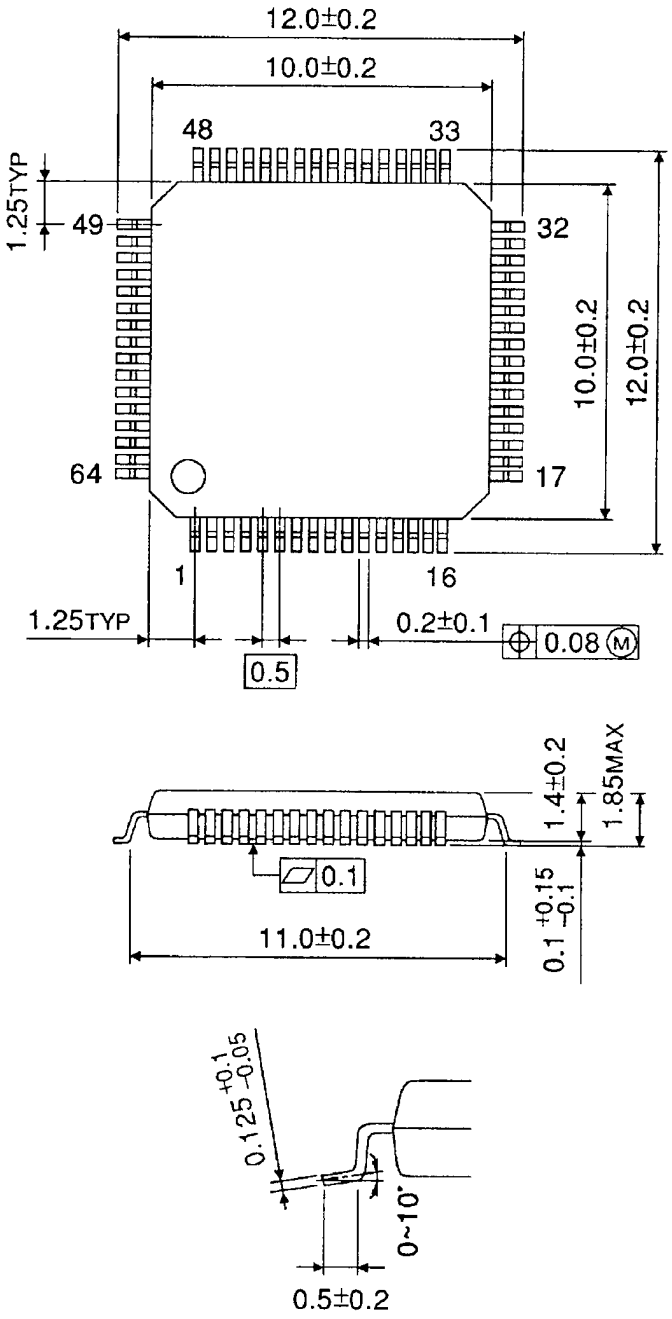
QFP64-P-1414-0.80A Unit : mm



Weight: 0.5 g (typ.)

Package Dimensions

LQFP64-P-1010-0.50 Unit : mm



Weight: 0.4 g (typ.)

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