PNX8510/11
Analog Companion Chip

Rev. 02 — 8 October 2001 Product data

1. Introduction

The PNX8510/11 is intended to serve as an analog back end “companion” for digital ICs dealing with video and audio signal processing.

The primary difference between the PNX8510 and the PNX8511 is as follows:

- PNX8510 includes the Macrovision™ pay-per-view copy protection system.
- PNX8511 does not include the Macrovision™ pay-per-view copy protection system.

The PNX8510/11 provides two video encoders through two standardized D1 interfaces. The encoders can be bypassed to get direct access to the video DACs for higher resolution displays, such as some of the ATSC formats. The PNX8510/11 also contains a sophisticated sync raster engine which can be utilized to generate various synchronization patterns for interlaced and non-interlaced image formats. The sync raster engine together with an up-sampling filter and a sync insertion unit compose a complete HDTV-capable data path including tri-level sync generation.

The PNX8510/11 also provides two independent pairs of stereo audio DACs with two corresponding I^2S interfaces.

Figure 1 shows the PNX8510/11 with a typical source decoder IC.

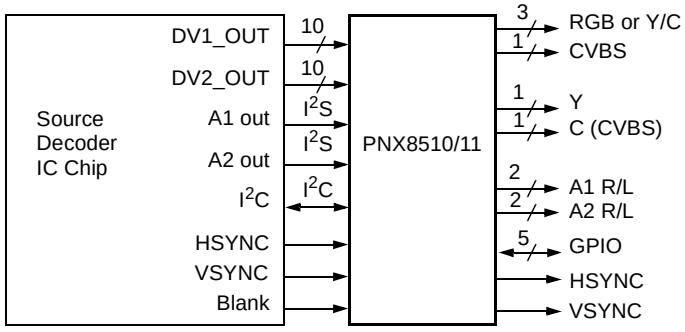


Figure 1: System Level Diagram

1.1 Features

The features of the PNX8510/11 are as follows:

PNX8510

- Six 10-bit video DACs running at up to 135 MHz 1LSB DNL
- Four audio DACs arranged as two stereo pairs

- Two built-in digital video encoders
- PAL B/G, NTSC-M, SECAM encoding
- Two 10-bit D1 inputs with embedded VBI data
- Two I^2S independent audio input ports
- I^2C programmable (slave interface)
- Support for high resolution video out up to 81 MHz interface clock rate
- Support for various input modes (2xD1, RGB, 1x 2D1 muxed, 24/30-bit RGB, DD1...)
- Programmable generation of embedded analog and external digital sync signals compliant to VESA and SMPTE 274 standards
- VBI encoding for standard definition video out
- Teletext insertion for PAL-WST, NTSC-WST, NABTS
- VPS video programming service encoding
- Closed caption encoding
- CGMS copy generation management system according to CPR-1204
- Internal color bar generator for standard definition video out
- JTAG-controlled test signals on video and audio converters
- Macrovision™ pay-per-view copy protection system, rev. 7.1 (SCART support with Macrovision copy protection on the RGB lines)

PNX8511

Features are identical to the PNX8510 except that Macrovision™ is not available.

2. Video Pipeline

2.1 Overview

The video pipeline contains two independent video channels. The primary channel is used to display graphic or video content on a standard television, CRT monitor or an HDTV system. The secondary video channel may connect to a VCR or a second standard TV for recording or secondary display purposes. No high definition or RGB output is available through the second video channel.

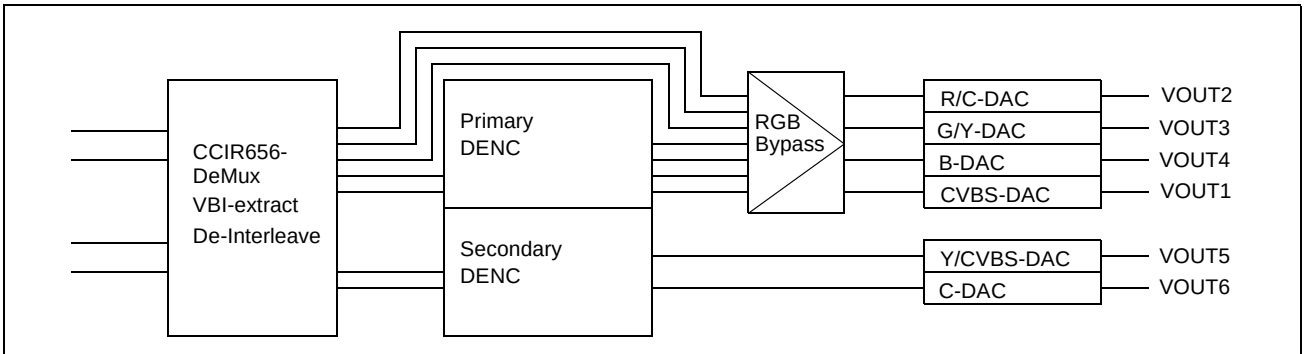


Figure 2: Video Path Block Diagram

The two video pipelines are driven by two standard D1 interfaces, which can operate in various modes in 8 or 10-bit precision. The following tables summarize the different modes of operation for the video interface of the PNX8510/11.

The video interfaces and the sync raster engines are designed in a generic way. The only limiting factor is the data rate of the received video streams. All formats with a total interface speed requirement below 81 MHz can be displayed by the PNX8510/11.

Table 1: Primary Video Channel Standard Interface Modes

Interface Modes	Mode	Interface Speed
4:4:4 RGB or YUV or YCrCb or YPrPb	4:4:4 Muxed Components 10/8-bit	up to 81 MHz
4:2:2 YUV or YCrCb or YPrPb	4:2:2 Muxed components 10/8-bit	up to 81 MHz

Table 2: Primary Video Channel Standard Display Modes

Display Modes	Mode	Interface Speed	Used Data Path
PAL/NTSC/SECAM 4:2:2 YUV i.e. PAL: 864 pixel/line x 312.5 lines/field x 50Hz = 13.5 MHz/Y samples 7.5 MHz/U samples 7.5 MHz/V samples	4:2:2 Muxed components 10/8-bit	27 MHz	SD-CVBS-data path
PAL/NTSC/SECAM RGB/YUV i.e. PAL: 864 pixel/line x 312.5 lines/field x 50Hz = 13.5 MHz/Y samples 7.5 MHz/U samples 7.5 MHz/V samples	4:2:2 Muxed components 10/8-bit	27 MHz	SD-CVB and RGB/ YUV data paths
2FH PAL/NTSC/SECAM 4:4:4 RGB/YUV/YCrCb/YPrPb i.e. PAL: 864 pixel/line x 312.5 lines/field x 50 Hz x2 = 27 MHz/component	4:4:4 Muxed Components 10/8-bit	81 MHz	HD-data path
480P PAL/NTSC/SECAM 4:4:4 RGB/YUV/YCrCb/YPrPb i.e. PAL: 864 pixel/line x 625 lines/field x 50 Hz = 27 MHz/component	4:4:4 Muxed Components 10/8-bit	81 MHz	HD-data path
generic D1 mode; the interface clock can run up to 81MHz, the components can have either 4:2:2 or 4:4:4 color resolution, but must be in the correct color space.	4:4:4 Muxed components/ 4:2:2 Muxed components (use of both D1 interfaces required) 10/8-bit	up to 81 MHz	HD-data path

Table 3: Secondary Video Channel Standard Interface Modes

Interface Modes	Mode	Interface Speed
4:2:2 YUV or YCrCb or YPrPb	4:2:2 Muxed components 10/8-bit	27 MHz

Table 4: Secondary Video Channel Standard Display Modes

Display Modes	Mode	Interface Speed	Used Data Path
PAL/NTSC/SECAM 4:2:2 YUV i.e. PAL: 864 pixel/line x 312.5 lines/field x 50Hz = 13.5MHz/Y samples 7.5 MHz/U samples 7.5 MHz/V samples	4:2:2 Muxed components 10/8-bit	27 MHz	SD-CVBS-data path

Table 5: Special Interface/Display Modes

Display/Interface Modes	Mode	Interface Speed
24-bit RGB/YUV Both D1 interfaces and the secondary audio channel are combined to provide high-speed direct access to video DACs . Pin Assignment 24-Bit Mode red[7] - I^2S_IN2_SD red[6] - I^2S_IN2_WS red[5] - I^2S_IN2_SCK red[4] - I^2S_AOS2_CLK red[3] - DV_IN1[9] red[2] - DV_IN1[8] red[1] - DV_IN1[7] red[0] - DV_IN1[6] green[7] - DV_IN1[5] green[6] - DV_IN1[4] green[5] - DV_IN1[3] green[4] - DV_IN1[2] green[3] - DV_IN1[1] green[2] - DV_IN1[0] green[1] - DV_IN2[9] green[0] - DV_IN2[8] blue[7] - DV_IN2[7] blue[6] - DV_IN2[6] blue[5] - DV_IN2[5] blue[4] - DV_IN2[4] blue[3] - DV_IN2[3] blue[2] - DV_IN2[2] blue[1] - DV_IN2[1] blue[0] - DV_IN2[0 Pin Assignment 30-Bit Mode red[9] - I^2S_IN2_SD red[8] - I^2S_IN2_WS red[7] - I^2S_IN2_SCK red[6] - I^2S_AOS2_CLK red[5] - DV_IN1[9] red[4] - DV_IN1[8] red[3] - DV_IN1[7] red[2] - DV_IN1[6] red[1] - GPIO[5] red[0] - GPIO[4] green[9] - DV_IN1[5] green[8] - DV_IN1[4] green[7] - DV_IN1[3] green[6] - DV_IN1[2] green[5] - DV_IN1[1] green[4] - DV_IN1[0] green[3] - DV_IN2[9] green[2] - DV_IN2[8] green[1] - GPIO[3] green[0] - GPIO[2] blue[9] - DV_IN2[7] blue[8] - DV_IN2[6] blue[7] - DV_IN2[5] blue[6] - DV_IN2[4] blue[5] - DV_IN2[3] blue[4] - DV_IN2[2] blue[3] - DV_IN2[1] blue[2] - DV_IN2[0] blue[1] - GPIO[1] blue[0] - DV_CLK2 Note: In case of the 24/30-bit full parallel input, no secondary audio channel is available.	24-bit direct RGB/YUV 8/10-bit	up to 81 MHz
Single interface mode 2 (D1) Accommodates 2 synchronous multiplexed D1 streams for low cost applications (both streams are extracted)	2x muxed 4:2:2 single D1 8/10-bit	54 MHz
Interleaved interface mode Same formats as in single interface mode 1 and 2 but only one of the two interleaved video streams is extracted per interface. Selection of the extracted slice is possible by software, Usage of two PNX8510/11 chips possible to support up to 4 display/record devices	2x muxed 4:2:2 single D1 or 2x muxed 4:4:4 RGB/YUV 8/10-bit	54 MHz or 81 MHz or pos-neg edge 27 MHz (SAA7128 compliant)
Combined double D1 mode: the two D1 interfaces are combined to carry a single HDTV stream in 4:2:2 YUV or 4:2:2 YPrPb format primary D1: Y channel secondary D1: muxed UV or PrPb channel i.e.: 1920x1080 60 Hz interlaced 2200 pixel/line x 562.5 lines/field x 60 Hz = 74.25 MHz/Y samples 37.125 MHz/Cr/Pr samples 37.125 MHz/Cb/Pb samples Note: In case of the combined double D1 mode, no secondary display channel is available.	2 combined D1 8/10-bit	up to 75 MHz per D1

The PNX8510/11 supports color space conversion only in the primary RGB standard definition data path. For the high definition part of the primary video data path and for the secondary video data path no color space conversion is available. Hence the video data has to be provided in the display destination color space.

Aside from built-in video encoders, which generate all necessary timing and filtering for an appropriate sync raster for PAL, NTSC and SECAM, the PNX8510/11 contains a separate raster-generation engine which also supports but is not limited to the HD-formats, such as the SMPTE 274M. Furthermore the PNX8510/11 contains an up-sampling filter to convert 4:2:2 formats (other than standard definition formats) to 4:4:4.

Note: In the case of combined double D1 mode, no secondary display channel is available.

If the interface is operated in D1 mode, the data stream presented to the interface has to be D1 compliant i.e., the maximum and minimum codes (8-bit 0x00 0xFF, 10-bit 0x000 0x3FF) must not occur during active video.

A detailed description of video input data formats can be found in Section 2.2 Video Input Modes. The video modes mentioned in Section 2.2 correspond to the settings of the DEMUX_MODE bits in the register 0x95 VMUXCTL. If the video interface clock frequency is not equivalent to the processing and the video DAC operation frequency the appropriate divider registers in the audio/clock register section have to be programmed. As a general rule the following settings should be used:

422 YUV SD Single Interface Mode

27MHz interface clock

27MHz processing clock

27MHz DAC clock

444RGB 2FH Single Interface Mode

81MHz interface clock

27MHz processing clock

27MHz DAC clock

422 YUV 1080i Double Interface Mode

74.25MHz interface clock

74.25MHz processing clock

74.25MHz DAC clock

2.2 Video Input Modes

The PNX8510/11 video interface supports a wide variety of video formats. The video interface is designed in a generic fashion. It is de-coupled from the actual video data paths in the system and imposes only a few restrictions on the video data streams provided to the chip.

This section explains the possible video stream formats and provides details on synchronizing the PNX8510/11 with respect to a particular video data format.

The PNX8510/11 accepts the following video formats on a single interface with up to 81 MHz interface clock:

2.2.1 YUV 4:2:2

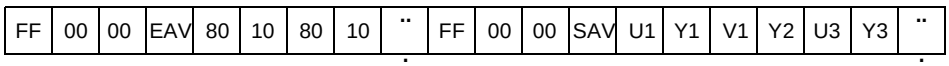


Figure 3: YUV 4:2:2

This is the CCIR-656 compliant format and will mainly be used at an interface speed of 27 MHz to feed the video encoder modules in the chip.

This is the standard interface format for the secondary video encoder pipeline unless the chip is used in High Definition (HD) mode.

The YUV 4:2:2 format can also be used to feed the HD data path as long as the pixel clock rate stays below 81 MHz. To operate the HD data path with 4:2:2 source material the 4:2:2 to 4:4:4 filter should be enabled to achieve the best video quality.

2.2.2 RGB 4:4:4

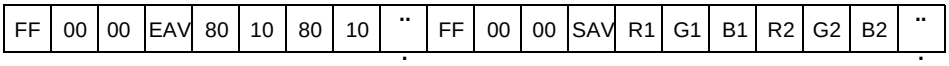


Figure 4: RGB 4:4:4

This mode is only useful if the HD data path in the PNX8510/11 is in operation. The RGB 4:4:4 interface mode is not applicable to the standard definition RGB path operation due to the implicit clocking requirements. The data rate for standard definition RGB 4:4:4 data would be 13.5 MHz per component resulting in an interface speed of 40.5 MHz. Because the chip does not contain any PLLs, it is not possible to extract 27 MHz out of the interface clock.

2.2.3 YUV 4:4:4

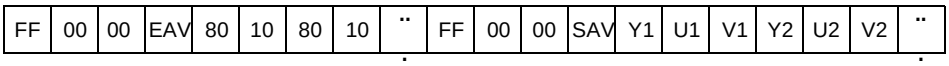


Figure 5: YUV 4:4:4

This mode is useful only if the HD data path in the PNX8510/11 is in operation.

2.2.4 YUV 4:2:2 Interleaved

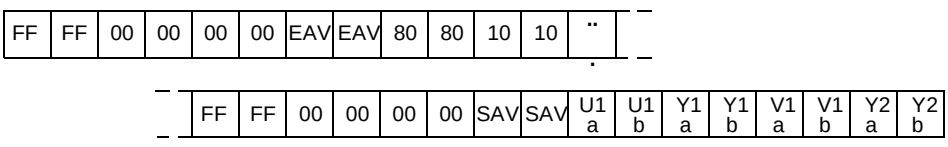


Figure 6: YUV 4:2:2 Interleaved

This mode supports two video data streams through one physical video interface. It can be used to utilize both video encoder channels in the chip with one interface only or to hook up two PNX8510/11 devices to one source providing an interleaved data stream. Each chip extracts one slice from the interleaved stream. This video format is useful for the encoder standard definition data path only.

2.2.5 RGB 4:4:4 Interleaved

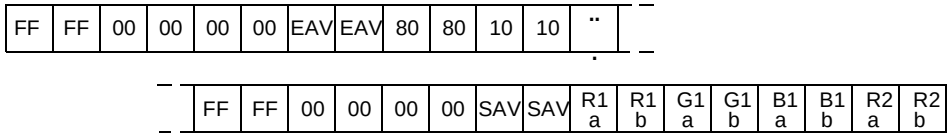


Figure 7: RGB 4:4:4 Interleaved

This mode supports two video data streams through one physical video interface. It can be used to utilize both video encoder channels in the chip with one interface only or to hook up two PNX8510/11 devices to one source providing an interleaved data stream. Each chip extracts one slice from the interleaved stream. This video format is useful for the standard definition RGB data path as well as for the HD data path.

2.2.6 YUV 4:4:4 Interleaved

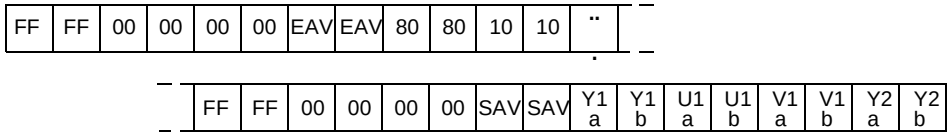


Figure 8: YUV 4:4:4 Interleaved

This mode supports two video data streams through one physical video interface. It can be used to utilize both video encoder channels with one interface only or to hook up two PNX8510/11 devices to one source providing an interleaved data stream. Each chip extracts one slice from the interleaved stream. This video format is useful for the HD data path only.

There are two modes defined for interleaved data streams. One is to run the interface at twice the speed and provide a qualifier on the HSYNC input to qualify a certain slice. The qualifier is essentially the interface clock divided by two.

The other interleaved interface format works on both clock edges of the interface clock, so one slice is latched at the positive edge and the other slice is latched at the negative edge of the interface clock.

2.2.7 YUV 4:2:2 HD Two Channel Format

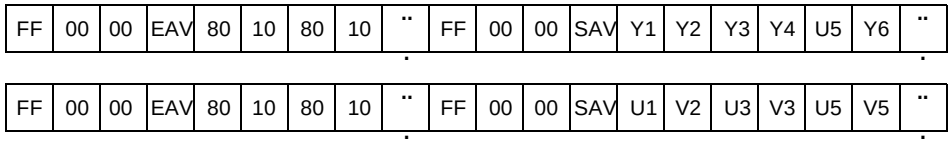


Figure 9: YUV 4:2:2 HD Two Channel Format

This format is used only for high definition video modes that exceed interface clock requirements of 81 MHz. For this video interface mode, both physical interfaces of the chip are utilized. The primary interface gets a D1-like data stream, which only contains the luminance information, while the secondary D1 interface carries the chrominance information.

2.3 Video Input Module

The video input module is responsible for accommodating all supported video data formats. It delivers a de-multiplexed and de-sliced data stream to the video processing modules.

As depicted in Figure 10, the IC has two video input ports which can accommodate 8 or 10-bit wide video data streams.

The normal mode of operation is that the DV1 interface is routed to the primary video data paths and the DV2 interface is routed to the secondary video data paths. The IC however accepts also so called sliced data formats. A sliced data format contains two single video data streams multiplexed together on a component basis. A more detailed description of the arrangement of the components can be found in Section 2.2 Video Input Modes. To enable sliced data formats the SLICE_MODE bit has to be set.

The De-Slice module essentially takes the two data streams apart by simply two to one de-multiplexing. The routing of the resulting two video data streams is determined by setting the SEL register bits in the primary and secondary video data path apertures appropriately. Sliced data formats come in two different flavors: double edge and qualified.

The double edge slice format has data changes on the positive and the negative clock edge where as the qualified mode qualifies one data stream of the two multiplexed ones with an active high on the HSYNC signal. To use this mode the USE_QUALIFIER bit must be set. The order of the slice qualification can be changed by setting the INV_QUALIFIER bit.

Since each of the video input interfaces can accept sliced data formats a total of four video data streams could be routed into the IC and two of them can be selected to be forwarded to the primary and the secondary video display pipeline.

Note: If the two video pipelines are sourced by only one video input interface operating in sliced mode, both video pipelines must receive the same input clock originating from the sliced data source.

The structure of the video input module is shown in the block diagram below.

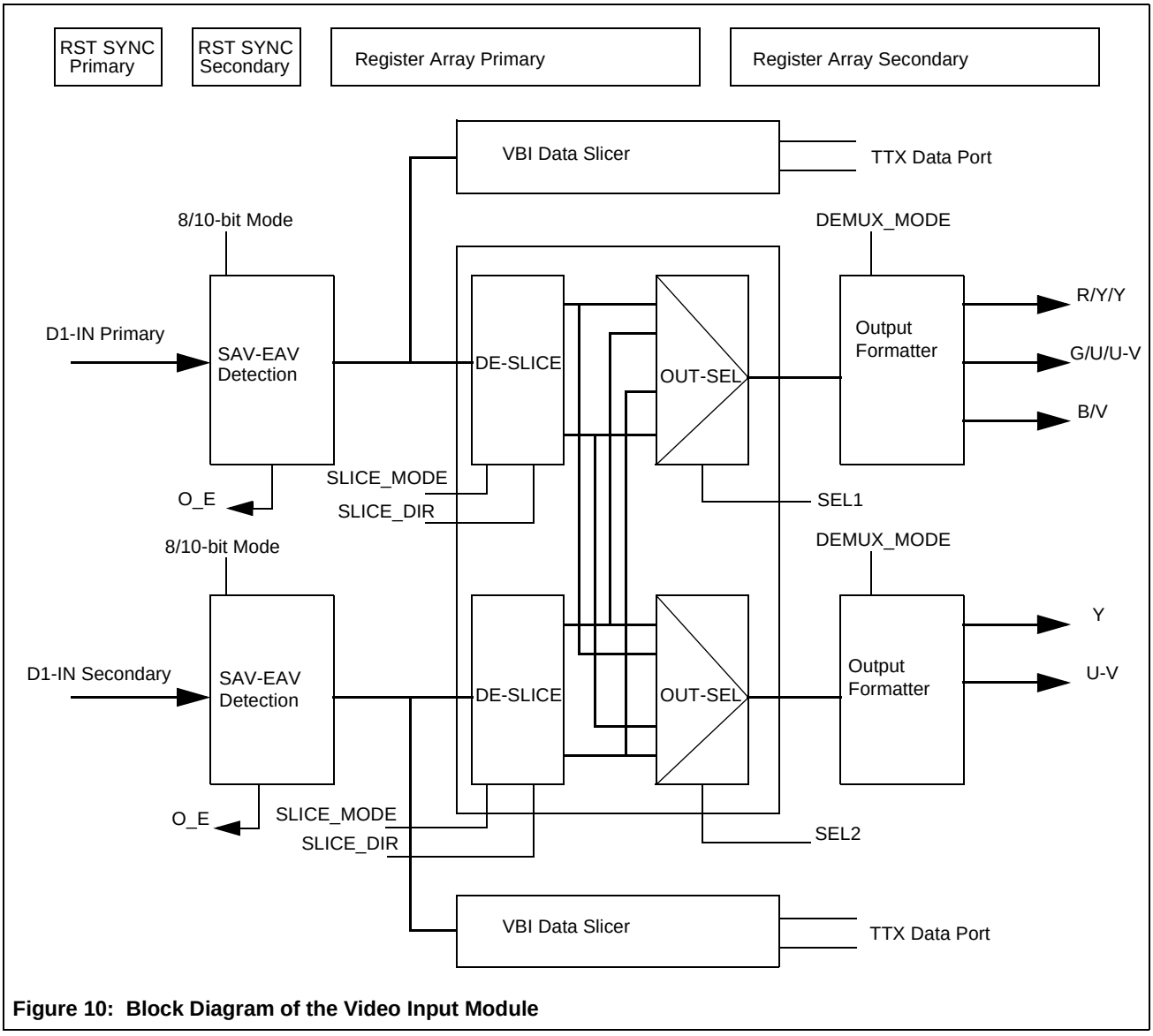


Figure 10: Block Diagram of the Video Input Module

2.4 Video DAC Control

The PNX8510/11 contains 6 video DACs. Four of them are dedicated to the primary video pipeline and the remaining 2 are assigned to the secondary video processing path.

The first DAC of the primary video channel (VOUT1) is always assigned to the primary standard definition data path. The output of the DAC can be changed from CVBS to Y by resetting the DAC control bit CVBSEN to zero.

The second DAC of the primary video channel (VOUT2) is either assigned to the standard definition data path and carries the chrominance (Y/C operation) if the CEN bit in the DAC control register is set or the Red/V channel (RGB/Component mode operation) if the DAC control register bit CEN is reset. In HD mode (SD_HD bit set to zero) this DAC carries either the Red channel or the Y channel depending on whether the HD path is operated in YUV or RGB mode. Note that the CEN bit must be reset for HD operation.

The third DAC of the primary video channel (VOUT3) carries the luminance channel if the VBSEN bit is set in standard definition mode (SD_HD=1'b1). This DAC streams out the Green/Y channel if the VBSEN bit is reset (RGB/Component mode operation). If the high definition data path is operational (SD_HD=1'b0) this DAC carries the Green or U channel depending on whether the HD path is operated in YUV or RGB mode.

The configuration of the fourth DAC in the primary video data path (VOUT4) can not be changed with a programming register. This DAC carries the Blue or U channel in standard definition mode and the Blue or V channel if the high definition data path is active.

The configuration of the DACs for the secondary video data path is limited to the CVBS/Y DAC (VOUT5). If the CVBSEN bit in the DAC control register is set this DAC carries the CVBS signal. Resetting the bit results in the Y signal being assigned to this DAC.

The second DAC of the secondary video pipeline (VDAC6) always carries the chrominance signal.

2.5 VBI Data

VBI data extraction from a D1 data stream is only supported for standard definition formats. The extraction follows the concept of Philips video decoders, such as the SAA7114. Both video interfaces can carry VBI data information. The content of the VBI data is entirely determined by the source decoder chip software driver.

The PNX8510/11 supports two VBI data streams. The limitation to two VBI data streams implies certain limitations when using multiple PNX8510/11 chips in a system. In this case one PNX8510/11 gets either one or two (all) VBI data streams. The other PNX8510/11 IC would get one or none.

Only the ANC/SAV-EAV header style VBI data encoding mode is supported in the PNX8510/11. According to these standards VBI data is always inserted in the horizontal blanking interval of a line. The data is preceded by an ANC header which is programmable. An internal header following the ANC contains a programmable sliced data identifier with the number of data bytes transmitted and two internal identification tokens containing data type, field type and line number. Figure 11 illustrates how the data is encoded in the horizontal blanking interval.

Note: In standard definition mode, only 8 of the 10 available signal lines of the D1 interface are used. The two LSB lines are fixed to zero.

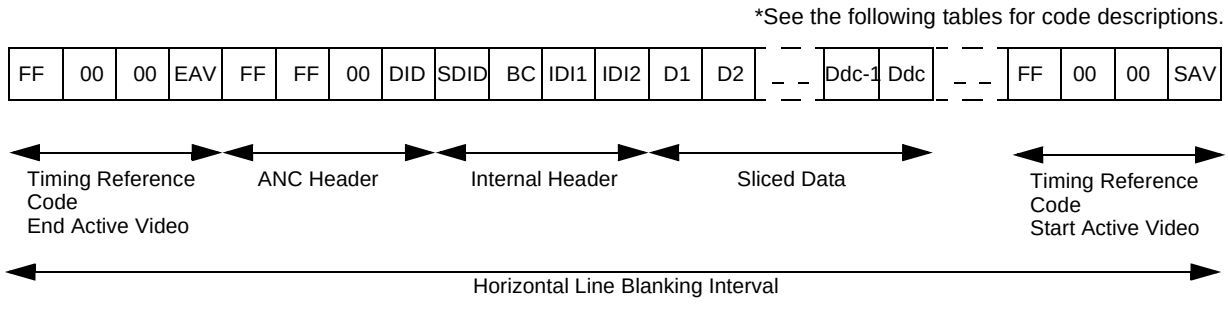


Figure 11: ANC VBI Data Insertion in D1

Table 6: VBI Header/Data Codes

Name	Function
SAV	start of active video
DID	data identifier: ignored, has to be set to 0x11h
SDID	sliced data identification: ignored, has to be set to 0x11h
BC	byte count describes the number of succeeding decoded data bytes
IDI1	internal data identification 1: OP, FID, LineNumber[8:3]
IDI2	internal data identification 2: OP, LineNumber[2:0], DataType
D1-Ddc	data bytes
EAV	end of active video

Table 7: VBI Data Header Format

Code	D9	D8	D7	D6	D5	D4	D3	D2
SDID	1	1	1	1	1	1	1	1
DID	1	1	1	1	1	1	1	1
BC	-	-	BC5	BC4	BC3	BC2	BC1	BC0
IDI1	-	field ID 0=field 1 1=field 2	LN8	LN7	LN6	LN5	LN4	LN3
IDI2	-	LN2	LN1	LN0	DT3	DT2	DT1	DT0
LN = line number; BC = byte count; DT = data type								

Table 8: SAV/EAV Codes NTSC

Line Number	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-19	0	1	1	0
20-263	0	0	1	0
264-265	0	1	1	0
266-282	1	1	1	0
283-525	1	0	1	0

Table 9: SAV/EAV Codes PAL

Line Number	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
336-623	1	0	1	0
624-625	1	1	1	0

Table 10: SAV/EAV-Sequence

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
preamble	1	1	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0
status word	1	F	V	H	P3	P2	P1	P0	0	0

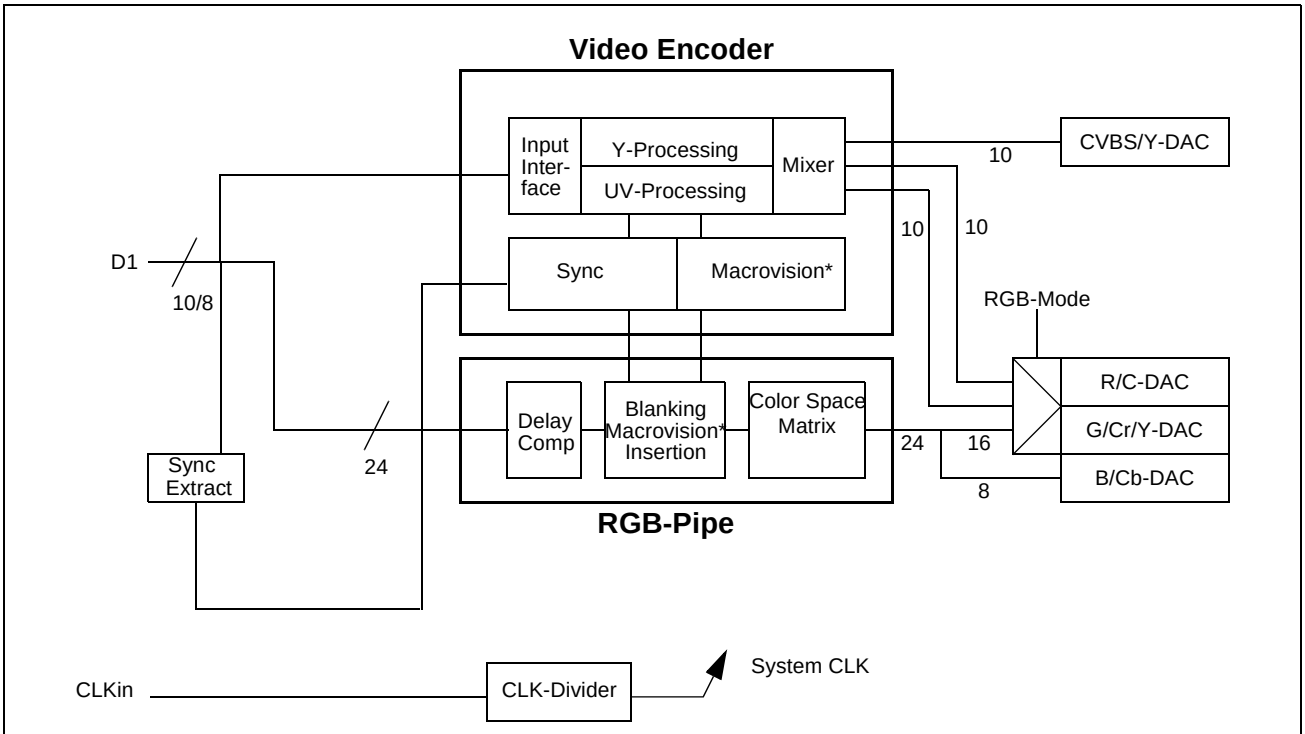
P0 to P3 are protection bits and calculated in the following way:

```
P3=V^H; P2=F^H; P1=F^V; P0=F^V^H
```

Table 11: Supported Data Types

Data Type	Standard
0000	Teletext EuroWST
0010	VPS video programming service
0011	WSS wide screen signalling
0100	closed caption
1100	US NABTS
1111	Programming (SubAddr1-Data1-SubAddr2-Data2 ...)

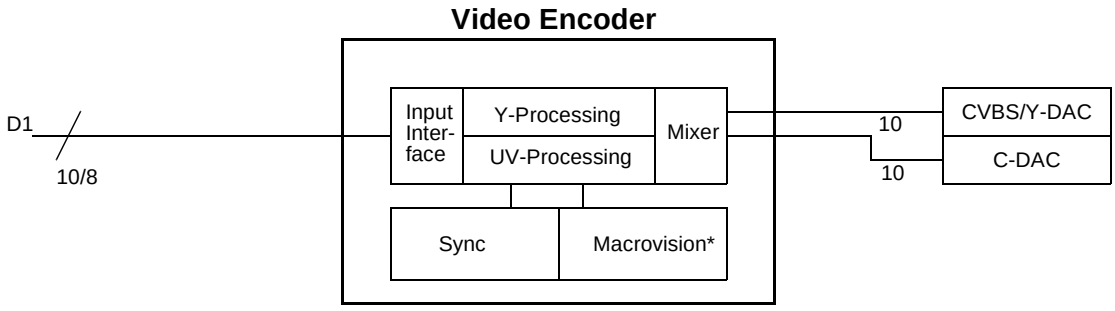
Figure 12 illustrates the different modes of operation for the primary video channel.



* Macrovision is not available in the PNX8511.

Figure 12: Primary Display Pipe (Standard Definition Operation Mode)

The secondary display consists of the Y and UV processing data path of a video encoder only. The synchronization information will be extracted from the incoming D1 data stream. The structure of the secondary display pipe is shown in the figure below.



* Macrovision is not available in the PNX8511.

Figure 13: Secondary Display Pipe (Standard Definition Operation Mode)

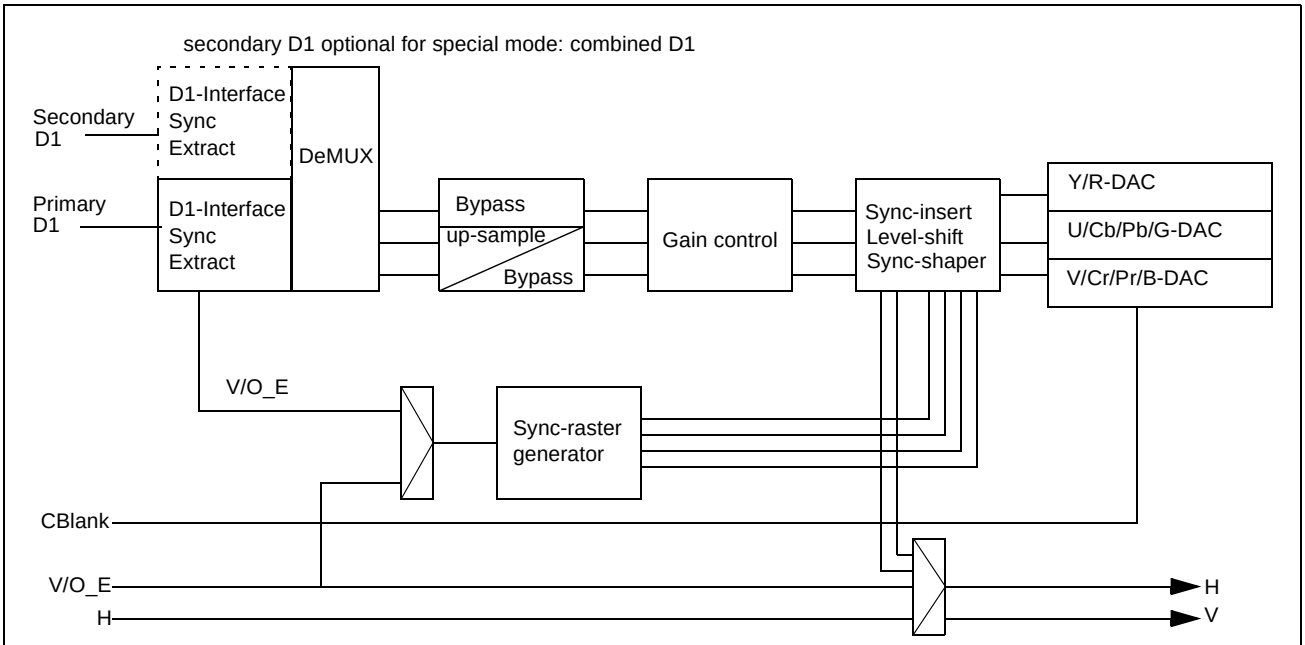


Figure 14: Primary Display Pipe (HD Operation Mode)

2.6 PAL/NTSC/SECAM Encoder

2.6.1 General

The PAL/NTSC/SECAM encoder accepts the YUV data and encodes it into an NTSC, PAL or SECAM video signal. From Y, U and V data, the encoder generates luminance, chrominance and subcarrier output signals, suitable for use as CVBS or separate Y and C signals.

Luminance is modified in gain and in offset (offset is programmable to enable different black level setups). In order to enable easy analog post filtering, luminance is interpolated from a 13.5 MHz data rate to a 27 MHz data rate, providing luminance in 10-bit resolution. This filter is also used to define smoothed transients for synchronization pulses and the blanking period.

Chrominance is modified in gain (programmable separately for U and V). The standard dependent burst is inserted before baseband color signals are interpolated from a 6.75 MHz data rate to a 27 MHz data rate.

One of the interpolation stages can be bypassed, thus providing a higher color bandwidth, which can be used for Y and C output. The FSC bits set the subcarrier frequency. To make sure the subcarrier is locked to the line frequency, as the standards require, the sync generator is able to reset the subcarrier generation periodically. This feature is controlled by the PHRES programming bits. These features are available to generate a standard interlaced signal; they will not work in non-interlaced mode.

A crystal-stable master clock of 27 MHz, which is twice the CCIR line-locked pixel clock of 13.5 MHz, is received from the interface clock pins. The encoder synthesizes all necessary internal signals, color subcarrier frequency, and synchronization signals from that clock.

For ease of analog post filtering, the signals are twice oversampled with respect to the pixel clock before digital-to-analog conversion.

Programming flexibility includes NTSC-M, PAL-B, SECAM main standards as well as other variations. A number of possibilities are provided for setting different video parameters, such as:

- Black and blanking level control
- Color subcarrier frequency
- Variable burst amplitude

The sync generator generates all the signals required to control the signal processing, provide the composite sync signal, insert the color burst, etc.

The encoder includes a cross-color reduction filter to reduce cross talk between the luminance and chrominance channels. In the CVBS signal, the signal amplitude is reduced by 15/16 to avoid overflow.

2.6.2 Luminance and Chrominance Processing

The Y processing provides a high performance 5 MHz lowpass filter. It adjusts the level range according to the standard and inserts the sync and blanking pulses. The insertion stage generates the correct pulse shapes. No further processing is necessary of the D/A converters for this purpose.

Chroma processing operates on the baseband signals as long as possible. At first, the signal amplitudes are adjusted and the burst is inserted. Afterwards the signals are passed through a 1.4 MHz lowpass filter. This filter can be switched to a higher cut-off frequency to allow more chroma bandwidth with S-Video. The quadrature modulator uses a DTO with 32-bits resolution for the subcarrier generation. Even with this high resolution, the DTO cannot generate the carrier locked to the line frequency as the standards require without further means. So the sync generator is able to reset the DTO periodically. This feature is controlled by the PHRES programming bits. These modes may only be switched on if the encoder is programmed to generate a standard signal; they will not work in non-interlaced mode.

2.6.3 Sync Generator

The sync generator is the timing master of the encoder. It generates all the signals required to control the signal processing, provide the composite sync signal, insert the color burst, etc. Via the FISE control bit, the circuit can be set to generate 50 Hz patterns for e.g., PAL B or 60 Hz patterns (NTSC M). It is possible to modify the number of lines per field by ±0.5 lines to generate a non-interlaced output signal. The sync generator also provides HS, VS and O_E signals to control the rest of the encoder.

2.6.4 Macrovision

PNX8510

The encoder supports Macrovision™ Anti-Taping for both NTSC and PAL. There is no Macrovision insertion for SECAM defined, however for AGC Pseudo Sync and BP pulses the same settings used for PAL could be used for SECAM. The different steps of this process can be programmed separately. The Macrovision control block provides all necessary timing and level information for inserting the correct pulses in the CVBS/Y/C/RGB/YUV data stream. Furthermore it provides the signals used to modify the subcarrier generator according to the Macrovision Burst Inversion requirements.

The encoder uses a blanking level during the vertical blanking interval that is defined by the value of BLNVB, thus providing two different programmable blanking levels. Outside vertical blanking, value of BLNNL is effective, which should be reduced according to Macrovision requirements. The copy protection means can be activated independently by the respective control bits. The copy protection mechanism is optional and will be enabled by bonding a die-pad to either VDD or VSS.

PNX8511

Macrovision is not available in the PNX8511.

2.7 HD Data Path

The high definition data path of the PNX8510/11 IC features an up-sampling filter, gain control and a universal sync insertion engine.

Input formats supported by the high definition data path are:

Double D1 mode:16/20 bit 422 (8/10 bit for Y and 8/10 bit for U/V); DEMUX_MODE set to 3’b011

Single interface HD 422 mode (UYVY 422 D1 format); DEMUX_MODE set to 3’b100

Single interface 444 (RGB/YUV 444 format); DEMUX_MODE set to 3’b001

Full 24/30 bit parallel input mode (YUV/RGB 444 formats); VMODE set to zero

RGB and YUV data types are accepted. However, there is no color space conversion in the HD data path so the input data type has to match the display data type.

The up-sampling filter can be applied to convert incoming 422 data formats to 444.

The data path also provides individual gain control for RGB/YUV which allows a +/- 0.5x amplitude change (HD_GAIN_R/Y, HD_GAIN_U/G, HD_GAIN_V/B control registers).

The HD sync insertion module following the filter and gain control circuits provides flexible insertion of synchronization signals into the Y, Y and V or R, G and B data paths. The insertion can be chosen on a component basis (Y/R_SYNC_INS_EN, U/G_SYNC_INS_EN, V/B_SYNC_INS_EN control registers) and the sync generator provides individual tables for the components. A more detailed description of the sync generator can be found in the next paragraph.

2.8 HD-Sync Generator Module

This section describes the operation and programming of the high definition (HD) video data path sync unit.

The module’s purpose is to provide the video data path that bypasses the digital video encoders with the appropriate synchronization pattern. The module design provides maximum flexibility in terms of raster generation for all interlaced and non-interlaced ATSC formats. The sync engine is

capable of providing a combination of event-value pairs which can be used to insert certain values at specified times in the outgoing data stream. It can also be used to generate digital signals associated with time events. They can be used as digital H- and V-synchronization signals.

The sync raster generation is fully programmable to accommodate different requirements. The raster generation can be either progressive or interlaced. Digital sync signal generation (H, V, Blank) as well as analog embedded sync generation are supported. The picture position is adjustable through the programmable relation between the sync pulses and the video contents.

The generation of embedded analog sync pulses is bound to a number of events which can be defined for a line. Several of these line-timing definitions can exist in parallel. For the final sync raster composition a certain sequence of lines with different sync event properties has to be defined. The sequence specifies a series of line types and the number of occurrences of this specific line type.

After the sequence has completed, it restarts from the beginning. In this way, the sync raster generation is generic and can be adopted to different standards (different sync shapes, various H-timing, interlaced, progressive...). However, to generate a stable picture, it is important that the sequence fits precisely to the incoming data stream in terms of the total number of pixels per frame.

The sync engine's flexibility is achieved by using a sequence of linked lists carrying the properties for the image, the lines as well as fractions of lines. The list dependencies are illustrated in Figure 15.

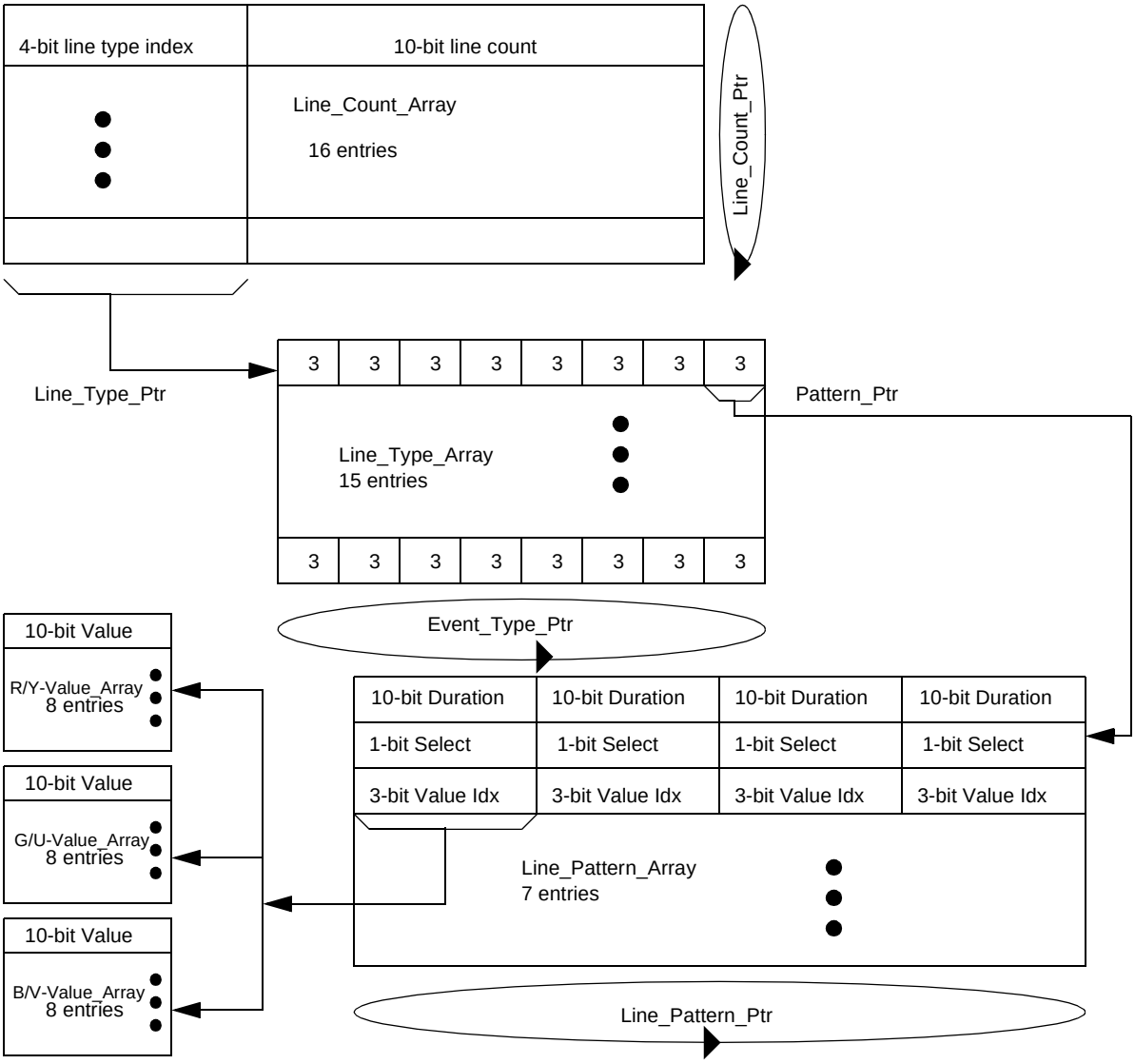


Figure 15: Sync Engine List Dependencies

The first table is called "Line_Count_Array" and serves as an array to hold the correct sequence of lines composing the synchronization raster. It can contain up to 16 entries. Each entry holds a 4-bit index (counted from 1 through 16)) and a 10-bit counter value.

The 4-bit index is a pointer to a line in the next table called "Line_Type_Array." A 10-bit counter value specifies how often this particular line is repeated. If the necessary line count for a particular line exceeds the 10 bits, it has to use two table entries. This table has to be terminated with a dummy entry containing a '0' index and '0' line count.

The second table, "Line_Type_Array" holds up to 15 entries (counted from 1 through 15). Each entry can contain up to eight index pointers. It is possible to have less than eight index pointers in any entry, in which case those index pointers should be filled with '0.' Each index pointer

points to a line with that index in the next table called “Line_Pattern_Array.” These pointers represent parts of a line raster. A line may be split up into a sync, a blank and an active portion followed by another blank portion, which would require four index pointers in one entry of the table.

The third table is called “Line_Pattern_Array” and it can contain a maximum of seven entries (counted from 1 though 7). The entries are used to define portions of a line representing a certain value for a certain number of clock cycles. Each of these seven entries can store up to four groups of “duration, select and value index.” It is possible to have less than four groups in any entry, in which case those groups should be filled with ‘0.’ ”Duration” is a 10-bit value representing the number of clock cycles. “Select” indicates whether the value is actually inserted into the video data stream or not. “Value index” is a 3-bit index into another array called “value array.” Certain bits of the “value index” can also be used to generate a digital sync raster provided at the H- and V-sync outputs of the PNX8510/11.

“Value array” can hold up to 8 values (counted from 0 though 7) which are 10-bit signed.

To ease the trigger setup for the sync generation module, a set of registers is provided to set up the screen raster defined as width and height. A trigger position can be specified as an x, y coordinate within the overall dimensions of the screen raster. If the x, y counter matches the specified coordinates, a trigger pulse is generated which pre-loads the tables with their initial values.

The listing below outlines an example on how to set up the sync tables for a 1080i HD raster:

```
// hd-sync config file for 1080i
#line_count_array
//index         //line_count
----------------------------------------
2               5           //5 lines vsync
4               1           //1 line sync-black-sync-black
6               14          //14 lines blank
1               537         //537 lines active video
6               5           //5 lines blank
5               1           //1 line sync-black-sync-blank
2               4           //4 lines sync
3               1           //1 line sync blank sync black
6               15          //15 lines blank
1               537         //537 lines active video
6               5           //5 lines blank
0               0           //dummy lines
0               0           //dummy lines
0               0           //dummy lines
0               0           //dummy lines
0               0           //dummy lines
#line_type_array
//p8    p7  p6  p5  p4  p3  p2  p1
--------------------------------------------------------------------------------
0       0   0   0   0   0   3   4 //sync-full active line
0       0   0   0   2   4   2   4 //sync-half blank-sync-half blank
0       0   0   0   1   4   2   4 //sync-half blank-sync-half black
0       0   0   0   1   4   1   4 //sync-half black-sync-half black
0       0   0   0   2   4   1   4 //sync-half black-sync-half blank
0       0   0   0   0   0   5   4 //sync-full line black
0       0   0   0   0   0   0   0
```

```
0       0   0   0   0   0   0   0
0       0   0   0   0   0   0   0
0       0   0   0   0   0   0   0
0       0   0   0   0   0   0   0
0       0   0   0   0   0   0   0
0       0   0   0   0   0   0   0
0       0   0   0   0   0   0   0
0       0   0   0   0   0   0   0
#line_pattern_array
//d=dur s=sel v=value
//d4    s4  v4  d3  s3  v3  d2  s2  v2  d1  s1  v1
-----------------------------------------------------
0       0   0   0   0   0   43  1   3   879 1   3 //half line black
0       0   0   0   0   0   43  1   3   879 1   0 //half line blank
43      1   3   959 0   6   959 0   6   59  1   3 //full active line
0       0   0   87  1   3   43  1   2   43  1   1 //sync pulse
43      1   3   959 1   3   959 1   3   59  1   3 //full line black
0       0   0   0   0   0   0   0   0   0   0   0
0       0   0   0   0   0   0   0   0   0   0   0

#value_array Y
//signed values
-------------------------------------
-512        //broad pulse level 0
-512        //lower sync tip 0
102         //upper sync tip 600
-204        //black/blank level org 204
0
0
0
0

#value_array U
//signed values
-------------------------------------
0           //broad pulse level 0
-432        //lower sync tip 0
432         //upper sync tip 600
0           //black/blank level org 0
0
0
0
0

#value_array V
//signed values
-------------------------------------
0           //broad pulse level 0
-432        //lower sync tip 0
432         //upper sync tip 600
0           //black/blank level org 250
```

```
0
0
0
0
```

A complete example of register settings for 1080i is given in Section 11. Video Programming Examples.

The listing below outlines an example on how to set up the sync tables for a 720p raster:

```
// hd-syn config file for 720p

#line_count_array
//index     line_count
2           5           //5 lines vsync
3           20          //20 lines blank
1           360         //360 lines active video
1           360         //360 lines active video
3           5           //5 lines blank
0           0           //dummy lines
0           0           //dummy lines
0           0           //dummy lines
0           0           //dummy lines
0           0

#line_type_array
//p8    p7  p6  p5  p4  p3  p2  p1
0       0   0   0   0   0   3   4 //sync-full line active
0       0   0   0   0   0   2   4 //sync-full line blank (vsync)
0       0   0   0   0   0   5   4 //sync-full line black (v-blanking)
0       0   0   0   0   0   0   0
0       0   0   0   0   0   0   0
0       0   0   0   0   0   0   0
0       0   0   0   0   0   0   0
0       0   0   0   0   0   0   0
0       0   0   0   0   0   0   0
0       0   0   0   0   0   0   0
0       0   0   0   0   0   0   0
0       0   0   0   0   0   0   0
0       0   0   0   0   0   0   0

#line_pattern_array
//dur4 sel4 val4 dur3 sel3 val3 dur2 sel2 val2 dur1 sel1 val 1
0      0    0    0    0    0    0    0    0    0    0    0 //empty
0      0    0    69   1    3    714  1    0    714  1    0 //full line blank
69     1    3    639  0    0    639  0    0    149  1    3 //full line active
0      0    0    69   1    3    39   1    2    39   1    1 //sync pulse
69     1    3    639  1    3    639  1    3    149  1    3 //full line black
0      0    0    0    0    0    0    0    0    0    0    0
0      0    0    0    0    0    0    0    0    0    0    0
```

```
#value_array Y
//signed values
-------------------------------------
-512        //broad pulse level 0
-512        //lower sync tip 0
102         //upper sync tip 600
-204        //black/blank level org 204
0
0
0
0

#value_array U
//signed values
-------------------------------------
0           //broad pulse level 0
-432        //lower sync tip 0
432         //upper sync tip 600
0           //black/blank level org 0
0
0
0
0

#value_array V
//signed values
-------------------------------------
0           //broad pulse level 0
-432        //lower sync tip 0
432         //upper sync tip 600
0           //black/blank level org 250
0
0
0
0
```

2.9 Limitations of the Video Pipe

In all HD modes, the video encoder will be switched off. Either a separate sync signal or the embedded syncs of the D1 input can be used to generate the sync raster driving the display device.

3. Audio Pipeline

The PNX8510/11 has two independent stereo channels, each connected to a separate audio interface. The primary audio channel is usually associated with the primary video channel and carries the accompanying sound information. The secondary audio channel usually carries the audio belonging to the record (secondary) video channel. Because they might originate from different sources, the two interfaces are operated by independent clocks.

Mute on/off is programmable by a register setting. Table 12 describes the expected audio performance.

Table 12: Audio Performance

Parameter	QFP100
Dynamic Range	85dB
S/(N+Disto.)	>85dB

The audio path has three general blocks: input, interpolation, and DAC.

- The input is, by default, a 24-bit I^2S interface. However, it can be programmed to accept other formats.
- The interpolator scales, filters and oversamples the incoming data by 64 x its sampling frequency. The result goes to a Noise Shaper, which shifts in-band noise to frequencies well above the audio spectrum. This provides a very high signal-to-noise ratio.
- Finite Impulse Response DACs convert the 1-bit data stream to analog output voltage.

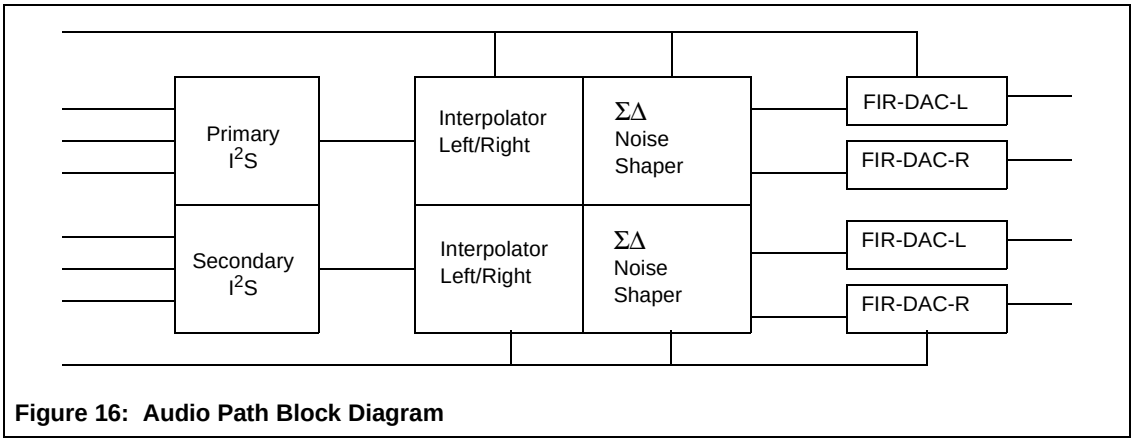


Figure 16: Audio Path Block Diagram

3.1 Audio Interface Operation

The audio interfaces can be operated in either slave or master mode:

- In slave mode, all required clocks (System CLK, SCK and WS) must be generated externally and must be synchronous with each other.
- In master mode, the PNX8510/11 only gets the System CLK and generates SCK and WS clocks synchronously to the applied System CLK. In this mode, System CLK is equal to 128 x Fs where Fs is the audio sampling frequency.

3.1.1 Audio Input Timing

The following timing diagrams illustrate the different modes of operation for the I^2S interface used in the PNX8510/11.

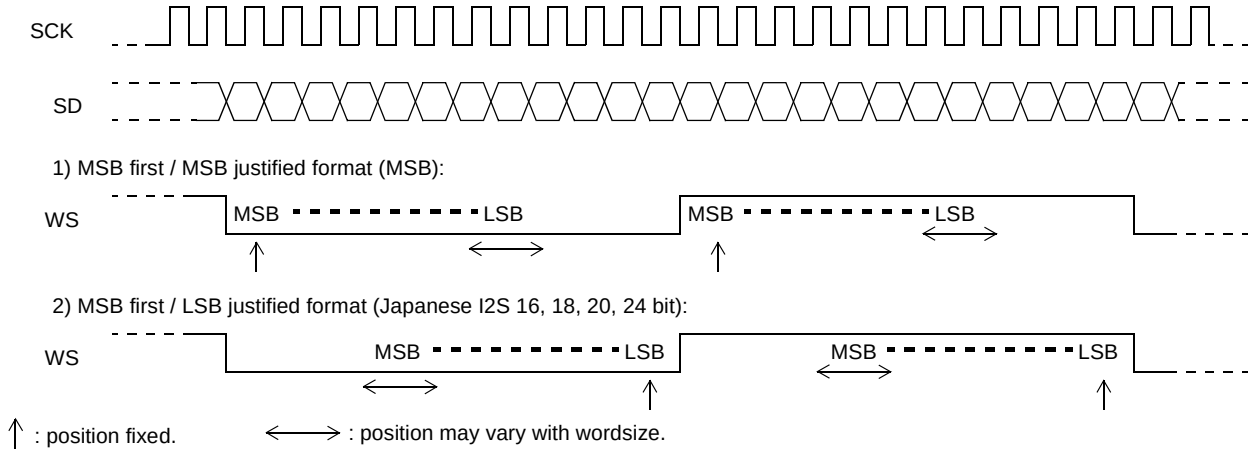


Figure 17: Input Formats. Justification bit is not delayed.

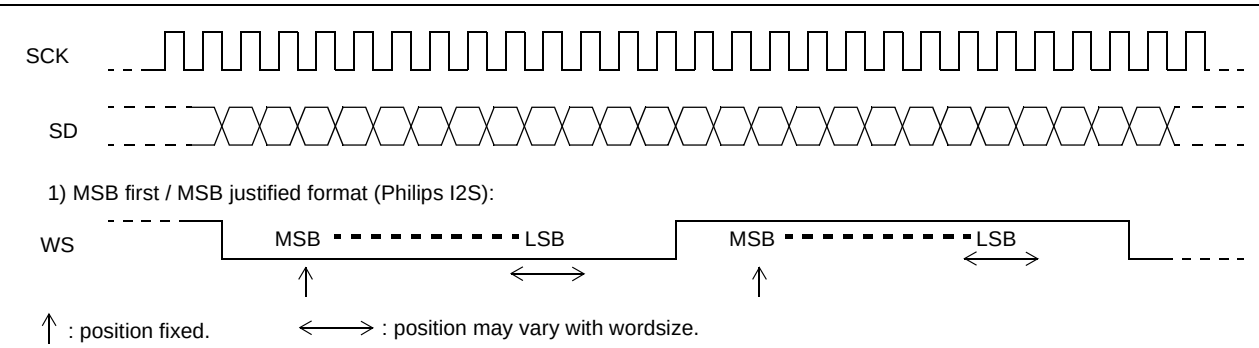


Figure 18: Input Format. Justification bit is one bit clock delayed.

Table 13: I^2S Signals

Port	Description
SCK	Bit clock
SD	PCM data
WS	Word Select; left right clock is equal to the sample rate.

3.2 Mute Modes

The audio modules of the PNX8510/11 have several mute functions. The mute operation is controlled via the programming registers quickmute, and mutemode.

Quick Mute: This is an overriding quickmute on the master channel, which mutes the interpolator output signal in 32 samples using the cosine roll-off coefficients. This means whenever the quickmute register is set to one, independent of what the mute setting of the microcontroller is, the output is muted.

Mute Mode: this register sets the mute mode for the MASTER MUTE to either soft mute (setting is ‘0’) or to quick mute (setting = ‘1’). For the master channel the quickmute function and the microcontroller mute function are OR’d.

Table 14: Mute Mode Control

Quick Mute	Microcontroller Mute	Function
0	0	No mute
0	1	1 microcontroller mute...mute mode depends on the ‘mutemode’ setting.
1	X	Overriding quick mute function

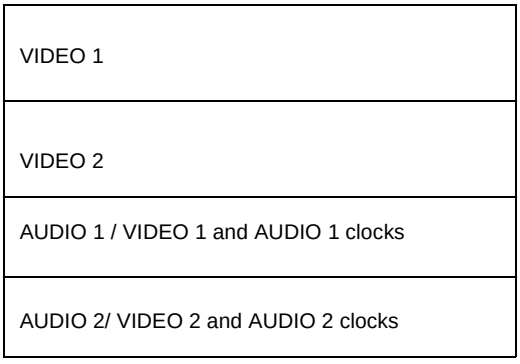
Table 15: Mute Mode Function

Mute Mode	Function
0	Mute function via micro controller interface is set to “soft mute.”
1	Mute function via micro controller interface is set to “quick-mute.”

4. Programming Interface

The configuration of the various interface modes and the digital video encoder setup can be controlled via an I^2C interface or a special VBI data packet sent during the horizontal blanking interval. With the VBI programming interface, a reliable real-time programming for the PNX8510/11 video blocks can be accomplished. For instance, this mode makes it very easy to carry the necessary programming data over to the digital encoder to encode a certain teletext packet in a specific scanline without extensive buffering. The format for programming registers in the PNX8510/11 via the VBI interface can be found in Section 2.5. Note that reprogramming clocks and audio registers are not possible via the VBI interface.

The PNX8510/11 is an I^2C slave device only. It uses four dedicated slave addresses to address the primary, secondary, audio and remaining control registers. The I^2C address set can be configured during reset with a pullup or pulldown combination of GPIO pins. Figure 19 below illustrates an example of how the I^2C device addresses are determined.



IIC address selection example:

GPIO5-2 are set to logic one and GPIO1 is set to zero during Anabel rest.

Address= GPIO5-GPIO4-XY-GPIO3-GPIO2-GPIO1-R/W

Address= 1-1-XY-1-1-0-R/W
VIDEO1= 1-1-0-0-1-1-0-R/W = 0xCC(write), 0xCD(read)
VIDEO2= 1-1-0-1-1-1-0-R/W = 0xDC(write), 0xDD(read)
AUDIO1= 1-1-1-0-1-1-0-R/W = 0xEC(write), 0xED(read)
AUDIO2= 1-1-1-1-1-1-0-R/W = 0xFC(write), 0xFD(read)

Figure 19: I^2C Address Determination

A detailed description of all programming registers can be found in Section 8. on page 29.

Note: Both video clocks have to be connected to the device for proper functioning of the I^2C programming interface.

5. GPIO Block Functional Description

GPIOs are multi-purpose pins. They may be programmed as input/output and used to carry signals into the IC or to monitor the status of the IC. The selection of these I/O pins is controlled through programmable registers. The GPIO module can be programmed via subaddress 90-95 of the primary video pipe.

5.1 Overview

The GPIO pins operate in two basic modes: Bootstrap mode and GPIO mode

During chip reset the GPIOs are in bootstrap mode. The status of all GPIO pins is monitored and used to determine the set of I^2C device addresses the IC responds to.

After the chip reset is released, the GPIO pins may be used in GPIO mode. In output mode each GPIO pin can be set to logic one or zero by programming the appropriate register. In input mode the status of each GPIO can be monitored by reading the appropriate status register. In addition to the register-driven I/O mode, some of the GPIO pins are used to reflect the status of internal signals. Some GPIO pins are also used as additional inputs to functional units if operated in input mode.

5.2 Operation

GPIO Set During Reset

During reset the GPIO output is disabled. GPIO_in is stored as gpio_in_stored and retains its value until the next reset. This stored value determines the I^2C device addresses. After reset, GPIO pins can be programmed for output with the OEN and OUT_SEL bits.

The I^2C subaddresses are derived from the GPIOs in the following way:

Primary video pipe: {gpio5,gpio4,0,0,gpio3,gpio2,gpio1}

Secondary video pipe: {gpio5,gpio4,0,1,gpio3,gpio2,gpio1}

Primary audio pipe: {gpio5,gpio4,1,0,gpio3,gpio2,gpio1}

Secondary audio pipe: {gpio5,gpio4,1,1,gpio3,gpio2,gpio1}

Checking/Setting the GPIO Status

Each GPIO pin is multiplexed four times to increase usability. The Figure 20 outlines the internal structure of one GPIO pin. In output mode the selection of the signal routed out to a GPIO pin is performed with the OUT_SEL register bits. The OEN bit is low active and enables the GPIO output mode. If OUT_SEL is set to 2'b11 and the OEN bit is set to zero, the GPIO pin can be set or reset by writing a one or zero into the STATUS location of the GPIO register. All other OUT_SEL settings are listed in 0x90—0x94 GPIO5-GPIO1 (0x90=GPIO1, ..., 0x94=GPIO5) Not present in secondary video channel.

To read the external status of a GPIO pin, the OEN needs to be set to one to avoid conflicts with signals routed out of the chip. If GPIO_IN_EN4 is set to one, the status of the GPIO pin can be monitored by reading the STATUS bit of the appropriate GPIO register. The function of all relevant GPIO_IN/OUT signals are listed in Figure 20 and Table 16.

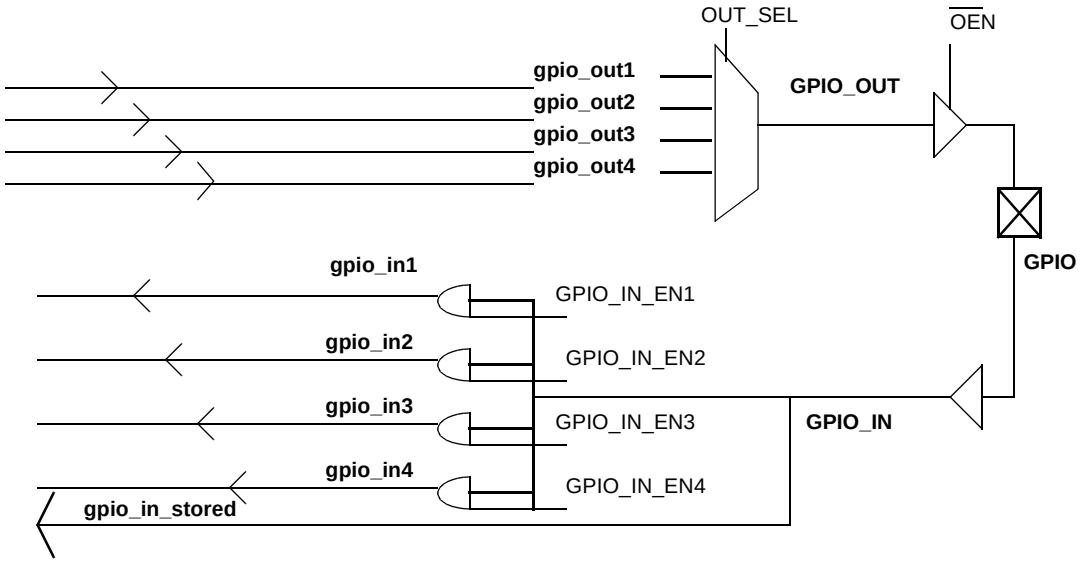


Figure 20: Operation Modes for one GPIO in the PNX8510/11

Table 16: Specific GPIO Assignments

Signal	Description
gpio5_out1	Composite sync secondary encoder
gpio5_out2	Vertical sync primary encoder
gpio5_in3	30-bit parallel video input mode: bit[1] = red channel
gpio4_out1	Data request secondary encoder
gpio4_out2	Composite sync primary encoder
gpio4_in3	30-bit parallel video input mode: bit[0] = red channel
gpio3_out1	Enable y secondary encoder (1/2 of the encoder operation frequency)
gpio3_out2	Odd/even signal primary encoder
gpio3_in1	Real time control input primary encoder
gpio3_in2	Real time control input secondary encoder
gpio3_in3	30-bit parallel video input mode: bit[1] = green channel
gpio2_out1	Odd/even signal secondary encoder
gpio2_out2	Data request primary encoder
gpio2_in3	30-bit parallel video input mode: bit[0] = green channel
gpio1_out1	Vertical sync secondary encoder
gpio_in3	30-bit parallel video input mode: bit[0] = blue channel
All other settings are reserved for future use.	

6. Clock Module

All of the PNX8510/11 modules receive their input clocks from the clocks module. The top level structure of the clocks module is shown below.

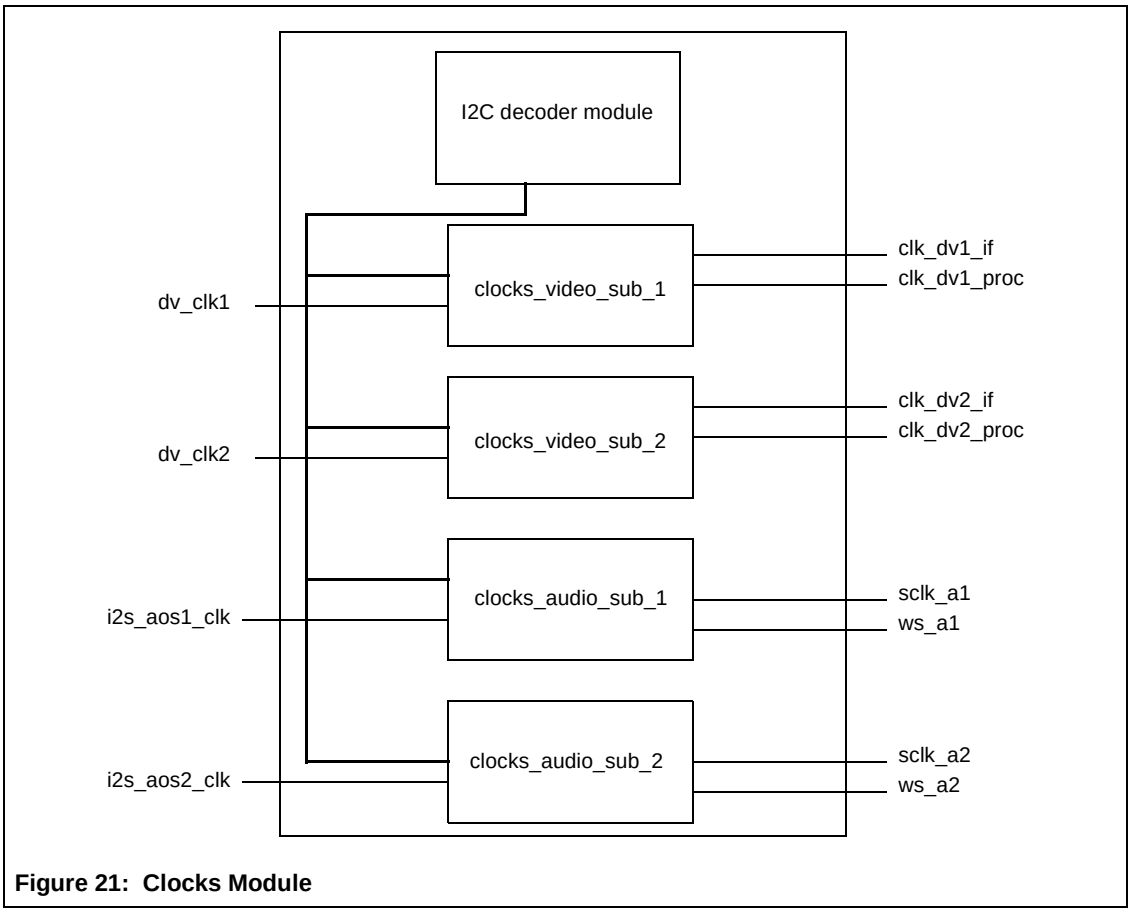


Figure 21: Clocks Module

The PNX8510/11 in normal operation mode receives four external clocks. Two clocks dv_clk1 and dv_clk2 are the clocks used for the primary and secondary video data paths. The other two clocks assemble the audio over-sampling clocks for the primary and secondary audio channel.

The PNX8510/11 video clocks are used to create two internal clocks: one for operating the video input interface (clk_dv1_if, clk_dv2_if), and one for operating the main video processing pipeline (clk_dv1_proc, clk_dv2_proc).

The audio interface normally operates in slave mode (over-sampling clock, word select and bit clock are provided from the externally connected I2S master). However the PNX8510/11 can be operated in master mode. This mode only requires the over-sampling clock to be provided. The bit clock and the word select signals are subdivided from the over-sampling clock and provided to the chip pins.

6.1 Clocks Video Submodule

The generation of the various clock signals needed for video pipelines takes place in the clocks video module. Figure 22 shows a block diagram of this module. The configuration registers for the clocks module can be found in Section 10. Audio/Clock Address Space.

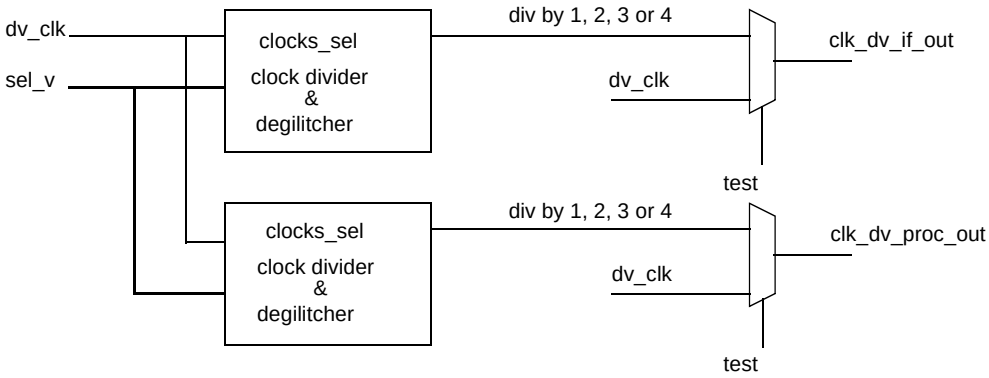


Figure 22: Clocks Video Submodule

6.2 Clocks Audio Submodule

The input clocks for the audio block are generated in the clocks audio submodule. Figure 23 shows a block diagram for this submodule.

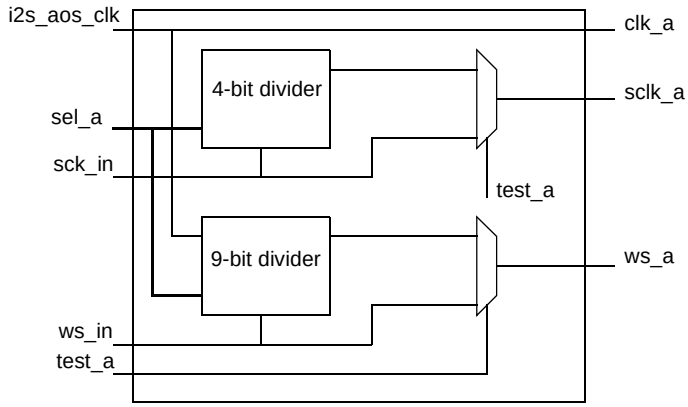


Figure 23: Clocks Audio Submodule

7. Test Mode

This section describes how the analog test modes are implemented in the PNX8510/11. Note that these test modes are intended for production test only. The chip needs to be brought into analog test mode via the JTAG boundary scan controller. Once the chip is in analog test mode the different test modes can be enabled via the GPIO pins. The data input for the video DAC's is provided via the DV1 interface for DACs 1 through 4 and via the DV2 interface for DACs 5 and 6 respectively. The "main switch" for the test mode is controlled by the JTAG boundary scan controller. Once the chip is in analog test mode, the GPIO pins can be used to select certain combinations outlined in the tables.

Table 17: Video DAC Test Modes

GPIO2	GPIO3	Test
0	0	VDAC1 and VDAC5 active
0	1	VDAC2 and VDAC6 active
1	0	VDAC3 and VDAC5 active
1	1	VDAC4 and VDAC6 active

For the video DACs 1 to 4, the primary 10-bit D1 interface (DV1_IN[9:0]) provides the 10-bit input. Video DACs 5 and 6 are stimulated through the secondary D1 interface (DV2_IN[9:0]).

Table 18: Audio DAC Test Modes

GPIO4	GPIO5	Test
0	0	ADAC1/2 and ADAC3/4 stereo pair first and second channel off
0	1	ADAC1/2 stereo pair first channel active
1	0	ADAC3/4 stereo pair second channel active
1	1	ADAC1/2 and ADAC3/4 stereo pair first and second channel active

The serial audio data streams for the first stereo pair are provided through the I2S_IN1_SD and the I2S_IN1_WS pins. The audio DAC pair 3 and 4 get their serial data through pins I2S_IN2_SD and I2S_IN2_WS.

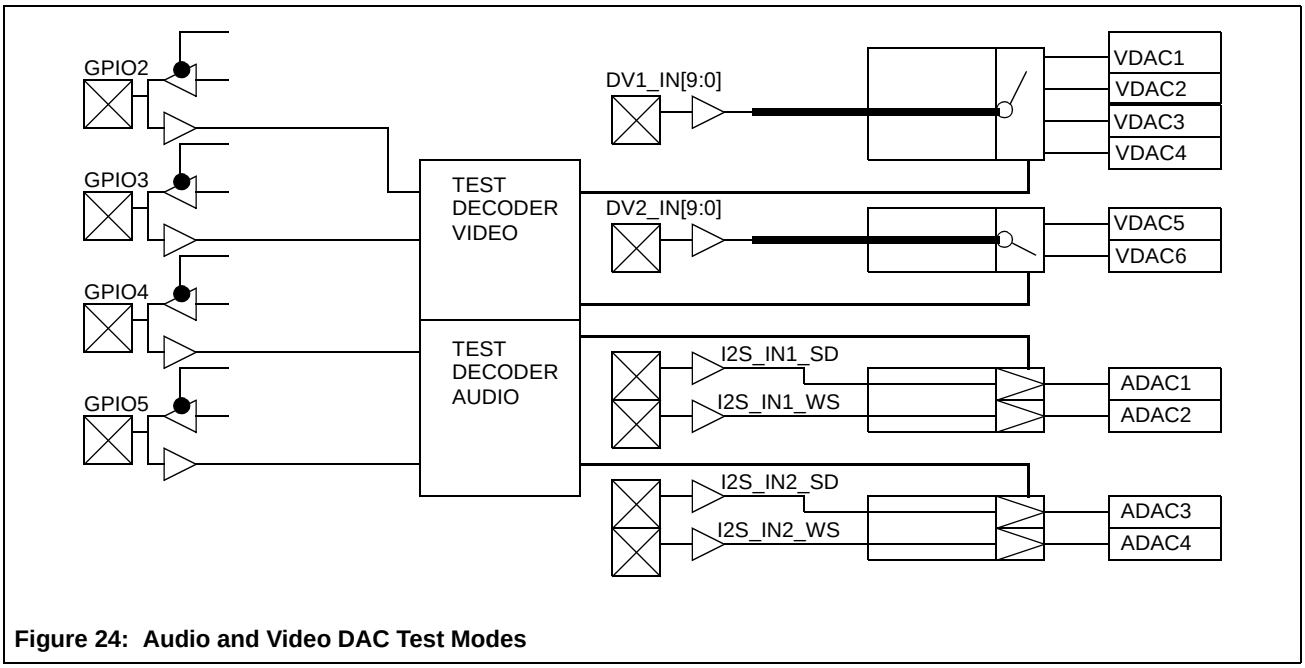


Figure 24: Audio and Video DAC Test Modes

8. Register Descriptions

The PNX8510/11 register space is divided into four different spaces. Each of them is addressed by a different I^2C device address. The first address space is dedicated to the primary video channel, the second space belongs to the secondary video channel. The third I^2C address space accommodates the registers that control the first audio channel. The fourth I^2C space is used to address the secondary audio channel.

The video channel registers are only listed once. Because the secondary video channel does not support high definition or RGB output, its registers have some minor differences, which are noted in the following tables as “Not present in secondary video channel.”

The slave addresses are selectable during boot. The registers for the primary and secondary audio and video modules are identical, except as noted in the register definitions. The following tables provide the offset—the base address is dependent on the module.

The actual address spaces are determined at boot time according to the GPIO settings. For more information, refer to Section 4. on page 24.

Table 19: PNX8510/11 Register Summary

Address	Name	Description
Video Address Space		
0x00	STATUS	Status register
0x1A	MSMT	Monitor sense mode threshold
0x1B	MSMS	Monitor sense mode status
0x26	WSS1	Wide screen signaling data
0x27	WSS2	Wide screen signaling enable
0x28	BCTL	Burst control
0x29	BCTL2	Burst control
0x2A	CGD1	Copy guard
0x2B	CGD2	Copy guard
0x2C	CGD	Copy guard enable
0x2D	DACCTL	DAC control *****
0x38	GAIN_Y	Gain adjust for Y component (SD RGB/YUV data path) *****
0x39	GAIN_UV	Gain adjust for UV component (SD RGB/YUV data path) *****
0x3A	INPCTL	Input control register *****
0x54	VPS1	Video programming system
0x55	VPS2	Video programming system
0x56	VPS3	Video programming system
0x57	VPS4	Video programming system
0x58	VPS5	Video programming system
0x59	VPS6	Video programming system
0x5A	CHPS	Color subcarrier phase
0x5B	GAINU	Gain adjust for U component
0x5C	GAINV	Gain adjust for V component
0x5D	BLCKL	Black level adjust
0x5E	BLNNL	Blank level adjust
0x5F	BLNVB/CCR	Cross color reduction / blank level (during vertical blank)
0x61	STDCTL	Video standard control
0x62	BSTA	Burst amplitude control
0x63—66	FSC0-FSC3	Color subcarrier frequency control
0x67	L21O0	Closed captioning odd field
0x68	L21O1	Closed captioning odd field

Table 19: PNX8510/11 Register Summary (Cont'd.)

Address	Name	Description
0x69	L21E0	Closed captioning even field
0x6A	L21E1	Closed captioning even field
0x6C	TRGCTL1	SD trigger control
0x6D	TRGCTL2	SD trigger control
0x6E	MULTICTL	Sync and blank control
0x6F	TTXCTL	VBI insertion control
0x70	ADWHS	Active display window start
0x71	ADWHE	Active display window end
0x72	ADWHS/E	Active display window - MSB
0x73	TTXHS	TTX control
0x74	TTXHL/TTXHD	TTX control
0x75	CSYNCA	Composite sync control
0x76	TTXOVS	TTX insertion control odd field
0x77	TTXOVE	TTX insertion control odd field
0x78	TTXEVS	TTX insertion control even field
0x79	TTXEVE	TTX insertion control even field
0x7A	FAL	First active line
0x7B	LAL	Last active line
0x7C	TTXCTRL	TTX format control
0x7E	DTTXL	TTX mask
0x7F	DTTXL2	TTX mask
0x80	LCNT_ARRAY_LINE	HD sync generator control *****
0x81	LCNT_ARRAY_LINE	HD sync generator control *****
0x82	LCNT_ARRAY_ADR	HD sync generator control *****
0x83—0x85	LTYPE_ARRAY_LINE	HD sync generator control *****
0x86	LTYPE_ARRAY_ADR	HD sync generator control *****
0x87—0x8D	LPATT_ARRAY_LINE	HD sync generator control *****
0x8E	LPATT_ARRAY_ADR	HD sync generator control *****
0x90—0x94	GPIO5-GPIO1	GPIO control *****
0x95	VMUXCTL	Video input mode control *****
0x96—0x97	VALUE_ARRAY_LINE	HD sync generator control *****
0x98	VALUE_ARRAY_ADR/ EVENT_TYPE_PTR	HD sync generator control *****
0x99—0x9A	TRIGGER_LINE	HD sync generator control *****
0x9B—0x9C	TRIGGER_DURATION	HD sync generator control *****
0x9D	TRIGGER_PTR	HD sync generator control *****
0x9E	BLANK_Y	Programmable blank level for Y (SD RGB/YUV data path) *****
0x9F	BLANK_UV	Programmable blank level for UV (SD RGB/YUV data path) *****
0xA0	RGB_CTRL	Color space matrix bypass enable *****

Table 19: PNX8510/11 Register Summary (Cont'd.)

Address	Name	Description
0xA2	BORDER_Y	Border color
0xA3	BORDER_U	Border color
0xA4	BORDER_V	Border color
0xA5	MISCCTRL	DAC and trigger control *
0xA6	HDCTRL	HD video path control *
0xA7	SYNC_DELAY	Sync and VBI programming control
0xA8	BLANK_R/Y	Blank offset control HD video path *
0xA9	BLANK_G/U	Blank offset control HD video path *
0xAA	BLANK_B/V	Blank offset control HD video path *
0xAE	SYNC_HEIGHT1	HD sync generator screen height *
0xAF	SYNC_HEIGHT2	HD sync generator screen height *
0xB0	SYNC_WIDTH1	HD sync generator screen width *
0xB1	SYNC_WIDTH2	HD sync generator screen width *
0xB2	SYNC_TRIGPOS_Y1	HD sync generator vertical position control1 *
0xB3	SYNC_TRIGPOS_Y2	HD sync generator vertical position control2 *
0xB4	SYNC_TRIGPOS_X1	HD sync generator horizontal position control1 *
0xB5	SYNC_TRIGPOS_X2	HD sync generator horizontal position control2 *
0xB6	SIG1	Video signature *
0xB7	SIG2	Video signature *
0xB8	SIG3	Video signature *
0xB9	SIG4	Video signature *
0xBA	SIGCTRL	Video signature analyzer control *
0xBC	BLANK_MSBs	Blank offset control *
0xBE	R/Y Value Array Line	R/Y value aray data *
0xBF	B/U Value Array Line	B/U value aray data *
0xC0	G/V Value Array Line	G/V value aray data *
0xC1	Value Array Line MSBs	Value aray data MSBs *
0xC2	DAC1 ADJ	Coarse current control DAC1 *
0xC3	DAC2 ADJ	Coarse current control DAC2 *
0xC4	DAC3 ADJ	Coarse current control DAC3 *
0xC5	DAC4 ADJ	Coarse current control DAC4 *
0xC6	DACC ADJ	Common current fine adjust for DACs 1-4 *
0xC7	HD_Gain R/Y	Gain adjust HD path *
0xC8	HD_Gain G/U	Gain adjust HD path *
0xC9	HD_Gain B/V	Gain adjust HD path *
Audio/Clock Address Space		
0x0000	CLK_AUDIO	Audio clock control
0x0001	CLK_IF	Video interface clock control

Table 19: PNX8510/11 Register Summary (Cont'd.)

Address	Name	Description
0x0002	CLK_PROC_DIV	Video processing clock control
0x0003	CLK_DAC_DIV	Video DAC clock control
0x00F4	I^2S_SET_REG	Audio interface control
0x00F5—00FB	FEATURE_REG	Audio feature control
0x00FC	INTERPOLATOR_REG1	Audio feature control
0x00FD	INTERPOLATOR_REG2	Audio feature control
0x00FE	Audio DAC power on register	Audio DAC control
Note: Register entries indicated with an asterisk (*****) have a different meaning or are not present in the secondary video address space. For more details, refer to the register description.		

9. Video Address Space

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x00			***STATUS***	
7	R	0	VER2	Version ID bit 2
6	R	0	VER1	Version ID bit 1
5	R	1	VER0	Version ID bit 0
4	R	-	CCRDO	Closed caption encoding done for odd field
3	R	-	CCRDE	Closed caption encoding done for even field
2		-	Unused	
1	R	-	FSEQ	Field Sequence 1 = During first field of a sequence 0 = Not the first field of a sequence
0	R	-	O_E	Status of the ODD/EVEN flag in the encoder

Registers 0x01 through 0x10 must be initialized to zero.

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x1A			***MSMT***	
7:0	R/W	-	MSMT	Monitor sense mode threshold for DAC's comparator
Offset 0x1B			***MSMS***	
7	R/W	0	MSM	Monitor sense mode 0 = Off 1 = On
6:4		-	Unused	
3	R/W	-	MSMS4	Monitor sense status DAC4 0 = Comparator is inactive. 1 = Comparator is active. *Not present in secondary video channel.
2	R/W	-	MSMS3	Monitor sense status DAC3 0 = Comparator is inactive. 1 = Comparator is active. *Not present in secondary video channel.

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
1	R/W	-	MSMS2	Monitor sense status DAC2 0 = Comparator is inactive. 1 = Comparator is active.
0	R/W	-	MSMS1	Monitor sense status DAC1 0 = Comparator is inactive. 1 = Comparator is active.

Registers 0x1C through 0x25 must be initialized to zero.

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x26			***WSS1***	
7:0	R/W	-	WSSD[7:0]	Wide screen signalling data bits 3:0 = Aspect ratio encoding bits 7:4 = Enhanced services
Offset 0x27			***WSS2***	
7	R/W	0	WSSON	Wide screen signalling enable 0 = wss switched off 1 = wss switched on
6		-	Unused	
5:0	R/W	-	WSSD[13:8]	Wide screen signalling data bits 13:11 = Reserved bits 10:8 = Subtitles
Offset 0x28			***RTC1/BCTL1***	
7	R/W	0	DECFIS	Field sequence detection via RTC 0 = Field sequence as FISE in address 61 1 = Field sequence detection via RTC interface
6	R/W	0	DECCOL	Color detection via RTC interface 0 = Color detection via RTC disabled 1 = Color detection via RTC enabled Note: The RTCE bit must be set to 1 to enable this feature.
5:0	R/W	0x21	BS	Starting point of color burst in clk cycles PAL=0x21 NTSC=0x25
Offset 0x29			***BCTL2***	
7:6		-	Unused	
5:0	R/W	0x1d	BE	Color burst end point in clk cycles PAL = 0x1D NTSC = 0x1D
Offset 0x2A			***CGD1***	
7:0	R/W	-	CG	Copy guard information bits 7:0 Note: The 14 LSBs of the byte carry the information encoded after the run-in. The 6 MSBs have to carry the CRCC bits in accordance with the definition of the CGMS encoding format.
Offset 0x2B			***CGD2***	
7:0	R/W	-	CG	Copy guard information bits 15:8 Note: The 14 LSBs of the byte carry the information encoded after the run-in. The 6 MSBs have to carry the CRCC bits in accordance with the definition of the CGMS encoding format.
Offset 0x2C			***CGD***	
7	R/W	0	CGEN	Copy guard enable 0 = Disabled 1 = Enabled

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
6:4		-	Unused	
3:0	R/W	-	CG	Copy guard information bits 19:16 Note: The 14 LSBs of the byte carry the information encoded after the run-in. The 6 MSBs have to carry the CRCC bits in accordance with the definition of the CGMS encoding format.
Offset 0x2D			***DACCTL Video data path***	
7	R/W	1	VBSEN	DAC3 control 0 = Video dac 3 carries the green channel.. 1 = Video dac 3 carries the luminance channel *Not present in secondary video channel.
6	R/W	1	CVBSEN	DAC1 control 0 = Video dac 1carries the luminance channel. 1 = Video dac 1 carries the CVBS channel.
5	R/W	1	CEN	DAC2 control 0 = Video dac 2 carries the red channel. 1 = Video dac 2 carries the chroma channel. *Not present in secondary video channel.
4:0		-	Unused	

Registers 0x2E—0x37 must be initialized to zero.

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x38			***GAIN_Y - Not present in secondary video channel.***	
7:5		-	Unused	
4:0	R/W	0x1A	GAIN_Y	Gain adjust for Y component in SD-RGB/YUV data path, two's complement number to adjust the gain from -50% to +50% Yout=Yin x (1+ GAIN_Y/32) *Not present in secondary video channel.
Offset 0x39			***GAIN_UV - Not present in secondary video channel.***	
7:5		-	Unused	
4:0	R/W	0x1A	GAIN_UV	Gain adjust for U/V components in SD-RGB/YUV data path, two's complement number to adjust the gain from -50% to +50% UVout=UVin x (1+ GAIN_UV/32) *Not present in secondary video channel.

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x3A			***INPCTL***	
7	R/W	0	CBENB	Color bar generator 0 = Color bar generation switched off 1 = Color bar generation enabled (SD-CVBS/YC modes only)
6	R/W	1	QUALINVERT	0 = Leave the pixel qualifier untouched. 1 = Invert the incoming pixel qualifier. *Not present in secondary video channel.
5	R/W	0	USE_QUAL	Use qualifier enable 0 = No qualifier is used, QUALINVERT should be set. 1 = The HSYNC input is used as slice qualifier in interleaved mode. *Not present in secondary video channel.

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
4	R/W	0	DEDGE	Double edge mode 0 = Double edge mode off; either the interface is running at 2x speed to get interleaved data in or only non-interleaved data streams are accepted. 1 = Input data is latched at positive and negative edge. The SLICE_DIR register determines which data slice goes in which channel.
3	R/W	1	SD_HD	Video mode switch 0 = HD data path in operation; encoder runs idle. 1 = SD data path in operation; encoder is in CVBS/YC or RGB mode *Not present in secondary video channel.
2	R/W	1	U2C	0 = Y/R data channel coming from the D1 interface left unchanged 1 = Y/R MSB of data coming from the D1 interface is inverted.
1	R/W	1	M2C	0 = U/G data channel coming from the D1 interface left unchanged 1 = U/G MSB of data coming from the D1 interface is inverted.
0	R/W	1	L2C	0 = V/B data channel coming from the D1 interface left unchanged 1 = V/B MSB of data coming from the D1 interface is inverted. *Not present in secondary video channel.

Registers 0x3B through 0x53 must be initialized to zero.

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x54			***VPS1***	
7	R/W	0	VPSEN	0 = Video programming system data insertion disabled 1 = Video programming system data insertion enabled
6:0		-	Unused	
Offset 0x55			***VPS2***	
7:0	R/W	-	VPSB5	Fifth byte of video programming system data
Offset 0x56			***VPS3***	
7:0	R/W	-	VPSB11	11th byte of video programming system data
Offset 0x57			***VPS4***	
7:0	R/W	-	VPSB12	12th byte of video programming system data
Offset 0x58			***VPS5***	
7:0	R/W	-	VPSB13	13th byte of video programming system data
Offset 0x59			***VPS6***	
7:0	R/W	-	VPSB14	14th byte of video programming system data
Offset 0x5A			***CHPS***	
7:0	R/W	0x0	CHPS	Phase of encoded color subcarrier (including burst) relative to horizontal sync. Can be adjusted in steps of 360/256 degrees.

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x5B, 0x5D(MSB)			***GAINU***	
7:0	R/W	0x7d	GAINU	Variable gain for Cb signal; input representation is in accordance with CCIR656. White to black = 92.5 IRE GAINU can be adjusted in a range from -2.17 x nominal to 2.16 x nominal GAINU=0 (output subcarrier contribution of U = 0) GAINU=0x76 (output subcarrier contribution of U = nominal) White to black = 100 IRE GAINU can be adjusted in a range from -2.05 x nominal to 2.04 x nominal GAINU=0 (output subcarrier contribution of U = 0) GAINU=0x7D (output subcarrier contribution of U = nominal) GAINU=0x6A (nominal Gain for Secam encoding)
Offset 0x5C, 0x5E(MSB)			***GAINV***	
7:0	R/W	0xaf	GAINV	Variable gain for Cr signal; input representation is in accordance with CCIR656. White to black = 92.5 IRE GAINV can be adjusted in a range from -1.55 x nominal to 1.55 x nominal GAINV=0 (output subcarrier contribution of V = 0) GAINV=0xA5 (output subcarrier contribution of V = nominal) White to black = 100 IRE GAINV can be adjusted in a range from -1.46 x nominal to 1.46 x nominal GAINV=0 (output subcarrier contribution of V = 0) GAINV=0xAF (output subcarrier contribution of V = nominal) GAINV=0x7F (nominal Gain for Secam encoding)
Offset 0x5D			***BLCKL***	
7	R/W	0	GAINU	Bit 8 of register 0x5B
6	R/W	0	DECOE	Odd/even field control via RTC interface 0 = Disabled 1 = Enabled
5:0	R/W	0x33	BLCKL	Variable black level; input representation is in accordance with CCIR656. White to sync = 140 IRE recommended BLCKL=0x3A BLCKL=0 (output black level = 29 IRE) BLCKL=0x3F (output black level = 49 IRE) output black level/IRE=BLCKL x 2/6.29+28.9 White to sync = 143 IRE recommended BLCKL=0x33 BLCKL=0 (output black level = 27 IRE) BLCKL=0x3F (output black level = 47 IRE) output black level/IRE=BLCKL x 2/6.18+26.5
Offset 0x5E			***BLNNL***	
7	R/W	0	GAINV	Bit 8 of register 0x5C
6	R/W	0	DECPH	Subcarrier phase reset control via RTC interface 0 = Disabled 1 = Enabled

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
5:0	R/W	0x35	BLNNL	Variable blanking level White to sync = 140 IRE recommended BLCKL=0x2E BLNNL=0 (output black level = 26 IRE) BLNNL=0x3F (output black level = 46 IRE) output black level/IRE=BLCKL x 2/6.29+25.4 White to sync = 143 IRE recommended BLCKL=0x35 BLNNL=0 (output black level = 26 IRE) BLNNL=0x3F (output black level = 46 IRE) output black level/IRE=BLCKL x 2/6.18+25.9
Offset 0x5F			***BLNVB/CCR***	
7:6	R/W	0x0	CCRS	Cross-color reduction filter settings for luminance path 00 = Cross color reduction filter off 01 = Filter is active; transfer characteristic 1 10 = Filter is active; transfer characteristic 2 11 = Filter is active; transfer characteristic 3
5:0	R/W	0x35	BLNVB	Variable blanking level during vertical blanking interval is typically identical to the value of BLNNL.
Offset 0x60			***must be initialized to zero.***	
Offset 0x61			***STDCTL***	
7:6		-	Unused	
5	R/W	0	INPI	0 = PAL switch phase is nominal. 1 = PAL switch phase is inverted compared to nominal if RTC is enabled.
4	R/W	0	YGS	0 = Luminance gain for white - black 100 IRE 1 = Luminance gain for white - black 92.5 IRE including 7.5 IRE set-up of black
3	R/W	0	SECAM	SECAM enable 0 = Secam encoding switched off 1 = Secam encoding switched on (PAL has to be 0)
2	R/W	1	SCBW	0 = Enlarged bandwidth for chrominance encoding 1 = Standard bandwidth for chrominance encoding
1	R/W	1	PAL	0 = NTSC encoding (non alternating V component) 1 = PAL encoding (alternating V component)
0	R/W	0	FISE	0 = 864 total pixel per line 1 = 858 total pixel per line
Offset 0x62			***RTCCTL/BSTA***	
7	R/W	0	RTCE	0 = No real time control of generated subcarrier frequency 1 = Real time control of generated subcarrier frequency
6:0	R/W	0x2f	BSTA	Amplitude of color burst; input representation is in accordance with CCIR 601 White to black = 92.5 IRE, burst = 40 IRE, NTSC encoding BSTA 0 to 2.02 x nominal recommended value BSTA = 0x3F White to black = 92.5 IRE, burst = 40 IRE, PAL encoding BSTA 0 to 2.82 x nominal recommended value BSTA = 0x2D White to black = 100 IRE, burst = 40 IRE, NTSC encoding BSTA 0 to 1.90 x nominal recommended value BSTA = 0x43 White to black = 92.5 IRE, burst = 40 IRE, PAL encoding BSTA 0 to 3.02 x nominal recommended value BSTA = 0x2F fixed burst amplitude for SECAM encoding

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x63—0x66			***FSC0-FSC3***	
7:0	R/W	0x2A09 8ACB	0x63=FSC0 0x64=FSC1 0x65=FSC2 0x66=FSC3	ffsc: subcarrier frequency (in multiples of line frequency) fllc: clock frequency (in multiples of line frequency) FSC = round ((ffsc/fllc)x2^32) FSC3 most significant byte FSC0 least significant byte NTSC-M: ffsc 227.5, fllc 1716 -> FSC = 21F07C1F PAL-B/G: ffsc 283.7516, fllc 1728 -> FSC = 2A098ACB SECAM: ffsc 274.304, fllc 1728 -> FSC = 28A33BB2
Offset 0x67			***L21O0***	
7:0	R/W	0x0	L21O0	First byte of closed captioning data, odd field
Offset 0x68			***L21O1***	
7:0	R/W	0x0	L21O1	Second byte of closed captioning data, odd field
Offset 0x69			***L21E0***	
7:0	R/W	0x0	L21E0	First byte of closed captioning data, even field
Offset 0x6A			***L21E1***	
7:0	R/W	0x0	L21E1	Second byte of closed captioning data, even field
Offset 0x6B			***must be initialized to zero.***	
Offset 0x6C			***TRGCTL1 - Not present in secondary video channel.***	
7:0	R/W	0x01	HTRIG	Sets horizontal trigger phase related to encoder input. Values above 1715 (FISE=1) or 1727 (FISE=0) are not allowed. Increasing HTRIG decreases delay as of all internally generated timing signals Reference mark: analog output horizontal sync (leading slope) coincides with active edge of RCV used for triggering at HTRIG=0x398.
Offset 0x6D			***TRGCTL2 - Not present in secondary video channel.***	
7:5	R/W	0x1	HTRIG	Sets horizontal trigger phase related to encoder input.
4:0	R/W	0x0	VTRIG	Increasing VTRIG decreases delays of all internally generated timing signals measured in half lines. Variation range of VTRIG = 0 to 0x1F
Offset 0x6E			***MULTICTL***	
7		-	Unused	
6	R/W	0	BLCKON	0 = Encoder in normal operation mode 1 = Output signal is forced to blanking level.
5:4	R/W	0x2	PHRES	Selects the phase reset mode of the color subcarrier. 00 = No phase reset or reset via RTC 01 = Phase reset every two lines 10 = Reset every eight fields 11 = Reset every four fields
3:2	R/W	0x0	LDEL	Selects the luminance delay in reference to the chrominance 00 = No luma delay 01 = 1LLC luma delay 10 = 2LLC luma delay 11 = 3LLC luma delay
1:0	R/W	0x0	FLC	Field length control 00 = Interlaced 312.5 lines/field at 50Hz, 262.5 lines/field at 60Hz 01 = Non interlaced 312 lines @50Hz, 262 lines @60Hz 10 = Non interlaced 313 lines @50Hz, 263 lines @60Hz 11 = Non interlaced 313 lines @50Hz, 263 lines @60Hz

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x6F			***TTXCTL***	
7:6	R/W	0x00	CCEN	Closed caption enable 00 = Line 21 encoding off 01 = Enables encoding in field 1 (odd). 10 = Enables encoding in field 2 (even). 11 = Enables encoding in both fields.
5	R/W	0	TTXEN	0 = Disables teletext insertion. 1 = Enables teletext insertion.
4:0	R/W	0x11	SCCLN	Selects the actual line where closed caption or extended data are encoded. line = (SCCLN + 4) for M-systems line = (SCCLN +1) for other systems
Offset 0x70			***ADWHS***	
7:0	R/W	0x5a	ADWHS7:0	Active Display Window Start bits 7 to 0 Defines the start of the active TV display portion after the border color. Values above 1715 (FISE=1) or 1727 (FISE=0) are not allowed.
Offset 0x71			***ADWHE***	
7:0	R/W	0x5a	ADWHE7:0	Active Display Window End bits 7 to 0 Defines the start of the active TV display portion after the border color. Values above 1715 (FISE=1) or 1727 (FISE=0) are not allowed.
Offset 0x72			***ADWHS/E***	
7		-	Unused	
6:4	R/W	0x6	ADWHE10:8	Active Display Window End bits 10 to 8. Defines the start of the active TV display portion after the border color. Values above 1715 (FISE=1) or 1727 (FISE=0) are not allowed.
3		-	Unused	
2:0	R/W	0x1	ADWHS10:8	Active Display Window Start bits 10 to 8 Defines the start of the active TV display portion after the border color. Values above 1715 (FISE=1) or 1727 (FISE=0) are not allowed.
Offset 0x73			***TTXHS***	
7:0	R/W	0x42	TTXHS	Start of signal on TTXRQ
Offset 0x74			***TTXHL/TTXHD***	
7:4	R/W	0x5	TTXHL	Length of TTXRQ window; only active at old TTX protocol Note: bit TTXO = 1
3:0	R/W	0x2	TTXHD	Indicates the delay in clock cycles between rising edge of TTXRQ output and valid data at pin TTX.
Offset 0x75			***CSYNCA***	
7:3	R/W	0x0	CSYNCA	Advanced composite sync against RGB output, adjustable from 0 XTAL clocks to 31 XTAL clocks
2:0		-	Unused	
Offset 0x76			***TTXOVS***	
7:0	R/W	0x5	TTXOVS	First line of occurrence of ttx data in odd field line = (TTXOVS + 4) for M-systems line = (TTXOVE +1) for other systems PAL: TTXOVS = 0x05 NTSC: TTXOVS = 0x06

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x77			***TTXOVE***	
7:0	R/W	0x16	TTXOVE	Last line of occurrence of ttx data in odd field line = (TTXOVS + 3) for M-systems line = TTXOVE for other systems PAL: TTXOVS = 0x16 NTSC: TTXOVS = 0x10
Offset 0x78			***TTXEVS***	
7:0	R/W	0x4	TTXEVS	First line of occurrence of ttx data in even field line = (TTXOVS + 4) for M-systems line = (TTXOVE + 1) for other systems PAL: TTXOVS = 0x04 NTSC: TTXOVS = 0x05
Offset 0x79			***TTXEVE***	
7:0	R/W	0x16	TTXEVE	Last line of occurrence of ttx data in even field line = (TTXOVS + 3) for M-systems line = TTXOVE for other systems PAL: TTXOVS = 0x16 NTSC: TTXOVS = 0x10
Offset 0x7A			***FAL***	
7:0	R/W	0x24	FAL	First active line = FAL+4 for M-systems and = FAL+1 for other systems. Measured in lines, FAL = 0 coincides with the first field sync pulse.
Offset 0x7B			***LAL***	
7:0	R/W	0x29	LAL	Last active line = LAL+3 for M-systems and = FAL for other systems. Measured in lines, LAL = 0 coincides with the first field sync pulse.
Offset 0x7C			***TTXCTRL***	
7	R/W	0	TTX60	0 = Enables NABTS (FISE=1) or European TTX (FISE=0). 1 = Enables World Standard Teletext 60Hz (FISE=1).
6	R/W	1	LAL8	Bit 8 of LAL
5	R/W	0	TTXO	0 =New TTX protocol selected. At each rising edge of TTXRQ a single TTX bit is requested. 1 = Old TTX protocol selected. The encoder provides a window of TTXRQ. The length of the window depends on the chosen TTX standard.
4	R/W	0	FAL8	Bit 8 of FAL
3	R/W	0	TTXEVE8	Bit 8 of TTXEVE
2	R/W	0	TTXOVE8	Bit 8 of TTXOVE
1	R/W	0	TTXEVS8	Bit 8 of TTXEVS
0	R/W	0	TTXOVS8	Bit 8 of TTXOVS
Offset 0x7D			***Must be initialized to zero.***	
Offset 0x7E			***DTTXL***	
7:0	R/W	0x00	DTTXL	Individual lines in both fields (PAL counting) can be disabled for insertion of teletext by the respective bits. Disabled line =LINExx(50Hz field rate). Bit 7 = Line 12; Bit 0 = Line 5 The mask is only effective if the lines are enabled via TTXOVS/ TTXOVE and TTXEVS/TTXEVE.

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0x7F			***DTTXL2***	
7:0	R/W	0x00	DTTXL	Individual lines in both fields (PAL counting) can be disabled for insertion of teletext by the respective bits. Disabled line = LINExx(50Hz field rate) Bit 7 = Line 20; Bit 0 = Line 13 The mask is only effective if the lines are enabled via TTXOVS/ TTXOVE and TTXEVS/TTXEVE.
Offset 0x80			***LCNT_ARRAY_LINE - Not present in secondary video channel.***	
7:0	R/W	-	LCNT_ARRAY_LINE	Line count array programming data lower 8 bits
Offset 0x81			***LCNT_ARRAY_LINE - Not present in secondary video channel.***	
7:6		-	Unused	
5:0	R/W	-	LCNT_ARRAY_LINE	Line count array programming data upper 6 bit
Offset 0x82			***LCNT_ARRAY_ADR - Not present in secondary video channel.***	
7:4		-	Unused	
3:0	R/W	-	LCNT_ARRAY_ADR	Line count array programming address Writing to this address initiates the transfer of the data previously written into locations 80 and 81 into an internal register array.
Offset 0x83—0x85			***LTYPE_ARRAY_LINE - Not present in secondary video channel.***	
7:0	R/W	-	LTYPE_ARRAY_LINE 0x83 -> LSBs 0x85 -> MSBs	Line type array programming data 2:0 = first index ... 23:21 = last index
Offset 0x86			***LTYPE_ARRAY_ADR - Not present in secondary video channel.***	
7:4		-	Unused	
3:0	R/W	-	LTYPE_ARRAY_ADR	Line type array programming address Writing to this address initiates the transfer of the data previously written into locations 83 through 85 into an internal register array.
Offset 0x87—0x8D			***LPATT_ARRAY_LINE - Not present in secondary video channel.***	
7:0	R/W	-	LPATT_ARRAY_LINE 0x87 -> LSBs 0x8D -> MSBs	Line pattern array programming data 13:4 = first duration 3:0 = first index ... 55:46 = last duration 45:42 last index
Offset 0x8E			***LPATT_ARRAY_ADR - Not present in secondary video channel.***	
7:3		-	Unused	
2:0	R/W	-	LTYPE_ARRAY_ADR	Line pattern array programming address Writing to this address initiates the transfer of the data previously written into locations 87 through 8D into an internal register array.
Offset 0x8F			***must be initialized to zero.***	
Offset 0x90—0x94			***GPIO5-GPIO1 (0x90=GPIO1, ..., 0x94=GPIO5) Not present in secondary video channel.***	
7	R/W	0	GPIO_IN_EN4	GPIO input enable 4
6	R/W	0	GPIO_IN_EN3	GPIO input enable 3
5	R/W	0	GPIO_IN_EN2	GPIO input enable 2
4	R/W	0	GPIO_IN_EN1	GPIO input enable 1
3	R/W	1	OEN	Output enable
2	R/W	0	STATUS	Write to register sets the GPIO pin if output select is set to 2’b11. Read to register returns the status of the gpio pin if GPIO_IN_EN4 is set, otherwise it returns 0.

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
1:0	R/W	0	OUT_SEL	Output selection bits 00 = Selects gpio_out1 01 = Selects gpio_out2 10 = Selects gpio_out3 11 = Read gpio status if GPIO_IN_EN4(bit7) is set.
Offset 0x95			***VMUXCTL***	
7	R/W	1	8/10-BIT	0 = 8-bit mode 1 =10-bit mode
6	R/W	1	SLICE_MODE	0 = Incoming data stream contains a single D1 stream. 1 = Incoming data stream is in sliced mode.
5	R/W	0	SLICE_DIR	De-slicer control determines where the extracted slice goes. 0: incoming slice 1 == outgoing slice 1 incoming slice 2 == outgoing slice 2 1: incoming slice 1 == outgoing slice 2 incoming slice 2 == outgoing slice 1
4:3	R/W	0x0	SEL	Data slice select mode Primary video channel: 00 = Slice 1 primary interface 01 = Slice 2 primary interface 10 = Slice 1 secondary interface 11 = Slice 2 secondary interface Secondary video channel: 00 = Slice 1 secondary interface 01 = Slice 2 secondary interface 10 = Slice 1 primary interface 11 = Slice 2 primary interface
2:0	R/W	0x0	DEMUX_MODE	Output demultiplex mode 000 = yuv422 001 = yuv444 / RGB444 010 = yuvx / RGBx 011 = yuvhd (double interface mode) 100= yuv422hd (single interface mode) All other modes are reserved.
Offset 0x96—0x97			***Must be initialized to zero.***	
Offset 0x98			***VALUE_ARRAY_ADR/EVENT_TYPE_PTR - Not present in secondary video channel.***	
7		-	Unused	
6:4		-	EVENT_TYPE_PTR	HD SYNC generator event type pointer; trigger load value
3		-	Unused	
2:0	R/W	-	VALUE_ARRAY_ADR	Value array programming address Writing to this address initiates the transfer of the data previously written into locations 0xBE through 0xC1 into an internal register array.
Offset 0x99—0x9A			***TRIGGER_LINE - Not present in secondary video channel.***	
7:0	R/W	-	TRIGGER_LINE	This value is used as a line count after trigger. register 0x99 bits 7:0 register 0x9A bits 9:8
Offset 0x9B—0x9C			***TRIGGER_DURATION - Not present in secondary video channel.***	
7:0	R/W	-	TRIGGER_DURATION	This value is used as the duration for a certain value after trigger. register 0x9B bits 7:0 register 0x9C bits 9:8
Offset 0x9D			***TRIGGER_PTR - Not present in secondary video channel.***	
7:4	R/W	-	LCNT_PTR_TRIGGER	This value is used as the line count pointer after trigger.

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
3:2		-	Unused	
1:0	R/W	-	LPATT_PTR_TRIGGER	This value is used as the line pattern pointer after trigger.
Offset 0x9e			***BLANK_Y - Not present in secondary video channel.***	
7:0	R/W	0x90	BLANK_Y	Programmable blank level for the R\Y SD-RGB/YUV channel
Offset 0x9f			***BLANK_UV - Not present in secondary video channel.***	
7:0	R/W	0	BLANK_UV	Programmable blank level for the UV SD-RGB/YUV channel
Offset 0xA0			***RGB_CTRL - Not present in secondary video channel.***	
7:2		-	Unused	
1	R/W	0	DEMOFF	YUV to RGB matrix bypass 0 = matrix enabled 1= matrix bypassed
0		-	Reserved	

Register 0xA1 must be initialized to zero.

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0xA2			***BORDER_Y***	
7:0	R/W	0x80	BORDER_Y	Border color Y component for encoder operation mode
Offset 0xA3			***BORDER_U***	
7:0	R/W	0x80	BORDER_U	Border color U component for encoder operation mode
Offset 0xA4			***BORDER_V***	
7:0	R/W	0x80	BORDER_V	Border color V component for encoder operation mode
Offset 0xA5			***MISCCTRL***	
7		-	Unused	
6	W	0	M24/30	Parallel video input mode select 0=30 bit parallel video input mode 1=24 bit parallel video input mode For details about which pins are used in 24 and 30-bit parallel modes, please refer to section 2 table 5. *Not present in secondary video channel. Always reads back '0'.
5	R/W	1	TRIGGER_MODE	External/embedded trigger selection 0 = External VSYNC/O_E signal triggers the HD-SYNC generator 1 = D1 embedded O_E signal used to trigger the HD-SYNC generator *Not present in secondary video channel.
4	R/W	1	VMODE	HD video data path enable 0 = Video demultiplexer bypassed for incoming 24/30-bit full parallel video streams (DEMUX_MODE settings ignored) 1 = Video demultiplexer enabled for HD signals (DEMUX_MODE settings apply) *Not present in secondary video channel.
3		-	Unused	
2	R/W	0	SLEEP	Video DAC sleep mode powers off all analog circuitry but the band gap reference. primary video channel: DAC1-4 secondary video channel: DAC5-6
1		-	Unused	

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
0	R/W	0	PD	Power down mode for DACs; powers all analog circuitry primary video channel: DAC1-4 secondary video channel: DAC5-6
Offset 0xA6			***HDCTRL - Not present in secondary video channel.***	
7	R/W	0	Y_TOCO	Y Two's complement <-> binary offset conversion 0 = Data at the output of the HD-data path are left unchanged 1 = MSB of data output of the HD-data path is inverted
6	R/W	0	U_TOCO	U Two's complement <-> binary offset conversion 0 = Data at the output of the HD-data path are left unchanged. 1 = MSB of data output of the HD-data path is inverted.
5	R/W	0	V_TOCO	V Two's complement <-> binary offset conversion 0 = Data at the output of the HD-data path are left unchanged. 1 = MSB of data output of the HD-data path is inverted.
4	R/W	0	Y/R_SYNC_INS_EN	Enables insertion of R/Y sync signals into the component signals. 0 = Embedded sync is disabled. 1 = Embedded sync is enabled.
3	R/W	0	U/G_SYNC_INS_EN	Enables insertion of G/U sync signals into the component signals. 0 = Embedded sync is disabled. 1 = Embedded sync is enabled.
2	R/W	0	V/B_SYNC_INS_EN	Enables insertion of B/V sync signals into the component signals. 0 = Embedded sync is disabled. 1 = Embedded sync is enabled.
1	R/W	0	SYNC_SIG_EN	Sync signal insertion enable 0 = No insertion of HD sync module generated sync signals - the external signals are forwarded to the sync pouts. 1 = The insertion of HD sync module generated H-sync, V-sync and Blank signals is enabled. (Note: This disables external sync signals.) • H-sync is derived from sync value[0]. • V-sync is derived from sync value[1]. • C-blank is derived from sync value[2].
0	R/W	0	UPSAMPLE_EN	Enable 422 to 444 upsampling filter 0 = Filter switched into bypass mode 1 = Filter is active.
Offset 0xA6			***DAC6_ADJ - Not present in primary video channel.***	
7:5		-	Unused	
4:0	R/W	0	DAC6_ADJ	DAC6 output level coarse adjustment
Offset 0xA7			***DAC5_ADJ - Not present in primary video channel.***	
7:5		-	Unused	
4:0	R/W	0	DAC5_ADJ	DAC5 output level coarse adjustment
Offset 0xA8			***DACC_ADJ - Not present in primary video channel.***	
7:4		-	Unused	
3:0	R/W	0	DACC_ADJ	DAC5 and 6 output level fine adjustment
Offset 0xA7			***SYNC_DELAY***	
7		0	VBIPROG	0 = Programming via VBI disabled (use this mode for 24-bit parallel mode and any other mode containing non-656 compliant data). 1 = Programming via VBI enabled
6:3		-	Unused	
2:0		1	SYNC_DELAY	Determines the sync-data delay for the incoming data stream and the associated H/V sync and Blank signals. *Not present in secondary video channel.

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0xA8			***BLANK_R/Y - Not present in secondary video channel.***	
7:0		0x0	BLANK_R/Y	Blank offset for the R/Y LSBs
Offset 0xA9			***BLANK_G/U - Not present in secondary video channel.***	
7:0		0x0	BLANK_G/U	Blank offset for the G/U LSBs
Offset 0xAA			***BLANK_B/V - Not present in secondary video channel.***	
7:0		0x0	BLANK_B/V	Blank offset for the B/V LSBs
Offset 0xAE			***SYNC_HEIGHT1 - Not present in secondary video channel.***	
7:0		-	SYNC_HEIGHT1	Sync raster height bits 7:0
Offset 0xAF			***SYNC_HEIGHT2 - Not present in secondary video channel.***	
7:0	R/W	-	SYNC_HEIGHT2	Sync raster height bits 15:8
Offset 0xB0			***SYNC_WIDTH1 - Not present in secondary video channel.***	
7:0	R/W	-	SYNC_WIDTH1	Sync raster width bits 7:0
Offset 0xB1			***SYNC_WIDTH2 - Not present in secondary video channel.***	
7:0	R/W	-	SYNC_WIDTH2	Sync raster width bits 15:8
Offset 0xB2			***SYNC_TRIGPOS_Y1 - Not present in secondary video channel.***	
7:0	R/W	-	SYNC_TRIGPOS_Y1	y trigger position bits 7:0
Offset 0xB3			***SYNC_TRIGPOS_Y2 - Not present in secondary video channel.***	
7:0	R/W	-	SYNC_TRIGPOS_Y2	y trigger position bits 15:8
Offset 0xB4			***SYNC_TRIGPOS_X1 - Not present in secondary video channel.***	
7:0	R/W	-	SYNC_TRIGPOS_X1	x trigger position bits 7:0
Offset 0xB5			***SYNC_TRIGPOS_X2 - Not present in secondary video channel.***	
7:0	R/W	-	SYNC_TRIGPOS_X2	x trigger position bits 15:8
Offset 0xB6			***SIG1- Not present in secondary video channel.***	
7:0	R	-	SIG1	Bit 7:0 primary video path signature
Offset 0xB7			***SIG2- Not present in secondary video channel.***	
7:0	R	-	SIG2	Bit 15:8 primary video path signature
Offset 0xB8			***SIG3- Not present in secondary video channel.***	
7:0	R	-	SIG3	Bit 7:0 secondary video path signature
Offset 0xB9			***SIG4- Not present in secondary video channel.***	
7:0	R		SIG4	Bit 15:8 secondary video path signature
Offset 0xBA			***SIGCTRL- Not present in secondary video channel.***	
7:4	R/W	0x7	SYNC_CTRL	Number of syncs needed to trigger signature analysis [-1]
3	R	-	SIG_DONE	AND combination of signature done for primary and secondary channel
2	R/W	0	SIG_ENABLE	Signature analyzer enable signal 0 = Signature analyzer disabled 1 = Signature analyzer enabled
1:0	R/W	0x0	SIG_SELECT	Video channel select for signature analysis 00 =Video dac 1 and video dac 5 01 =Video dac 2 and video dac 5 10 =Video dac 3 and video dac 6 11 = Video dac 4 and video dac 6
Offset 0xBC			***BLANK_MSBs- Not present in secondary video channel.***	
7:6		-	Unused	
5:4	R/W	-	BLANK_R/Y	Blank offset for the HD-R/Y channel MSBs

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
3:2	R/W	-	BLANK_G/U	Blank offset for the HD-G/U channel MSBs
1:0	R/W	-	BLANK_B/V	Blank offset for the HD-B/V channel MSBs
Offset 0xBE			***R/Y VALUE_ARRAY_LINE - Not present in secondary video channel.***	
7:0	R/W	-	R/Y-VALUE_ARRAY_LINE	R/Y Value array programming data register 0xBE bits 7:0 register 0xC1 bits 9:8
Offset 0xBF			***G/U VALUE_ARRAY_LINE - Not present in secondary video channel.***	
7:0	R/W	-	G/U-VALUE_ARRAY_LINE	G/U Value array programming data register 0xBF bits 7:0 register 0xC1 bits 9:8
Offset 0xC0			***B/V VALUE_ARRAY_LINE - Not present in secondary video channel.***	
7:0	R/W	-	B/V-VALUE_ARRAY_LINE	B/V Value array programming data register 0xC0 bits 7:0 register 0xC1 bits 9:8
Offset 0xC1			***VALUE_ARRAY_LINE-MSBs - Not present in secondary video channel.***	
7:6		-	Unused	
5:4	R/W	-	R/Y-VALUE_ARRAY_LINE	R/Y Value array programming data MSBs
3:2	R/W	-	G/U-VALUE_ARRAY_LINE	G/U Value array programming data MSBs
1:0	R/W	-	B/V-VALUE_ARRAY_LINE	B/V Value array programming data MSBs
Offset 0xC2			***DAC1_ADJ - Not present in secondary video channel.***	
7:5		-	Unused	
4:0	R/W	0	DAC1_ADJ	DAC1 output level coarse adjustment
Offset 0xC3			***DAC2_ADJ - Not present in secondary video channel.***	
7:5		-	Unused	
4:0	R/W	0	DAC2_ADJ	DAC2 output level coarse adjustment
Offset 0xC4			***DAC3_ADJ - Not present in secondary video channel.***	
7:5		-	Unused	
4:0	R/W	0	DAC3_ADJ	DAC3 output level coarse adjustment
Offset 0xC5			***DAC4_ADJ - Not present in secondary video channel.***	
7:5		-	Unused	
4:0	R/W	0	DAC4_ADJ	DAC4 output level coarse adjustment
Offset 0xC6			***DACC_ADJ - Not present in secondary video channel.***	
7:4		-	Unused	
3:0	R/W	0	DACC_ADJ	DAC1 to 4 output level fine adjustment
Offset 0xC7			***HD_GAIN_RY - Not present in secondary video channel.***	
7:0	R/W	0x00	HD_GAIN_R/Y	Gain adjust for R/Y component in HD-RGB/YUV data path, two's complement number to adjust the gain from 1-0.5 to 1+-0.5 out=in x (1+ GAIN/256)
Offset 0xC8			***HD_GAIN_GU - Not present in secondary video channel.***	
7:0	R/W	0x00	HD_GAIN_G/U	Gain adjust for G/U component in HD-RGB/YUV data path, two's complement number to adjust the gain from 1-0.5 to 1+-0.5 out=in x (1+ GAIN/256)
Offset 0xC9			***HD_GAIN_BV - Not present in secondary video channel.***	
7:0	R/W	0x00	HD_GAIN_B/V	Gain adjust for B/Vcomponent in HD-RGB/YUV data path, two's complement number to adjust the gain from 1-0.5 to 1+-0.5 out=in x (1+ GAIN/256)

10. Audio/Clock Address Space

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 0000			***CLK_AUDIO***	
7:1		-	Unused	
0	R/W	0	CLK_AUDIO	0= I^2S is in slave mode. 1= I^2S is in master mode.
Offset 0001			***CLK_IF Video Interface Clock***	
7:5		-	Unused	
4	R/W	0	CLK_IF_DIV8	0 = default (divide by 4). 1 = divide by 8.
3	R/W	0	CLK_IF_DIV6	0 = default (divide by 3). 1 = divide by 6.
2:1	R/W	0x0	CLK_IF_DIV	00= clk_if is input video clock divide by 1 (feed through). 01= clk_if is input video clock divide by 2. 10= clk_if is input video clock divide by 3/6. 11= clk_if is input video clock divide by 4/8.
0	R/W	0	CLK_IF_EN	0 = Normal functional mode 1 = Set the clock to zero.
Offset 0002			***CLK_PROC_DIV Video Processing Clock***	
7:5		-	Unused	
4	R/W	0	CLK_PROC_DIV8	0 = Divide by 4. 1 = Divide by 8.
3	R/W	0	CLK_PROC_DIV6	0 = Default (div.ide by 3). 1 = Divide by 6
2:1	R/W	0x0	CLK_PROC_DIV	00 = clk_proc is input video clock divide by 1 (feed through). 01 = clk_proc is input video clock divide by 2. 10 = clk_proc is input video clock divide by 3/6. 11 = clk_proc is input video clock divide by 4/8.
0	R/W	0	CLK_PROC_EN	0 = Normal functional mode 1 = Set the clock to zero.

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
Offset 00F4			***I2S_SET_REG***	
7:4		-	Unused	
3:0	R/W	0	i2s_format	0000 / Philips I^2S 0001 / LSB justified 16 bits 0010 / LSB justified 18 bits 0011 / LSB justified 20 bits 0100 / MSB 1000 / LSB justified 24 bits All other combinations are reserved for future use.
Offset 00F5(LSBs)—00FB(MSBs) FEATURE_REG				
54:47		-	Unused	
46:39		-	Unused	
38:36		-	Unused	

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
35:33	R/W	0	de-emph_1	De-emphasis Enable the digital de-emphasis filter for this channel. 000 = Other 001 = 32 kHz 010 = 44.1 kHz 011 = 48 kHz 100 = 96 kHz
32		-	Unused	
31	R/W	0	mt1	Mute 0 = Mute off 1 = Mute on
30:29	R/W	0	sound_feature	Controls the mode of the sound processing filters of Bass Boost and Treble. 00 = Flat 01 = Min 10 = Min 11 = Max
28:21	R/W	0	master_vol_right	Master volume control for right channel. Two times this 8-bit value to control the volume attenuation. The range is 0 dB to −∞ dB in steps of 0.25 dB.
20:17	R/W	0	bboost_right	Bass-boost for right channel Result is dependent on the sound_feature setting [30:29]. 20:17 Flat Min Max 0000 0 dB 0 dB 0 dB 0001 0 dB 2 dB 2 dB 0010 0 dB 4 dB 4 dB 0011 0 dB 6 dB 6 dB 0100 0 dB 8 dB 8 dB 0101 0 dB 10 dB 10 dB 0110 0 dB 12 dB 12 dB 0111 0 dB 14 dB 14 dB 1000 0 dB 16 dB 16 dB 1001 0 dB 18 dB 18 dB 1010 0 dB 18 dB 20 dB 1011 0 dB 18 dB 22 dB 1100 0 dB 18 dB 24 dB 1101 0 dB 18 dB 24 dB 1110 0 dB 18 dB 24 dB 1111 0 dB 18 dB 24 dB
16:15	R/W	0	treble_right	Treble for right channel. Result is dependent on the sound_feature setting [30:29]. 16:15 Flat Min Max 00 0 dB 0 dB 0 dB 01 0 dB 2 dB 2 dB 10 0 dB 4 dB 4 dB 11 0 dB 6 dB 6 dB
14:7	R/W	0	master_vol_left	Master volume control for left channel. Two times this 8-bit value to control the volume attenuation. The range is 0 dB to −∞ dB in steps of 0.25 dB.
6:3	R/W	0	bboost_left	Bass-boost for left channel Result is dependent on the sound_feature setting [30:29]. (Refer to bboost_right [20:17] above.)
2:1	R/W	0	treble_left	Treble for left channel. Result is dependent on the sound_feature setting [30:29]. 16:15 Flat Min Max 00 0 dB 0 dB 0 dB 01 0 dB 2 dB 2 dB 10 0 dB 4 dB 4 dB 11 0 dB 6 dB 6 dB

Bits	Read/ Write	Reset Value	Name (Field or Function)	Description
0	R/W	0	mtm	Mute 0 = Mute off 1 = Mute on
Offset 00FC			***INTERPLATOR_REG1***	
7	R/W	0	sdet_on	Silence detect enable 0 = Silence detection circuit disabled 1 = Silence detection circuit enabled
6	R/W	0	silence_override	Silence override 0 = No override. Audio DAC silence switch setting depends on the silence detector circuit and or on the master_mute status. 1 = Override. The Audio DAC silence switch is activated.
5	R/W	0	filter_comp	Switch between ‘flat’ (for the Digital Amplifier) or ‘compensate’ correction filter curve (for the Audio DAC). 0 = Curve for Audio DAC 1 = Curve for Digital Power Amp
4	R/W	0	da_pol_inv	Select the polarity of the DATA to the Audio DAC = a means to control the output signal polarity. The DC and AC dither which must be added to the noise-shaper input will NOT be inverted when inverting the audio data. 0 = Non inverting data out 1 = Inverting data out
3:2	R/W	00	sd_value	The number of ‘zero’ samples counted before the silence detector signals whether there has been digital silence: 00 = 3200 samples 01 = 4800 samples 10 = 9600 samples 11 = 19200 samples
1		-	Unused	
0		-	Unused	
Offset 00FD			***INTERPOLATOR_REG2***	
7:6		-	Unused	
5:4		-	Unused	
3	R/W	0	quickmute	This is an overriding quickmute on the master channel which mutes the interpolator output signal in 32 samples, using the cosine roll-off coefficients. 0 = Quick mute is off 1 = Quick mute on
2	R/W	0	mutemode	Mute function via micro controller interface: 0 = Soft mute mode 1 = Quick mute mode
1		-	Unused	
0		-	Unused	
Offset 00FE			***Audio DAC power on register***	
7:1		-	Unused	
0	R/W	1	pon	1 = Power on for audio DAC 0 = Power off for audio DAC

11. Video Programming Examples

The following listings provide programming examples for setting up a video channel into PAL, NTSC and SECAM modes.

[ANABEL_VIDEO] has to be substituted with the appropriate I^2C base address for the primary or secondary video channel.

[ANABEL_AUDIO] has to be substituted with the appropriate I^2C base address for the primary or secondary audio channel.

Note: The RGB and 1080i examples are only applicable to the primary video channel.

Table 20: ***NTSC Mode (CVBS/YC 27 MHz YUV422 Interface Mode)***

[ANABEL_VIDEO]	
Offset	**Value**
bit 7 of 0x27	0x0
bit 7 of 0x54	0x0
bit 6 of 0x2D	0xe0
0x3A	0x48
bit 7 and 6 of 0x5F	0x0
bit 7 of 0x62	0x0
bit 7 of 0x2C	0x0
bit 7, 6, 5 of 0x6F	0x0
0x95	0x80
0x28	0x25
0x29	0x1d
0x5A	0x88
bit 7 of 0x5D & 0x5B	0x86
bit 7 of 0x5E & 0x5C	0xba
bits [5:0] of 0x5D	0x2a
bits [5:0] of 0x5E	0x2e
bits [5:0] of 0x5F	0x2e
0x61	0x11
0x62	0x45
0x63-0x66	0x21f07c1f
0x6E	0x10
bit 4 of 0x7C & 0x7A	0x000
bit 6 of 0x7C & 0x7B	0x101
bits[2:0] of 0x72 & 0x70	0x102
bits [6:4] of 0x72 & 0x71	0x68c
bits [7:5] of 0x6D & 0x6C	0x0fa
bits [4:0] 0x6D	0x0

Table 21: ***NTSC Mode (CVBS/YC 27 MHz YUV422 Interface Mode)***

[ANABEL_AUDIO]	
Offset	**Value**
0x01	0x0
0x02	0x0

Table 22: ***Pal Mode (CVBS/YC 27 MHz YUV422 Interface Mode)***

[ANABEL_VIDEO]	
Offset	**Value**
bit 7 of 0x27	0x0
bit 7 of 0x54	0x0
bit 6 of 0x2D	0xe0
0x3A	0x48
bit7and 6 of 0x5F	0x0
bit 7 of 0x62	0x0
bit 7 of 0x2C	0x0
bit 7, 6, 5 of 0x6F	0x0
0x95	0x80
0x28	0x21
0x29	0x1d
0x5A	0x0
bit 7 of 0x5D & 0x5B	0x7d
bit 7 of 0x5E & 0x5C	0xaf
bits [5:0] of 0x5D	0x23
bits [5:0] of 0x5E	0x35
bits [5:0] of 0x5F	0x35
0x61	0x02
0x62	0x2f
0x63-0x66	0x2a098acb
0x6E	0x20
bit 4 of 0x7C & 0x7A	0x1b
bit 6 of 0x7C & 0x7B	0x130
bits[2:0] of 0x72 & 0x70	0x160
bits [6:4] of 0x72 & 0x71	0x65a
bits [7:5] of 0x6D & 0x6C	0x107
bits [4:0] 0x6D	0x0

Table 23: ***Pal Mode (CVBS/YC 27 MHz YUV422 Interface Mode)***

[ANABEL_AUDIO]	
Offset	**Value**
0x01	0x0
0x02	0x0

Table 24: ***SECAM (CVBS/YC 27 MHz YUV422 Interface Mode)***

[ANABEL_VIDEO]	
Offset	**Value**
bit 7 of 0x27	0x0
bit 7 of 0x54	0x0
bit 6 of 0x2D	0xe0
0x3A	0x48
bit 7 and 6 of 0x5F	0x0
bit 7 of 0x62	0x0
bit 7 of 0x2C	0x0
bit 7, 6, 5 of 0x6F	0x0
0x95	0x80
0x28	0x21
0x29	0x1d
0x5A	0x0
bit 7 of 0x5D & 0x5B	0x6A
bit 7 of 0x5E & 0x5C	0x7f
bits [5:0] of 0x5D	0x23
bits [5:0] of 0x5E	0x35
bits [5:0] of 0x5F	0x35
0x61	0x0c
0x62	0x2f
0x63-0x66	0x28a33bb2
0x6E	0x10
bit 4 of 0x7C & 0x7A	0x1b
bit 6 of 0x7C & 0x7B	0x130
bits[2:0] of 0x72 & 0x70	0x160
bits [6:4] of 0x72 & 0x71	0x65a
bits [7:5] of 0x6D & 0x6C	0x107
bits [4:0] 0x6D	0x0

Table 25: ***SECAM (CVBS/YC 27 MHz YUV422 Interface Mode)***

[ANABEL_AUDIO]	
Offset	**Value**
0x01	0x0
0x02	0x0

Table 26: ***NTSC (RGB 27 MHz YUV422 Interface Mode)***

[ANABEL_VIDEO]	
Offset	**Value**
0x27	0x0
0x54	0x0
0x2D	0x00
0x3A	0x49
0x2C	0x0
0x6F	0x0
0x95	0x80
0x28	0x1d
0x29	0x25
0x5A	0x88
bit 7 of 0x5D & 0x5B	0x86
bit 7 of 0x5E & 0x5C	0xba
bits [5:0] of 0x5D	0x2a
bits [5:0] of 0x5E	0x2e
bits [5:0] of 0x5F	0x2e
0x61	0x11
0x62	0x45
0x63-0x66	0x21f07c1f
0x6E	0x90
bit 4 of 0x7C & 0x7A	0x000
bit 6 of 0x7C & 0x7B	0x101
bits[2:0] of 0x72 & 0x70	0x102
bits [6:4] of 0x72 & 0x71	0x68c
bits [7:5] of 0x6D & 0x6C	0x0fa
bits [4:0] 0x6D	0x0

Table 27: ***NTSC (RGB 27 MHz YUV422 Interface Mode)***

[ANABEL_AUDIO]	
Offset	**Value**
0x01	0x0
0x02	0x0

Table 28: ***PAL (RGB 27 MHz YUV422 Interface Mode)***

[ANABEL_VIDEO]	
Offset	**Value**
0x27	0x0
0x54	0x0
0x2D	0x00
0x3A	0x49
0x2C	0x0
0x6F	0x0
0x95	0x80
0x28	0x1d
0x29	0x21
0x5A	0x0
bit 7 of 0x5D & 0x5B	0x7d
bit 7 of 0x5E & 0x5C	0xaf
bits [5:0] of 0x5D	0x23
bits [5:0] of 0x5E	0x35
bits [5:0] of 0x5F	0x35
0x61	0x02
0x62	0x2f
0x63-0x66	0x2a098acb
0x6E	0xa0
bit 4 of 0x7C & 0x7A	0x1b
bit 6 of 0x7C & 0x7B	0x130
bits[2:0] of 0x72 & 0x70	0x160
bits [6:4] of 0x72 & 0x71	0x65a
bits [7:5] of 0x6D & 0x6C	0x107
bits [4:0] 0x6D	0x0

Table 29: ***PAL (RGB 27 MHz YUV422 Interface Mode)***

[ANABEL_AUDIO]	
Name	**Value**
0x01	0x0
0x02	0x0

Table 30: ***1080i (74.25 MHz Two Interface 422YUV Mode)***

[ANABEL_VIDEO]	
Offset	**Value**
0x80	0x05
0x81	0x08
0x82	0x00
0x82	0x01
0x80	0x01
0x81	0x10
0x82	0x01
0x82	0x02
0x80	0x0e
0x81	0x18
0x82	0x02
0x82	0x03
0x80	0x19
0x81	0x06
0x82	0x03
0x82	0x04
0x80	0x05
0x81	0x18
0x82	0x04
0x82	0x05
0x80	0x01
0x81	0x14
0x82	0x05
0x82	0x06
0x80	0x04
0x81	0x08
0x82	0x06
0x82	0x07
0x80	0x01
0x81	0x0c

Table 30: ***1080i (74.25 MHz Two Interface 422YUV Mode)*** (Cont'd.)

[ANABEL_VIDEO]	
Offset	**Value**
0x82	0x07
0x82	0x08
0x80	0x0f
0x81	0x18
0x82	0x08
0x82	0x09
0x80	0x19
0x81	0x06
0x82	0x09
0x82	0x0a
0x80	0x05
0x81	0x18
0x82	0x0a
0x82	0x0b
0x80	0x00
0x81	0x00
0x82	0x0b
0x82	0x0c
0x80	0x00
0x81	0x00
0x82	0x0c
0x82	0x0d
0x80	0x00
0x81	0x00
0x82	0x0d
0x82	0x0e
0x80	0x00
0x81	0x00
0x82	0x0e
0x82	0x0f
0x83	0x1c
0x84	0x00
0x85	0x00
0x86	0x00
0x86	0x01
0x83	0x14
0x84	0x05
0x85	0x00

Table 30: ***1080i (74.25 MHz Two Interface 422YUV Mode)*** (Cont'd.)

[ANABEL_VIDEO]	
Offset	**Value**
0x86	0x01
0x86	0x02
0x83	0x14
0x84	0x03
0x85	0x00
0x86	0x02
0x86	0x03
0x83	0x0c
0x84	0x03
0x85	0x00
0x86	0x03
0x86	0x04
0x83	0x0c
0x84	0x05
0x85	0x00
0x86	0x04
0x86	0x05
0x83	0x2c
0x84	0x00
0x85	0x00
0x86	0x05
0x86	0x06
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x06
0x86	0x07
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x07
0x86	0x08
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x08
0x86	0x09
0x83	0x00

Table 30: ***1080i (74.25 MHz Two Interface 422YUV Mode)*** (Cont'd.)

[ANABEL_VIDEO]	
Offset	**Value**
0x84	0x00
0x85	0x00
0x86	0x09
0x86	0x0a
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x0a
0x86	0x0b
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x0b
0x86	0x0c
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x0c
0x86	0x0d
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x0d
0x86	0x0e
0x87	0xfb
0x88	0xf6
0x89	0xae
0x8a	0x00
0x8b	0x00
0x8c	0x00
0x8d	0x00
0x8e	0x00
0x8e	0x01
0x87	0xf8
0x88	0xf6
0x89	0xae
0x8a	0x00
0x8b	0x00

Table 30: ***1080i (74.25 MHz Two Interface 422YUV Mode)*** (Cont'd.)

[ANABEL_VIDEO]	
Offset	**Value**
0x8c	0x00
0x8d	0x00
0x8e	0x01
0x8e	0x02
0x87	0xbb
0x88	0x83
0x89	0xfd
0x8a	0x6e
0x8b	0xbf
0x8c	0xef
0x8d	0x0a
0x8e	0x02
0x8e	0x03
0x87	0xb9
0x88	0x82
0x89	0xae
0x8a	0xb0
0x8b	0x57
0x8c	0x00
0x8d	0x00
0x8e	0x03
0x8e	0x04
0x87	0xbb
0x88	0xc3
0x89	0xfe
0x8a	0xbe
0x8b	0xbf
0x8c	0xef
0x8d	0x0a
0x8e	0x04
0x8e	0x05
0xbe	0x00
0xbf	0x9c
0xc0	0x6a
0xc1	0x2f
0x98	0x00
0x98	0x01
0xbe	0x00

Table 30: ***1080i (74.25 MHz Two Interface 422YUV Mode)*** (Cont'd.)

[ANABEL_VIDEO]	
Offset	**Value**
0xbf	0x9c
0xc0	0x6a
0xc1	0x2f
0x98	0x01
0x98	0x02
0xbe	0x66
0xbf	0x64
0xc0	0x78
0xc1	0x00
0x98	0x02
0x98	0x03
0xbe	0x33
0xbf	0xd4
0xc0	0xc0
0xc1	0x3a
0x98	0x03
0x98	0x04
0xbe	0x00
0xbf	0x00
0xc0	0x00
0xc1	0x00
0x98	0x04
0x98	0x05
0xbe	0x00
0xbf	0x00
0xc0	0x00
0xc1	0x00
0x98	0x05
0x98	0x06
0xbe	0xf6
0xbf	0x14
0xc0	0x23
0xc1	0x30
0x98	0x06
0x98	0x07
0x99	0x03
0x9a	0x00
0x9c	0x00

Table 30: ***1080i (74.25 MHz Two Interface 422YUV Mode)*** (Cont'd.)

[ANABEL_VIDEO]	
Offset	**Value**
0x9b	0x02
0x9d	0x11
0xae	0x64
0xaf	0x04
0xb0	0x97
0xb1	0x08
0xb4	0x15
0xb5	0x00
0xb2	0x15
0xb3	0x00

Table 31: ***1080i (74.25 MHz Two Interface 422YUV Mode)***

[ANABEL_AUDIO]	
Offset	**Value**
0x01	0x0
0x02	0x0

Table 32: ***720p (74.25 MHz Two Interface 422YUV Mode)***

[ANABEL_VIDEO]	
Offset	**Value**
0x80	0x05
0x81	0x08
0x82	0x00
0x82	0x01
0x80	0x14
0x81	0x0c
0x82	0x01
0x82	0x02
0x80	0x68
0x81	0x05
0x82	0x02
0x82	0x03
0x80	0x68
0x81	0x05
0x82	0x03
0x82	0x04
0x80	0x05

Table 32: ***720p (74.25 MHz Two Interface 422YUV Mode)*** (Cont'd.)

[ANABEL_VIDEO]	
Offset	**Value**
0x81	0x0c
0x82	0x04
0x82	0x05
0x80	0x00
0x81	0x00
0x82	0x05
0x82	0x06
0x80	0x00
0x81	0x00
0x82	0x06
0x82	0x07
0x80	0x00
0x81	0x00
0x82	0x07
0x82	0x08
0x80	0x00
0x81	0x00
0x82	0x08
0x82	0x09
0x80	0x00
0x81	0x00
0x82	0x09
0x82	0x0a
0x83	0x1c
0x84	0x00
0x85	0x00
0x86	0x00
0x86	0x01
0x83	0x14
0x84	0x00
0x85	0x00
0x86	0x01
0x86	0x02
0x83	0x2c
0x84	0x00
0x85	0x00
0x86	0x02
0x86	0x03

Table 32: ***720p (74.25 MHz Two Interface 422YUV Mode)*** (Cont'd.)

[ANABEL_VIDEO]	
Offset	**Value**
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x03
0x86	0x04
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x04
0x86	0x05
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x05
0x86	0x06
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x06
0x86	0x07
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x07
0x86	0x08
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x08
0x86	0x09
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x09
0x86	0x0a
0x83	0x00
0x84	0x00
0x85	0x00

Table 32: ***720p (74.25 MHz Two Interface 422YUV Mode)*** (Cont'd.)

[ANABEL_VIDEO]	
Offset	**Value**
0x86	0x0a
0x86	0x0b
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x0b
0x86	0x0c
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x0c
0x86	0x0d
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x0d
0x86	0x0e
0x87	0x00
0x88	0x00
0x89	0x00
0x8a	0x00
0x8b	0x00
0x8c	0x00
0x8d	0x00
0x8e	0x00
0x8e	0x01
0x87	0xa8
0x88	0x2c
0x89	0x2a
0x8a	0xbb
0x8b	0x45
0x8c	0x00
0x8d	0x00
0x8e	0x01
0x8e	0x02
0x87	0x5b
0x88	0x09
0x89	0xfc

Table 32: ***720p (74.25 MHz Two Interface 422YUV Mode)*** (Cont'd.)

[ANABEL_VIDEO]	
Offset	**Value**
0x8a	0x09
0x8b	0x7f
0x8c	0x6e
0x8d	0x11
0x8e	0x02
0x8e	0x03
0x87	0x79
0x88	0x82
0x89	0x9e
0x8a	0xb0
0x8b	0x45
0x8c	0x00
0x8d	0x00
0x8e	0x03
0x8e	0x04
0x87	0x5b
0x88	0xc9
0x89	0xfe
0x8a	0xb9
0x8b	0x7f
0x8c	0x6e
0x8d	0x11
0x8e	0x04
0x8e	0x05
0x87	0x00
0x88	0x00
0x89	0x00
0x8a	0x00
0x8b	0x00
0x8c	0x00
0x8d	0x00
0x8e	0x05
0x8e	0x06
0x87	0x00
0x88	0x00
0x89	0x00
0x8a	0x00
0x8b	0x00

Table 32: ***720p (74.25 MHz Two Interface 422YUV Mode)*** (Cont'd.)

[ANABEL_VIDEO]	
Offset	**Value**
0x8c	0x00
0x8d	0x00
0x8e	0x06
0x8e	0x07
0xbe	0x00
0xbf	0x00
0xc0	0x00
0xc1	0x20
0x98	0x00
0x98	0x01
0xbe	0x00
0xbf	0x00
0xc0	0x00
0xc1	0x20
0x98	0x01
0x98	0x02
0xbe	0xff
0xbf	0x00
0xc0	0x00
0xc1	0x10
0x98	0x02
0x98	0x03
0xbe	0x56
0xbf	0x00
0xc0	0x00
0xc1	0x30
0x98	0x03
0x98	0x04
0xbe	0x00
0xbf	0x00
0xc0	0x00
0xc1	0x00
0x98	0x04
0x98	0x05
0xbe	0x00
0xbf	0x00
0xc0	0x00
0xc1	0x00

Table 32: ***720p (74.25 MHz Two Interface 422YUV Mode)*** (Cont'd.)

[ANABEL_VIDEO]	
Offset	**Value**
0x98	0x05
0x98	0x06
0xbe	0x00
0xbf	0x00
0xc0	0x00
0xc1	0x00
0x98	0x06
0x98	0x07
0x99	0x03
0x9a	0x00
0x9c	0x00
0x9b	0x02
0x9d	0x11
0xa8	0x80
0xa9	0x00
0xaa	0x00
0xae	0xed
0xaf	0x02
0xb0	0x71
0xb1	0x06
0xb4	0x20
0xb5	0x70
0xb	0x10
0xb3	0x70

Table 33: ***720p (74.25 MHz Two Interface 422YUV Mode)***

[ANABEL_AUDIO]	
Offset	**Value**
0x01	0x0
0x02	0x0

12. Physical and Electrical Characteristics

12.1 PNX8510/11 Signal Descriptions

Table 34: Signal Descriptions (by Pin No.)

Pin No.	Name	Description
1	AVDDA1	Audio DAC analog supply
2	AVSS1	Audio DAC analog ground
3	TRST	JTAG reset
4	RESETN	Chip reset in signal (low active)
5	SUB	Audio digital ground
6	SUB	Audio digital ground
7	AVDDD	Audio DAC digital supply
8	BONDDOWN	Digital ground
9	TDI	JTAG controller test data input
10	TDO	JTAG controller test data output
11	TCK	JTAG controller test clock input
12	TMS	JTAG controller test mode select input
13	VSS	Digital ground
14	VDD	Digital supply
15	I2S_IN2_SCK	Bit clock IO for secondary audio channel
16	I2S_IN2_WS	Word select IO for secondary audio channel
17	I2S_IN2_SD	Serial data in for secondary audio channel
18	BONDDOWN	Digital ground
19	I2S_AOS2_CLK	Oversampling clock input for secondary audio channel
20	I2S_IN1_SCK	Bit clock IO for primary audio channel
21	I2S_IN1_WS	Word select IO for primary audio channel
22	I2S_IN1_SD	Serial data in for primary audio channel
23	I2S_AOS1_CLK	Oversampling clock input for primary audio channel
24	VSSI	Digital ground
25	VDDI	Digital supply
26	I2C_SDA	I^2C data line (bi-directional)
27	I2C_SCL	I^2C clock line (input)
28	VSYNC_IN	Vertical sync input for primary video interface
29	HSYNC_IN	Horizontal sync input for primary video interface
30	BLANK_IN	Blanking input signal for primary video pipeline
31	VSSE1	Digital ground
32	VSYNC_OUT	Vertical sync output for primary video pipeline
33	HSYNC_OUT	Horizontal sync output for primary video pipeline
34	VDDE	Digital supply
35	VSS	Digital ground

Table 34: Signal Descriptions (by Pin No.) (Cont'd.)

Pin No.	Name	Description
36	VDD	Digital supply
37	VAVDD2_2	Analog supply for video DACs
38	VOUT5	Video output for secondary channel, Y/CVBS-DAC
39	IDUMP2	Current return path for C-DAC and CVBS/Y-DAC
40	VOUT6	Video output for secondary channel, C-DAC
41	RSET2	Current setting resistor for secondary channel DACs
42	VAVSS2	Analog ground for video DACs
43	VAVDD2_1	Analog supply for video DACs
44	VOUT1	Video output for primary video DAC 1 (CVBS/Y)
45	VAVDD1	Analog supply for video DACs
46	VOUT4	Video output for primary video DAC 4 (Blue)
47	VOUT3	Video output for primary video DAC 3 (Y/Green)
48	IDUMP1	Current return path for all primary channel DACs
49	VOUT2	Video output for primary video DAC 2 (C/Red)
50	VAVDD1	Analog supply for video DACs
51	RSET1	Current setting resistor for primary channel DACs
52	VREF1	No connection (leave floating)
53	VAVSS1	Analog ground for video DACs
54	VSS	Digital ground
55	VDD	Digital supply
56	DV_CLK1	Primary video interface clock
57	DV9_IN1	Primary video D1 input
58	DV8_IN1	Primary video D1 input
59	DV7_IN1	Primary video D1 input
60	DV6_IN1	Primary video D1 input
61	DV5_IN1	Primary video D1 input
62	DV4_IN1	Primary video D1 input
63	DV3_IN1	Primary video D1 input
64	DV2_IN1	Primary video D1 input
65	DV1_IN1	Primary video D1 input
66	DV0_IN1	Primary video D1 input
67	VSS	Digital ground
68	VDD	Digital supply
69	DV_CLK2	Secondary video interface clock
70	DV9_IN2	Secondary video D1 input
71	DV8_IN2	Secondary video D1 input
72	DV7_IN2	Secondary video D1 input
73	DV6_IN2	Secondary video D1 input
74	DV5_IN2	Secondary video D1 input

Table 34: Signal Descriptions (by Pin No.) (Cont'd.)

Pin No.	Name	Description
75	DV4_IN2	Secondary video D1 input
76	DV3_IN2	Secondary video D1 input
77	DV2_IN2	Secondary video D1 input
78	DV1_IN2	Secondary video D1 input
79	DV0_IN2	Secondary video D1 input
80	VSSI	Digital ground
81	VDDI	Digital supply
82	VSS	Digital ground
83	VDD	Digital supply
84	GPIO[0]	General purpose input/output
85	GPIO[1]	General purpose input/output
86	GPIO[2]	General purpose input/output
87	GPIO[3]	General purpose input/output
88	GPIO[4]	General purpose input/output
89	AVSS2	Audio DAC output buffer supply
90	AVDDA2	Audio DAC supply
91	AOUT_R2	Audio output for right secondary audio channel
92	AVSSA2	Audio DAC ground
93	AVREF2	Audio DAC reference
94	AVDDO2	Audio DAC output buffer supply
95	AOUT_L2	Audio output for left secondary audio channel
96	AOUT_R1	Audio output for right primary audio channel
97	AVREF1	Audio DAC reference
98	AVDDO1	Audio DAC output buffer supply
99	AVSSA1	Audio DAC ground
100	AOUT_L1	Audio output for left primary audio channel

12.2 Electrical Characteristics

Range: VDD = 3.0 to 3.6 V; Tamb = 0 to +70°C

Note: For Table 35, VDD = 3.3; Tamb = 25°C, unless otherwise stated.

Table 35: Electrical Specifications

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
Power Consumption						
SD[1]		RGB/Y-C		1.02	1.15	W
Half HD[1]		YPrPb		1.09	1.26	W
Full HD[1]		YPrPb		1.58	1.97	W
Supply						
VAVDD	Digital supply audio		3.0	3.3	3.6	V

Table 35: Electrical Specifications (Cont'd.)

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
VDVDD	Digital supply video		3.0	3.3	3.6	V
AVDDD	Analog supply video		3.15	3.3	3.45	V
AVDDA	Analog supply audio		3.15	3.3	3.45	V
Inputs						
VIL	Low level input voltage		-0.5		+0.8	V
VIH	High level input voltage		2.0		VDD+0.3	V
ILI	Input leakage current		-		1	uA
Ci	Input capacitance	clocks			10	pF
		data			8	pF
		I/Os at high impedance			8	pF
Outputs						
VOL	Low level output voltage	IOL=2mA	-		0.4	V
VOH	High level input voltage	IOH=2mA	2.4		-	V
I^2S bus; SDA, SCL						
VIL	Low level output voltage		-0.5		+0.3	V
VIH	High level input voltage		0.7		VDD+0.3	V
Ii	Input current	Vi=low or high	-10		+10	mA
VOL	Low level output voltage (SDA)	Iol=3mA	-		0.4	V
Io	Output current	during ACK	3		-	mA
Input Timing						
tsu	Input data setup time		TBD			ns
thd	Input data hold time		TBD			ns
Data and Reference Signal Output Timing						
CL	Output load cap.		TBD		TBD	pf
th	Output hold time		TBD			ns
td	Output delay				TBD	ns
Audio DAC Outputs						
V_{out}	Full scale output voltage[2]			1.0		V_{rms}
V_{com}	Common mode output voltage[3]			1.65		V
R_{load}	Load resistance		4			kΩ
R_{out}, V_{ref}	Equivalent AC resistance seen at VREF terminal			25		kΩ
(THD+N)/S	(THD+N)/S @ 0dB, 1 kHz			-90		dB
	(THD+N)/S @ -60dB, 1 kHz			-40		dB(A)
S/N	SNR at digital silence			90		dB(A)
	SNR at digital silence			95		dB(A)

Table 35: Electrical Specifications (Cont'd.)

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
DC Offset Characteristics						
V_{offset}	DC-offset compensation			-43		mV
Video DAC Outputs						
INL	Integral nonlinearity	Static	±0.6			lsb
DN			±0.5			lsb
	Output rise time	Load 37.5 Ω //15pF	2.3			ns
	Output fall time	Load 37.5 Ω //15pF	2.3			ns
	Clock frequency				200	MHz
I_{out}	Output current programming	See Section 12.3 for application information.				
Vref				1.23		V
	Output load			0.35		V
	Detection threshold (comparator)				100	ns
	Operating to sleep delay				200	ns
	Operating to power down delay				200	ns
	Sleep to power down delay				200	ns
	Sleep to operating				200	ns
	Power delay				200	ns
	Power down to operating delay				200	ns
	Power down to sleep delay				200	ns

Notes:
[1] Requires proper assembly of package to heat spreader. See Figure 29 Footprint for heat spreader requirements and Section 14.4 for soldering and footprint requirements.
[2] Full scale output voltage is directly proportional to DC voltage at VREF pin (VDDA/2) and maximum digital signal level at low frequencies. Relation: Vout(rms) = α * 1.645 * vref/1.41, α = maximum digital input level at low frequencies.
[3] Common mode output voltage equals VREF=VDDA/2/.

12.3 Application Information

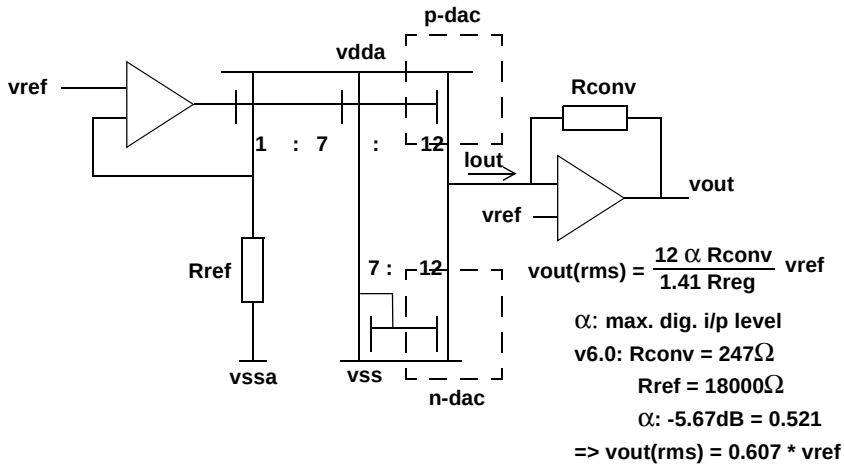


Figure 25: Simplified Schematic of Audio DAC

From the simplified schematic of the DAC in Figure 25 it can be seen that the output voltage swing depends upon:

- the maximum digital input level at low frequencies (α)
- the reference voltage vref (nominal VDDA/2)
- the current mirror gain (ideally 12)
- the ratio of the I/V conversion resistance (Rconv) and the reference resistance (Rref)

This relationship is:

$$Vout(rms) = 12 \cdot \alpha/\sqrt{2} \cdot Rconv/Rref \cdot Vref$$

The reference resistor is dimensioned to be 18kΩ. Since the reference voltage Vref is nominally half the supply voltage, the I/V conversion resistor must be dimensioned by:

$$Rconv = Vout(rms)/Vref \cdot \sqrt{2}/(12 \cdot \alpha) \cdot Rref$$

For an rms output voltage of 1000mVrms, a reference voltage of 1.65V, a reference resistance of 18 kΩ and a maximum digital input level of 0.521 (-5.67dB), the I/V conversion resistor should be 2470 Ω.

Figure 26 shows the circuitry for the reconstruction filter of the video D/A converters.

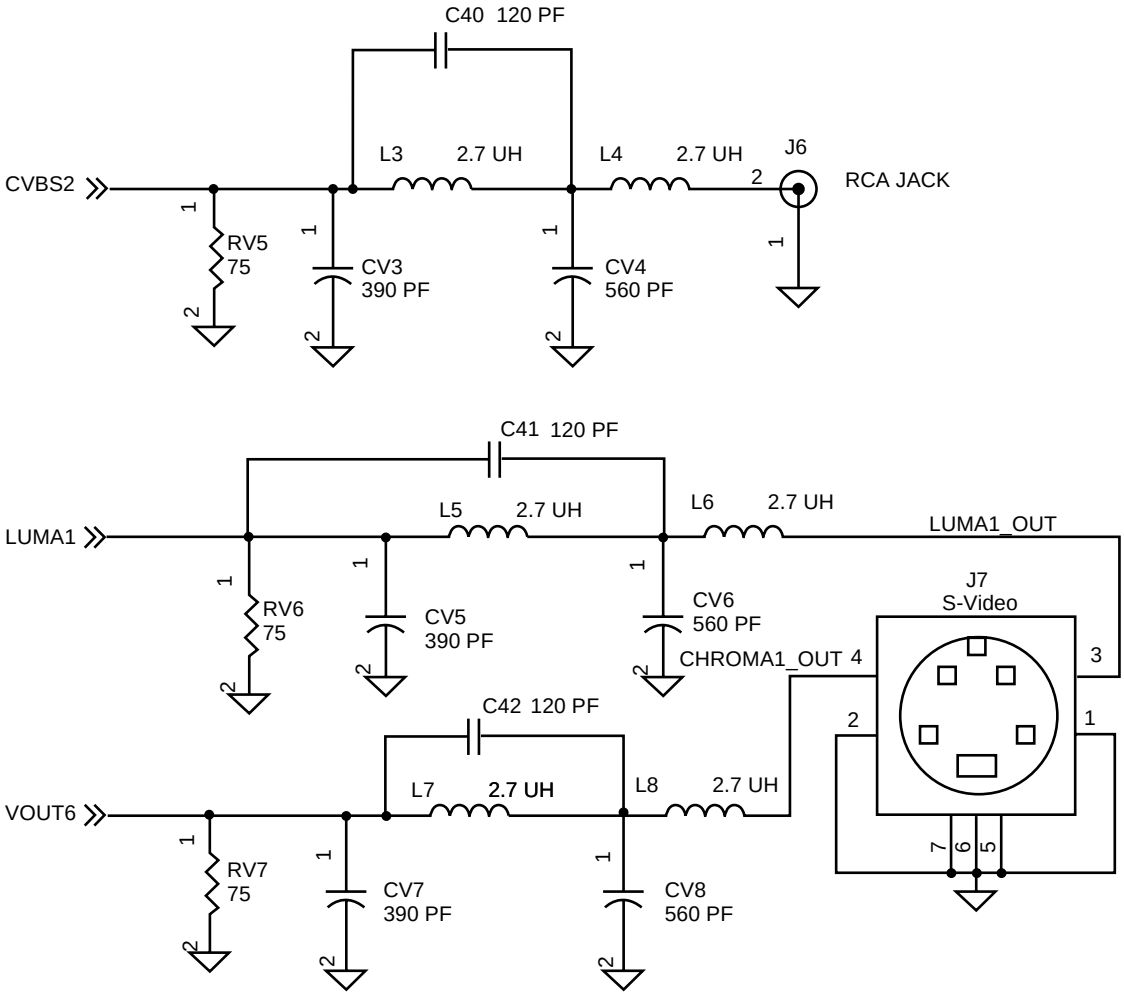


Figure 26: DAC Reconstruction Filter Circuitry

12.3.1 Video DACs of Primary and Secondary Video Channels

The video DACs used in both the primary and secondary video channels employ segmented current mode architecture. The programming feature of DACs is valid for both the primary and secondary video channels.

The primary video channel has in its path four DACs: R, G, B and CVBS. The programming option “Fine Adjust” — via the common four bits of I^2C [3:0] — can simultaneously adjust the central output level of all four DACs in a range of ± 7% in 1% increments. Please note the four bits are signed values. The following table shows the programming values.

Table 36: Common I^2C Bits for all DACs (Output Level: Fine Adjustment in 1% Increments)

B03	B02	B01	B00	Vout
0	0	0	0	0%
0	0	0	1	+1%
0	0	1	0	+2%
0	0	1	1	+3%

Table 36: Common I²C Bits for all DACs (Output Level: Fine Adjustment in 1% Increments)

B03	B02	B01	B00	Vout
0	1	0	0	+4%
0	1	0	1	+5%
0	1	1	0	+6%
0	1	1	1	+7%
1	0	0	0	0%
1	0	0	1	-1%
1	0	1	0	-2%
1	0	1	1	-3%
1	1	0	0	-4%
1	1	0	1	-5%
1	1	1	0	-6%
1	1	1	1	-7%

The programming option “Coarse Adjust” uses five separate bits [14:10] of I²C to independently adjust the output level of each R, G, B and CVBS DAC between 0.58V and 1.23V (in increments of 21mV, assuming an effective load of 75 // 75 = 37.5 Ω). Note that these five bits are not signed.

Table 37: Separate I²C Bits 31x21mV (Output Level: Coarse Adjustment for each DAC)

Bit Values					Vout
0	0	0	0	0	0%
0	0	0	0	1	+3.6%
0	0	0	1	0	+7.2%
0	0	0	1	1	+10.7%
0	0	1	0	0	+14.3%
0	0	1	0	1	+17.9%
0	0	1	1	0	+21.5%
0	0	1	1	1	+25.0%
0	1	0	0	0	+28.6%
0	1	0	0	1	+32.2%
0	1	0	1	0	+35.8%
0	1	0	1	1	+39.4%
0	1	1	0	0	+42.9%
0	1	1	0	1	+46.5%
0	1	1	1	0	+50.1%
0	1	1	1	1	+53.7%
1	0	0	0	0	+57.3%
1	0	0	0	1	+60.8%
1	0	0	1	0	+64.4%
1	0	0	1	1	+68%
1	0	1	0	0	+71.6%

Table 37: Separate I²C Bits 31x21mV (Output Level: Coarse Adjustment for each DAC)

Bit Values					Vout
1	0	1	0	1	+75.1%
1	0	1	1	0	+78.7%
1	0	1	1	1	+82.3%
1	1	0	0	0	+85.9%
1	1	0	0	1	+89.5%
1	1	0	1	0	+93.0%
1	1	0	1	1	+96.6%
1	1	1	0	0	+100.2%
1	1	1	0	1	+103.8%
1	1	1	1	0	+107.4%
1	1	1	1	1	+110.9%

Programming Examples

Assuming an effective load of 75 // 75 = 37.5 Ω, Rset = 1kΩ, the coarse bits are set to 0 0 0 0 and the fine adjust bits are set to 0 0 0 0 0. The output will be sitting at the minimum level of Vout = 0.579V.

For example, if Vout is set to 1 V, then the fine adjust bits should be set to 0 0 0 0 0 and the coarse adjust bits set to 1 0 1 0 0.

Sleep and Powerdown Modes

- Sleep mode occurs when all current output switches are disabled asynchronously so that no current flows in either Iout or Idump pins i.e., IOUT = IDUMP = 0. Sleep mode allows a rapid recovery from a low power consumption state. Each DAC can be put into sleep mode asynchronously where IOUT = IDUMP = 0, yet still supply current flows to power the bandgap, opmap, and other analog DAC components, including the digital logic.
- Powerdown mode occurs when each DAC can be asynchronously put into zero state current so that all current output switches are disabled. This includes current to all analog and digital components of the DAC such as bandgap reference, opmaps, etc. In this mode IDDD = IDDA = 0.

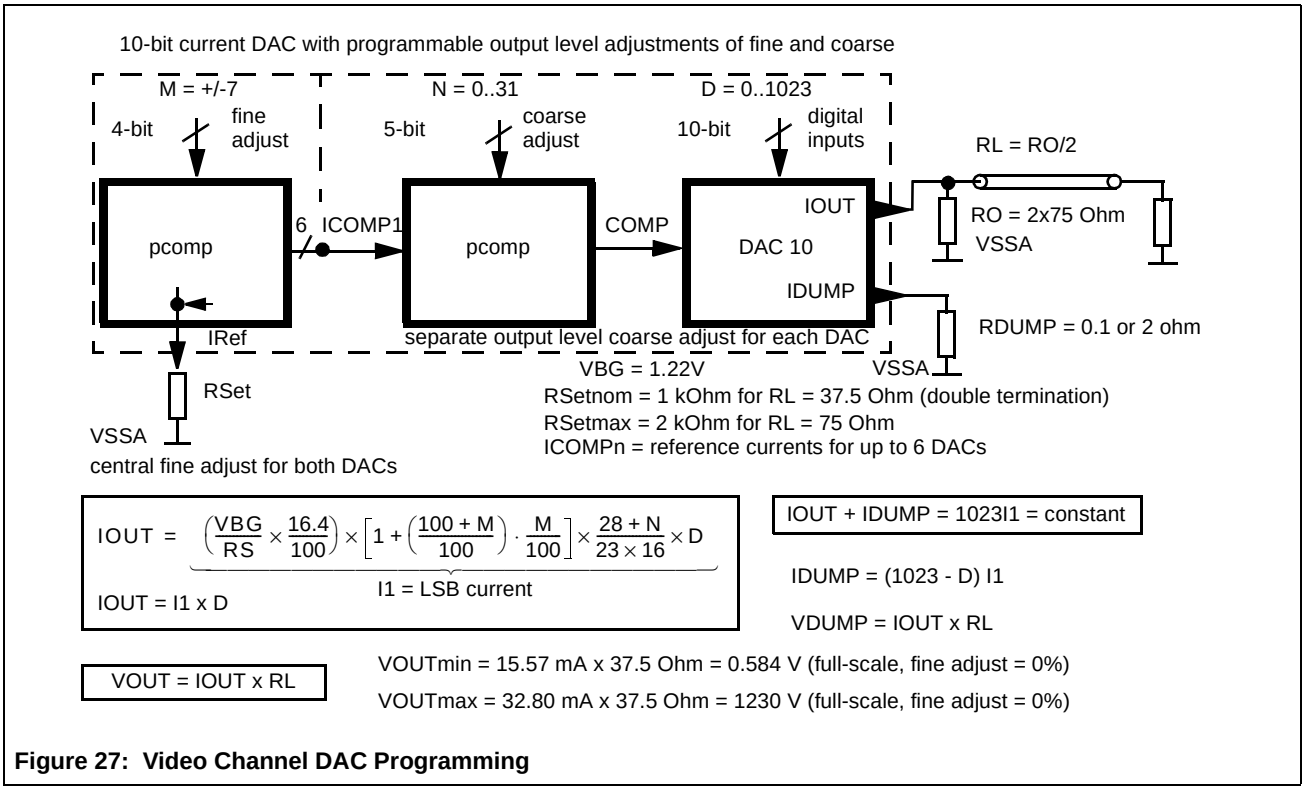


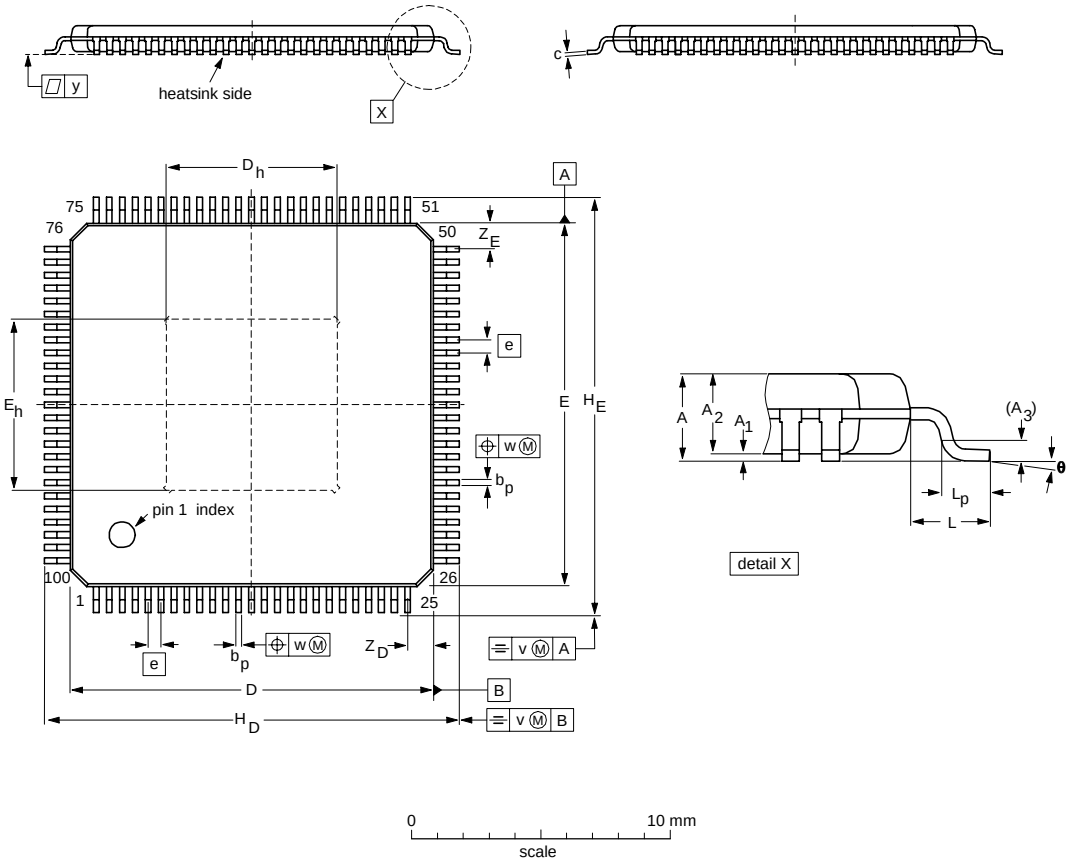
Figure 27: Video Channel DAC Programming

Figure 27 provides an example for calculating the RSet for the video DACs from given output voltage and termination.

13. Package Description

Figure 28 illustrates the 100-pin HTQFP package showing the dimensions in millimeters

HTQFP100: plastic, heatsink thin quad flat package; 100 leads; body 14 x 14 x 1.0 mm **SOT638-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	14.1 13.9	7.1 6.1	14.1 13.9	7.1 6.1	0.5	16.15 15.85	16.15 15.85	1.0	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT638-1						01-03-30

Figure 28: Package Diagram

14. Soldering

14.1 Introduction to Soldering Surface-Mount Packages

The following information provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in the Philips' *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface-mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

For the PNX8510/11 only reflow soldering is suitable.

14.2 Reflow Soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250° C. The top-surface temperature of the packages should preferably be kept below 220° C for thick/large packages, and below 235° C for small/thin packages.

14.3 Manual Soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300° C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320° C.

14.4 Footprint

For good thermal behavior of the PNX8510/11 in the application, the exposed pad needs to be soldered to the motherboard. Figure 29 shows the recommended footprint and solderpaste placement. A matrix of solderpaste dots has to be placed on a copper square. For optimal heat dissipation through the motherboard, the recommendation is to connect the copper square with vias to the inner-ground plane of the application board.

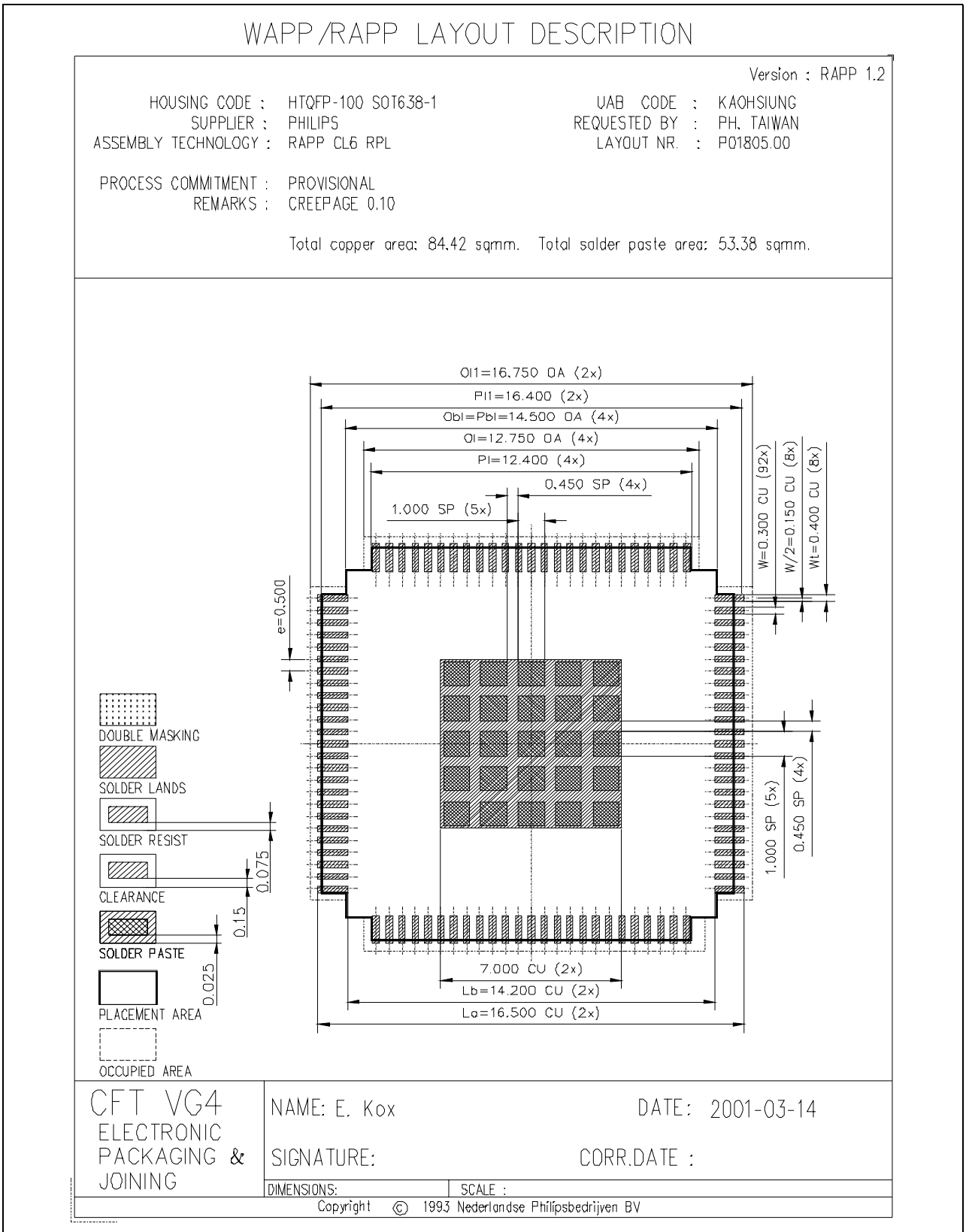


Figure 29: Footprint

15. Ordering Information

Type Number	Package		
	12NC	Name	Version
PNX8510HW/B1	9352 695 80557	HTQFP100	SOT638-1
PNX8511HW/B1	9352 695 76557	HTQFP100	SOT638-1

16. Revision History

Table 38: Revision History

Rev	Date	CPCN	Description
02	20010924	853-2300 27221	Upgraded to product data. Supersedes initial version of 27 August 2001 (9397 750 08495). Modifications: • The format of this document has been redesigned to comply with Philips Semiconductors' new presentation and information standard.
01	20010827		Preliminary release posted on BHS (DVI) Intranet web site

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Data Sheet Status[1]	Product Status[2]	Definitions
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