PRERELEASE

LTC2400

24-Bit µPower ΔΣ ADC in SO-8

November 1998

FEATURES

- 24-Bit ADC in SO-8 Package
- 4ppm INL, No Missing Codes
- 4ppm Full-Scale Error
- 0.5ppm Offset
- 0.3ppm Noise
- Internal Oscillator—No External Components Required
- 110dB Min, 50Hz/60Hz Notch Filter
- Single Conversion Settling Time for Multiplexed Applications
- Reference Input Voltage: 0.1V to 0.9 × V_{CC}
- Live Zero—Extended Input Range Accommodates 12.5% Overrange and Underrange
- Single Supply 2.7V to 5.5V Operation
- Low Supply Current (200µA) and Auto Shutdown

APPLICATIONS

- Weight Scales
- Direct Temperature Measurement
- Gas Analyzers
- Strain-Gage Transducers
- Instrumentation
- Data Acquisition
- Industrial Process Control
- 6-Digit DVMs

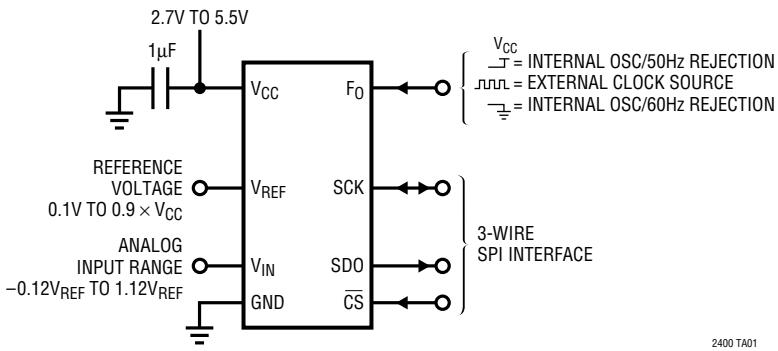
DESCRIPTION

The LTC®2400 is a 2.7V to 5.5V micropower 24-bit converter with an integrated oscillator, a 4ppm INL and 0.3ppm RMS noise. It uses delta-sigma technology and it provides single cycle settling time for multiplexed applications. Through a single pin the LTC2400 can be configured for better than 110dB rejection at 50Hz or 60Hz ±2%, or it can be driven by an external oscillator for a user defined rejection frequency in the range 1Hz to 120Hz. The internal oscillator requires no external frequency setting components.

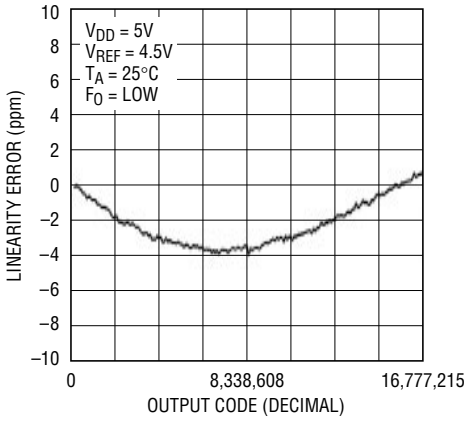
The converter accepts any external reference voltage from 0.1V to 0.9 × V_{CC}. With its extended input conversion range of –12.5% V_{REF} to 112.5% V_{REF} the LTC2400 smoothly resolves the offset and overrange problems of preceding sensors or signal conditioning circuits.

The LTC2400 communicates through a flexible 3-wire digital interface which is compatible with SPI and MICROWIRE™ protocols.

TYPICAL APPLICATION



Total Unadjusted Error vs Output Code

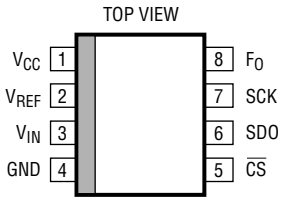


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND .....–0.3V to 7V
Analog Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Reference Input Voltage to GND .. –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Operating Temperature Range
LTC2400C..... 0°C to 70°C
LTC2400I..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec).....300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC2400C LTC2400I
S8 PART MARKING
2400 2400I

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS **(Notes 3, 4)**

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	2.5V ≤ V_{REF} ≤ V_{CC}, (Note 5)	●	24			Bits
Integral Nonlinearity	V_{REF} = 2.5V (Note 6) V_{REF} = 4.5V (Note 6)	●		2 4	8 15	ppm of V_{REF} ppm of V_{REF}
Offset Error	2.5V ≤ V_{REF} ≤ 0.9 × V_{CC}	●		0.5	3	ppm of V_{REF}
Offset Error Drift	2.5V ≤ V_{REF} ≤ 0.9 × V_{CC}	●		0.01		ppm of V_{REF}/°C
Full-Scale Error	2.5V ≤ V_{REF} ≤ 0.9 × V_{CC}	●		4	10	ppm of V_{REF}
Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ 0.9 × V_{CC}	●		0.04		ppm of V_{REF}/°C
Total Unadjusted Error	V_{REF} = 2.5V V_{REF} = 4.5V	●		5 10	20 30	ppm of V_{REF} ppm of V_{REF}
Output Noise	V_{IN} = 0V (Note 13)	●		1.5		μV_{RMS}
Normal Mode Rejection 60Hz ±2%	(Note 7)	●	110	140		dB
Normal Mode Rejection 50Hz ±2%	(Note 8)	●	110	140		dB
Reference Input Rejection 60Hz ±2%	(Note 7)	●	110	140		dB
Reference Input Rejection 50Hz ±2%	(Note 8)	●	110	140		dB
Power Supply Rejection DC	V_{REF} = 2.5V, V_{IN} = 0V	●		100		dB
Power Supply Rejection 60Hz ±2%	V_{REF} = 2.5V, V_{IN} = 0V, (Note 7)	●		110		dB
Power Supply Rejection 50Hz ±2%	V_{REF} = 2.5V, V_{IN} = 0V, (Note 8)	●		110		dB

ANALOG INPUT AND REFERENCE **(Note 3)**

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range	(Note 14)	●	–0.125 • V_{REF}		1.125 • V_{REF}	V
V_{REF}	Reference Voltage Range		●	0.1		0.9 × V_{CC}	V
$C_{S(IN)}$	Input Sampling Capacitance		●		10		pF
$C_{S(REF)}$	Reference Sampling Capacitance		●		15		pF
I_{IN}	Input Leakage Current	V_{IN} = 0V, $\overline{CS}$ = V_{CC}	●		1	10	nA
I_{REF}	Reference Leakage Current	V_{REF} = 5V, $\overline{CS}$ = V_{CC}	●		1	10	nA

DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage $\overline{CS}$, F_O	$2.7V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 3.3V$	● ●	2.5 2.0			V V
V_{IL}	Low Level Input Voltage $\overline{CS}$, F_O	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$	● ●			0.8 0.6	V V
V_{IH}	High Level Input Voltage SCK	$2.7V \le V_{CC} \le 5.5V$ (Note 9) $2.7V \le V_{CC} \le 3.3V$ (Note 9)	● ●	2.5 2.0			V V
V_{IL}	Low Level Input Voltage SCK	$4.5V \le V_{CC} \le 5.5V$ (Note 9) $2.7V \le V_{CC} \le 5.5V$ (Note 9)	● ●			0.8 0.6	V V
I_{IN}	Digital Input Current $\overline{CS}$, F_O	$0V \le V_{IN} \le V_{CC}$	●	–10		10	µA
I_{IN}	Digital Input Current SCK	$0V \le V_{IN} \le V_{CC}$ (Note 9)	●	–10		10	µA
C_{IN}	Digital Input Capacitance $\overline{CS}$, F_O		●		10		pF
C_{IN}	Digital Input Capacitance SCK	(Note 9)	●		10		pF
V_{OH}	High Level Output Voltage SDO	$I_O = -800\mu A$	●	$V_{CC} - 0.5V$			V
V_{OL}	Low Level Output Voltage SDO	$I_O = 1.6mA$	●			0.4V	V
V_{OH}	High Level Output Voltage SCK	$I_O = -800\mu A$ (Note 10)	●	$V_{CC} - 0.5V$			V
V_{OL}	Low Level Output Voltage SCK	$I_O = 1.6mA$ (Note 10)	●			0.4V	V
I_{OZ}	High-Z Output Leakage SDO		●		10		µA

POWER REQUIREMENTS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current Conversion Mode Sleep Mode	 $\overline{CS}$ = 0V (Note 12) $\overline{CS} = V_{CC}$ (Note 12)	● 	 	 200 20	 	 µA µA

TIMING CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range		●	2.56		307.2	kHz
t_{HEO}	External Oscillator High Period		●	0.5		390	µs
t_{LEO}	External Oscillator Low Period		●	0.5		390	µs
t_{CONV}	Conversion Time	F_O = 0V $F_O = V_{CC}$ External Oscillator (Note 11)	● ● ●	130.66 156.80	133.33 160 $20480/f_{EOSC}$ (in kHz)	136 163.20	ms ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 10) External Oscillator (Notes 10, 11)			19.2 $f_{EOSC}/8$		kHz kHz

TIMING CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
D_{ISCK}	Internal SCK Duty Cycle	(Note 10)		45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 9)	●			2000	kHz
t_{LESCK}	External SCK Low Period	(Note 9)	●	250			ns
t_{HESCK}	External SCK High Period	(Note 9)	●	250			ns
t_{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 10, 12) External Oscillator (Notes 10, 11)	● ●	1.64	1.67 $256/f_{EOSC}$ (in kHz)	1.7	ms ms
t_{DOUT_ESCK}	External SCK 32-Bit Data Output Time	(Note 9)	●		$32/f_{ESCK}$ (in kHz)		ms
t_1	$\overline{CS}$ ↓ to SDO Low Z		●	0		50	ns
t2	$\overline{CS}$ ↑ to SDO High Z		●	0		50	ns
t3	$\overline{CS}$ ↓ to SCK ↓	(Note 10)	●	0		50	ns
t4	$\overline{CS}$ ↓ to SCK ↑	(Note 9)	●	50			ns
t_{KQMAX}	SCK ↓ to SDO Valid		●			150	ns
t_{KQMIN}	SDO Hold After SCK ↓	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS}$ ↓		●	50			ns
t_6	SCK Hold After $\overline{CS}$ ↓		●			50	ns

The ● denotes specifications which apply over the full operating temperature range; all other limits and typicals apply to $T_A = 25°C$.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7 to 5.5V unless otherwise specified.

Note 4: Internal Conversion Clock source with the F_O pin tied to GND or to V_{CC} or to external conversion clock source with f_{EOSC} = 153600Hz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: F_O = 0V (internal oscillator) or f_{EOSC} = 153600Hz ±2% (external oscillator).

Note 8: $F_O = V_{CC}$ (internal oscillator) or f_{EOSC} = 128000Hz ±2% (external oscillator).

Note 9: The converter is in External SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the Data Output is f_{ESCK} and is expressed in kHz.

Note 10: The converter is in Internal SCK mode of operation such that the SCK pin is used as digital output. In this mode of operation the SCK pin has a total equivalent load capacitance C_{LOAD} = 20pF.

Note 11: The external oscillator is connected to the F_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 12: The converter uses the internal oscillator. F_O = 0V or $F_O = V_{CC}$.

Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: For reference voltage values $V_{REF} > 2.5V$ the extended input of $-0.125 \bullet V_{REF}$ to $1.125 \bullet V_{REF}$ is limited by the absolute maximum rating of the Analog Input Voltage pin (Pin 3). For $2.5V < V_{REF} \leq 0.267V + 0.89 \bullet V_{CC}$ the Input Voltage Range is –0.3V to $1.125 \bullet V_{REF}$. For $0.267V + 0.89 \bullet V_{CC} < V_{REF} \leq V_{CC}$ the Input Voltage Range is –0.3V to V_{CC} + 0.3V.

PIN FUNCTIONS

V_{CC} (Pin 1): Positive Supply Voltage. Bypass to GND (Pin 4) with a 10µF tantalum capacitor in parallel with 0.1µF ceramic capacitor as close to the part as possible.

V_{REF} (Pin 2): Reference Input. The reference voltage range is 0.1V to $0.9 \times V_{CC}$.

V_{IN} (Pin 3): Analog Input. The input voltage range is $-0.125 \bullet V_{REF}$ to $1.125 \bullet V_{REF}$. For $V_{REF} > 2.5V$ the input voltage range may be limited by the pin absolute maximum rating of –0.3V to V_{CC} + 0.3V.

GND (Pin 4): Ground. Shared pin for analog ground, digital ground, reference ground and signal ground. Should be connected directly to a ground plane through a minimum length trace or it should be the single-point-ground in a single point grounding system.

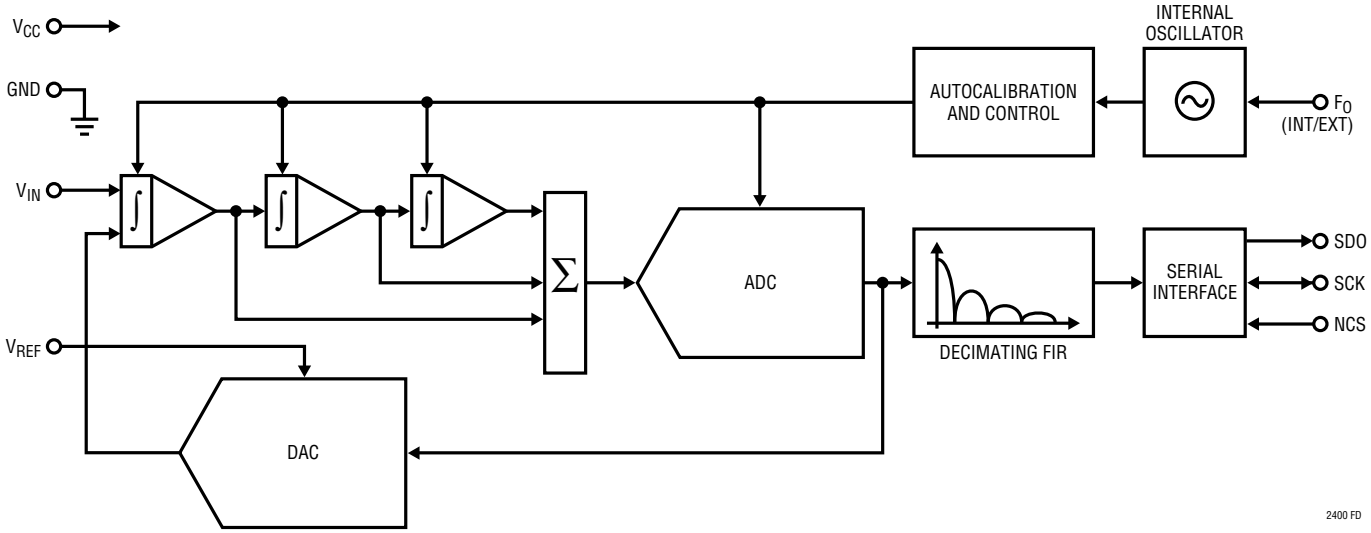
$\overline{CS}$ (Pin 5): Active Low Digital Input. A low on this pin enables the SDO digital output. Following each conversion the ADC automatically enters the Sleep mode and remains in this low power state as long as $\overline{CS}$ is high. A low on $\overline{CS}$ wakes up the ADC. A high on this pin disables the SDO digital output. A low-to-high transition on $\overline{CS}$ during the Data Output state aborts the data transfer and stats a new conversion.

SDO (Pin 6): Three-State Digital Output. During the data output period this pin is used for serial data output. When the chip select $\overline{CS}$ is high ($\overline{CS} = V_{CC}$) the SDO pin is in a high impedance state. During the Conversion and Sleep periods this pin can be used as a conversion status output. The conversion status can be observed by pulling $\overline{CS}$ low.

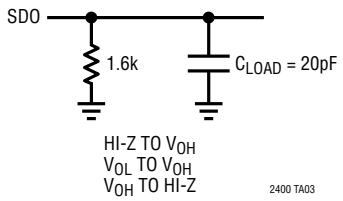
SCK (Pin 7): Bidirectional Digital. In Internal Serial Clock Operation mode, SCK is used as digital output for the internal serial interface clock during the data output period. In External Serial Clock Operation mode, SCK is used as digital input for the external serial interface. A weak internal pull-up is automatically activated in Internal Serial Clock Operation mode.

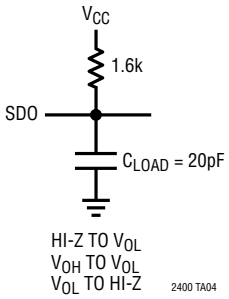
F_O (Pin 8): Digital input which controls the ADC's notch frequencies and conversion time. When the F_O pin is connected to V_{CC} ($F_O = V_{CC}$) the converter uses its internal oscillator and the digital filter first null is located at 50Hz. When the F_O pin is connected to GND (F_O = 0V) the converter uses its internal oscillator and the digital filter first null is located at 60Hz. When F_O is driven by an external clock signal with a frequency f_{EOSC} the converter uses this signal as its clock and the digital filter first null is located at a frequency $f_{EOSC}/2560$.

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS





APPLICATIONS INFORMATION

Converter Operation Cycle

The LTC2400 operation cycle is composed of three distinct states: Conversion, Sleep and Data Output (see Figure 1). After the completion of a conversion the LTC2400 automatically enters the Sleep state and reduces its power consumption by more than an order of magnitude. The converter remains in this state as long as a logic HIGH level is detected at the $\overline{CS}$ pin. Whenever a new data point is not required the LTC2400 should be kept in this state by maintaining a logic HIGH at the $\overline{CS}$ pin.

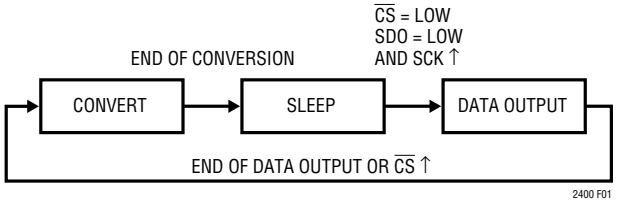


Figure 1. LTC2400 State Transition Diagram

From the Sleep state the converter will transition into the Data Output state on the first LOW to HIGH transition of the SCK pin which occurs while the $\overline{CS}$ input pin is driven LOW (the SDO output pin is also in a LOW state indicating the conversion is complete). The signal at the SCK pin can be generated internally (Internal SCK mode and SCK is an output pin) or externally (External SCK mode and SCK is an input pin).

When the converter is in the Data Output state and logic HIGH is detected at the $\overline{CS}$ pin the Data Output Operation is aborted, a new conversion is started and the LTC2400 enters the Conversion state. Even if a logic LOW is continuously maintained at the $\overline{CS}$ pin the data output is automatically terminated after the transmission of the 32nd bit of data. At this moment a new conversion is started and the LTC2400 enters the Conversion state.

A detailed description of the transitions between the Sleep, Data Output and Conversion states in various conditions is contained in the Configuration Options section.

The time the converter spends in each one of these three states is determined by the selected operation mode. The various options are described in Table 1.

Power-Up Sequence

The LTC2400 automatically enters an internal reset state whenever the power supply voltage V_{CC} drops below approximately 2.2V. This feature is necessary in order to guarantee the integrity of the conversion result and of the Serial Interface mode selection.

When the V_{CC} voltage raises above this critical threshold the converter creates an internal power-on-reset signal with duration of approximately 0.5ms. The power-on-reset signal clears all internal registers and activates the internal SCK pull-up device. After the power-on-reset delay, if the $\overline{CS}$ pin is LOW, the SCK pin is tested and the Serial Clock Operation mode is selected (internal if SDO = HIGH and external if SDO = LOW). Following the power-on-reset signal the LTC2400 starts a normal conversion cycle and follows the normal succession of states described above.

APPLICATIONS INFORMATION

Table 1. LTC2400 State Duration

State	Operating Mode		Duration
CONVERT	Internal Oscillator	F_O = LOW (60Hz Rejection)	133ms
		F_O = HIGH (50Hz Rejection)	160ms
	External Oscillator	F_O = External Oscillator with Frequency f_{EOSC} kHz	$20480/f_{EOSC}$ms
SLEEP			As Long As $\overline{CS}$ = HIGH
DATA OUTPUT	Internal Serial Clock	F_O = LOW/HIGH (Internal Oscillator)	As Long As $\overline{CS}$ = LOW But Not Longer Than 1.67ms
		F_O = External Oscillator with Frequency f_{EOSC} kHz	As Long As $\overline{CS}$ = LOW But Not Longer Than $256/f_{EOSC}$ms
	External Serial Clock with Frequency f_{SCK} kHz		As Long As $\overline{CS}$ = LOW But Not Longer Than $32/f_{SCK}$ms

Reference Voltage Range

The LTC2400 can accept a reference voltage from 0V to $0.9 \times V_{CC}$. The converter output noise is determined by the thermal noise of the front end circuits, and as such it will not scale with the reference voltage. Therefore, a decrease in reference voltage will not improve the converter resolution. On the other hand, a reduced reference voltage will improve the overall converter INL performance. The recommended range for the LTC2400 voltage reference is 100mV to $0.9 \times V_{CC}$.

Input Voltage Range

The converter is able to accommodate system level offset and gain errors as well as system level overrange situations due to its extended input range. The LTC2400 converts input signals within the extended input range $-0.125V \bullet V_{REF}$ to $1.125 \bullet V_{REF}$.

For large values of V_{REF} this range is limited by the absolute maximum voltage range of –0.3V to (V_{CC} + 0.3V). Beyond this range the input ESD protection devices begin to turn on and the errors due to the input leakage current increase rapidly.

Because of the very low input capacitance of the V_{IN} pin, if the V_{IN} signal can go beyond the absolute maximum range of –0.3V to (V_{CC} + 0.3V) a resistor of up to 5k can be added in series with the V_{IN} input in order to limit the input current. In the physical layout it is important to maintain the parasitic capacitance of the connection between this series resistance and the V_{IN} pin as low as possible, therefore the resistor should be located as close as possible to the V_{IN} pin. The effect of the series resistance on the converter accuracy can be evaluated from the curves presented in the Typical Performance Characteristics section. In addition it is important to understand that such a series resistor will introduce a temperature dependent offset error due to the input leakage current. A 10nA input leakage current will develop a 1ppm offset error on a 500Ω resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

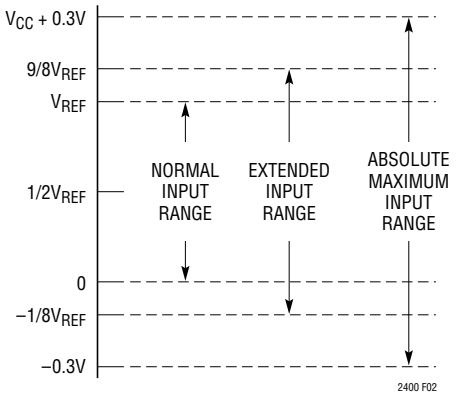


Figure 2. LTC2400 Input Range

APPLICATIONS INFORMATION

Output Data Format

The LTC2400 serial output data stream can be up to 32 bits long. The serial data transfer can be aborted at any time as described in the Configuration Options section. A serial bit is output at the SDO pin on each falling edge of the SCK signal after the first rising edge during the Data Output state. The first four bits contain status information indicating the sign and the expanded input range condition for the input signal.

Bit 31 (first output bit) is the end of conversion (EOC) indicator. This bit is available at the SDO pin during the Conversion and Sleep states whenever the $\overline{CS}$ pin is LOW. This bit is HIGH only during the Conversion and goes LOW when the conversion is complete.

Bit 30 (second output bit) is not used in this implementation and is always LOW.

Bit 29 (third output bit) is the conversion result sign indicator (SIG). If the input signal is ≥0 this bit is HIGH. If the input signal is <0 this bit is LOW.

Bit 28 (forth output bit) is the extended input range (EXR) indicator. If the input is within the normal input range $0 \le V_{IN} \le V_{REF}$ this bit is LOW. If the input is outside the normal input range $V_{IN} > V_{REF}$ or $V_{IN} < 0$ this bit is HIGH. The function of these bits is summarized in Table 2.

Table 2. LTC2400 Status Bits

Input Range	B31 (MSB) EOC	B30	B29 SIG	B28 EXR
$V_{IN} > V_{REF}$	0	0	1	1
$0 \le V_{IN} \le V_{REF}$	0	0	1	0
$V_{IN} < 0$	0	0	0	1

The next 28 bits represent the conversion result and are output MSB first (i.e. Bit 4 is the most significant bit of the conversion result while Bit 31 is the least significant bit of the conversion result). See Table 3.

As long as the voltage on the V_{IN} pin is maintained within the –0.3V to (V_{CC} + 0.3V) absolute maximum operating range a correct result is generated for any input value from $-0.125 \cdot V_{REF}$ to $1.125 \cdot V_{REF}$. For input voltages greater than $1.125 \cdot V_{REF}$ the conversion result is clamped to the value corresponding to $1.125 \cdot V_{REF}$. For input voltages below $-0.125 \cdot V_{REF}$ the conversion result is clamped to the value corresponding to $-0.125 \cdot V_{REF}$.

The output code including the status bits form a uniform monotonic unsigned binary encoding of the analog input value. Digital arithmetic operations can be performed upon the entire 32-bit output without having to eliminate or block out any one of the four status bits.

Table 3. LTC2400 Output Data Format

Input Voltage	B31 EOC	B30 DMY	B29 SIG	B28 EXR	B27 MSB	B26	B25	B24	B23	…	B0 LSB
$V_{IN} > 9/8 \cdot V_{REF}$	0	0	1	1	0	0	0	1	1	...	1
$9/8 \cdot V_{REF}$	0	0	1	1	0	0	0	1	1	...	1
V_{REF} + 1LSB	0	0	1	1	0	0	0	0	0	...	0
V_{REF}	0	0	1	0	1	1	1	1	1	...	1
$3/4V_{REF}$ + 1LSB	0	0	1	0	1	1	0	0	0	...	0
$3/4V_{REF}$	0	0	1	0	1	0	1	1	1	...	1
$1/2V_{REF}$ + 1LSB	0	0	1	0	1	0	0	0	0	...	0
$1/2V_{REF}$	0	0	1	0	0	1	1	1	1	...	1
$1/4V_{REF}$ + 1LSB	0	0	1	0	0	1	0	0	0	...	0
$1/4V_{REF}$	0	0	1	0	0	0	1	1	1	...	1
0	0	0	1	0	0	0	0	0	0	...	0
–1LSB	0	0	0	1	1	1	1	1	1	...	1
$-1/8 \cdot V_{REF}$	0	0	0	1	1	1	1	0	0	...	0
$V_{IN} < -1/8 \cdot V_{REF}$	0	0	0	1	1	1	1	0	0	...	0

APPLICATIONS INFORMATION

Frequency Rejection Selection (F_O Pin Connection)

The LTC2400 internal oscillator provides better than 110dB normal mode rejection at the line frequency and all its harmonics for 50Hz ±2% or 60Hz ±2%. For 60Hz rejection F_O (Pin 8) should be connected to GND (Pin 4) or to a LOW logic level while for 50Hz rejection the F_O pin should be connected to V_{CC} (Pin 1) or to a HIGH logic level.

The selection of 50Hz or 60Hz rejection can also be made during normal operation by an external controller able to drive F_O to an appropriate logic level. A selection change during the Sleep or Data Output states will not disturb the converter operation. If the selection is made during the Conversion state the result of the conversion in progress may be outside specifications but the following conversions will not be affected.

When a fundamental rejection frequency different from 50Hz or 60Hz is required or when the converter must be synchronized with an outside source the LTC2400 can operate with an external conversion clock. The converter automatically detects the presence of an external clock signal at the F_O pin and turns off the internal oscillator. (The frequency f_{EOSC} of the external signal must be at least 2560Hz.) The external clock signal duty cycle is not significant as long as the minimum and maximum specifications for the high and low periods t_{HEO} and t_{LEO} are observed.

While operating with an external conversion clock with a frequency f_{EOSC} the LTC2400 provides better than 110dB normal mode rejection in a frequency range $f_{EOSC}/2560$ ±4% and its harmonics. The normal mode rejection as a function of the input frequency deviation from $f_{EOSC}/2560$ is shown in Figure 3.

Whenever an external clock is not present at the F_O pin the converter automatically activates its internal oscillator and enters the Internal Conversion Clock mode. The LTC2400 operation will not be disturbed if the change of conversion clock source occurs during the Sleep state or during the Data Output state while the converter uses an external serial clock. If the change occurs during the Conversion state the result of the conversion in progress may be outside specifications but the following conversions will not be affected. If the change occurs during the Data Output state and the converter is in the Internal SCK mode, the serial clock duty cycle may be distorted but the serial data stream will remain valid.

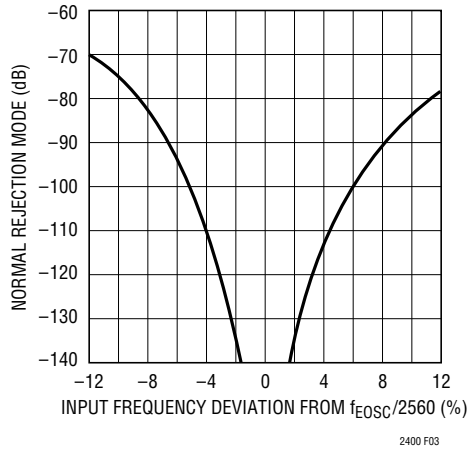


Figure 3. LTC2400 Normal Mode Rejection When Using an External Oscillator of Frequency f_{EOSC}

Digital Signal Levels

The LTC2400 digital inputs (F_O, $\overline{CS}$ and SCK in External SCK mode of operation) accept standard logic levels and the internal hysteresis receivers can tolerate edge rates as slow as 100µs. In the same time the LTC2400 exceptional accuracy, shared ground pin and very low power supply current demand special considerations when designing the digital interface.

The digital output signals (SDO and SCK in Internal SCK mode of operation) are less of a concern because they are not generally active during the Conversion state.

A 250µA power supply current flowing through the 0.01Ω resistance of the common ground pin will develop a 2.5µV offset signal. For a reference voltage V_{REF} = 2.5V this represents a 1ppm offset error. In order to preserve the LTC2400 accuracy it is very important to minimize the ground path impedance which may appear in series with the input and/or reference signal and to reduce the current which may flow through this path.

The GND pin should be connected to a low resistance ground plane through a minimum length trace. The use of multiple via holes is recommended to further reduce the connection resistance.

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In an alternative configuration the GND pin of the converter can be the single-point-ground in a single point grounding system. The input signal ground, the reference signal ground, the digital drivers ground (usually the digital ground) and the power supply ground (the analog ground) should be connected in a star configuration with the common point located as close to the GND pin as possible.

The power supply current during the Conversion state should be kept to a minimum. This goal can be achieved by restricting the number of digital signal transitions occurring during this period to the minimum necessary.

While a digital input signal is in the range 0.5V to (V_{CC} – 0.5V) the CMOS input receiver draws additional current from the power supply. It should be noted that, when any one of the digital input signals (F_O, $\overline{CS}$ and SCK in External SCK mode of operation) is within this range, the LTC2400 power supply current may increase even if the signal in question is at a valid logic level. For micro power operation and in order to minimize the potential errors due to additional ground pin current it is recommended to drive all digital input signals to full CMOS levels [V_{IL} < 0.4V and V_{OH} > (V_{CC} – 0.4V)].

Severe ground pin current disturbances can also occur due to the undershoot of fast digital input signals. Undershoot and overshoot occur because of the impedance mismatch at the converter pin when the transition time of an external control signal is less than twice the propagation delay from the driver to LTC2400. For reference, on a regular FR-4 board the signal propagation velocity is approximately 183ps/inch for internal traces and 170ps/inch for surface traces. Thus a driver generating a control signal with a minimum transition time of 1ns must be connected to the converter pin through a trace shorter than 2.5 inches. This problem becomes particularly difficult when shared control lines are used and multiple reflections may occur. The solution is to carefully terminate all transmission lines close to their characteristic impedance.

Parallel termination near the LTC2400 pin will eliminate this problem but will increase the driver power dissipation. A series resistor between 27Ω and 56Ω placed near the driver or near the LTC2400 pin will also eliminate this problem without additional power dissipation. The actual resistor value depends upon the trace impedance and connection topology.

SERIAL INTERFACE

The LTC2400 transmits the conversion results and receives the start of conversion command through a synchronous 3-wire interface. During the Conversion and Sleep states this interface is used to assess the converter status and during the Data Output state it is used to read the conversion result.

Serial Clock Input/Output SCK

The serial clock signal present on SCK (Pin 7) is used to synchronize the data transfer. Each bit of data is driven by SDO (Pin 6) on the falling edge of the serial clock.

In the Internal SCK mode of operation the SCK pin is an output and the LTC2400 creates its own serial clock by dividing the internal conversion clock by 8. In the External SCK mode of operation the SCK pin is used as input. The selection between Internal and External SCK operation modes is performed every time a HIGH to LOW transition is detected at the $\overline{CS}$ pin. If SCK is HIGH during this transition the converter enters the Internal SCK mode. If SCK is LOW during this transition the converter enters the External SCK mode.

In order to accommodate the continuous conversion mode in which $\overline{CS}$ (Pin 5) is permanently tied to GND (Pin 4), the LTC2400 also selects between Internal and External SCK operation modes during power-on reset. At this time an internal pull-up is activated in order to test the state of the SCK pin even if an external driver does not drive this pin. If during the power-on reset phase the $\overline{CS}$ pin and the SCK pin are kept low, the converter enters the External SCK mode. If during the power-on reset phase the $\overline{CS}$ pin is LOW and the SCK pin is not externally driven or is kept HIGH, the converter enters the Internal SCK mode.

The converter remembers the previously selected Serial Clock mode of operation as long as $\overline{CS}$ is low. Following a LOW to HIGH transition on $\overline{CS}$ a new selection must be made on the following $\overline{CS}$ HIGH to LOW transition. Even if the LTC2400 is in Internal SCK mode the SCK output driver

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is enabled only during the Data Output state. During the Conversion and Sleep states, if $\overline{CS}$ is LOW and the converter is in Internal SCK mode, an internal weak pull-up is activated for the SCK pin. During the same states, if $\overline{CS}$ is HIGH the internal pull-up is activated only if SCK is already high. Thus, when not externally driven the SCK pin will be kept HIGH by the internal pull-up such that the $\overline{CS}$ falling edge will select the Internal SCK mode.

Figure 4 shows a typical data output sequence in the Internal SCK mode which is selected when, during the falling edge of $\overline{CS}$, the SCK pin is HIGH. Following the falling edge of $\overline{CS}$ the converter drives 32 clock pulses through the SCK pin. On every falling edge of SCK a new data bit is driven at the SDO pin.

Figure 5 shows a typical data output sequence in the External SCK mode which is selected when, during the falling edge of $\overline{CS}$, the SCK pin is LOW. Following the falling edge of $\overline{CS}$ the first 32 clock pulses received at the SCK pin are used to shift out the conversion result through the SDO pin.

Serial Data Output SDO

The serial data output pin, SDO (Pin 6), is used to drive the serial data during the Data Output state. In addition the SDO pin is used as an end of conversion indicator during the Conversion and Sleep states.

In order to enable a shared serial data line configuration, when $\overline{CS}$ (Pin 5) is HIGH the SDO driver is switched to a high impedance state.

Whenever $\overline{CS}$ is LOW during the conversion phase the SDO pin is driven HIGH to indicate that the current conversion cycle has not yet been completed.

Whenever $\overline{CS}$ is LOW during the sleep phase the SDO pin is driven LOW to indicate that the current conversion cycle has been completed. It is important to notice that the LTC2400 will exit the Sleep state on the first rising edge of SCK occurring while $\overline{CS}$ is LOW.

When operating in the External SCK mode, the end of conversion status can be tested without forcing the con-

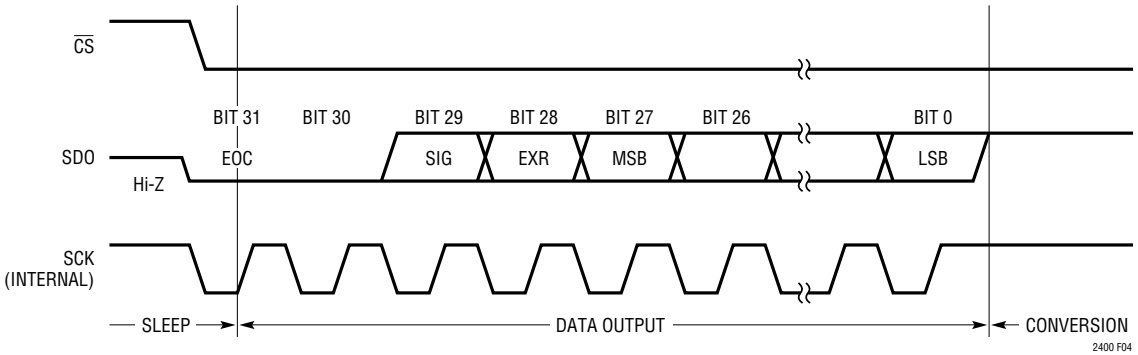

Figure 4. Typical Internal SCK Data Output Operation

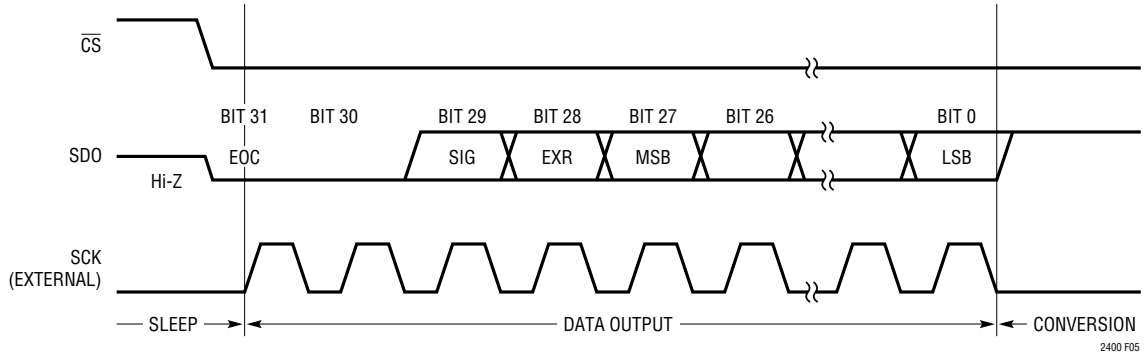

Figure 5. Typical External SCK Data Output Operation

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verter to enter the Data Output state as long as the SCK pin is maintained LOW during the test (the SCK pin should be already LOW on the falling edge of $\overline{CS}$ in order to indicate the External SCK mode). The serial interface waveforms corresponding to this situation are shown in Figure 6. The first time $\overline{CS}$ is driven LOW the SDO signal changes from the HIGH-Z state to HIGH indicating that the conversion is in progress. The second time $\overline{CS}$ is driven LOW the SDO signal again changes from HIGH-Z to HIGH because the conversion is not yet finished. When the conversion cycle is completed the SDO pin switches from HIGH to LOW indicating the availability of a new conversion result and the LTC2400 enters the Sleep state. As long as the SCK pin is maintained LOW the converter remains in Sleep mode. The third time $\overline{CS}$ is driven LOW the SDO signal changes from HIGH-Z to LOW indicating a completed conversion. At some point in time the SCK pin is driven from a LOW to a HIGH thus terminating the Sleep state and beginning the Data Output state.

When operating in the Internal SCK mode, the end of conversion status can be tested without forcing the converter to enter the Data Output state as long as the $\overline{CS}$ pin is maintained LOW for a time period less than $T_{EOCtest}$. $T_{EOCtest}$ is equal with 45% of the Internal SCK period $1/f_{SCK}$. If LTC2400 is using the internal oscillator (Pin F_O is maintained at a LOW or HIGH logic level) $T_{EOCtest} = 23\mu s$. If the LTC2400 is using an external oscillator of frequency f_{EOSC} (connected to the F_O pin) $T_{EOCtest} = 3.6/f_{EOSC}$. The serial interface waveforms corresponding to this situation are shown in Figure 7. The first time $\overline{CS}$ is driven LOW the SDO signal changes from the HIGH-Z state to HIGH indicating that the conversion is in progress. The second time $\overline{CS}$ is driven LOW the SDO signal again changes from HIGH-Z to HIGH because the conversion is not yet finished. When the conversion cycle is completed the SDO pin switches from HIGH to LOW indicating the availability of a new conversion result and the LTC2400 enters the Sleep state. At this moment, in order to maintain the

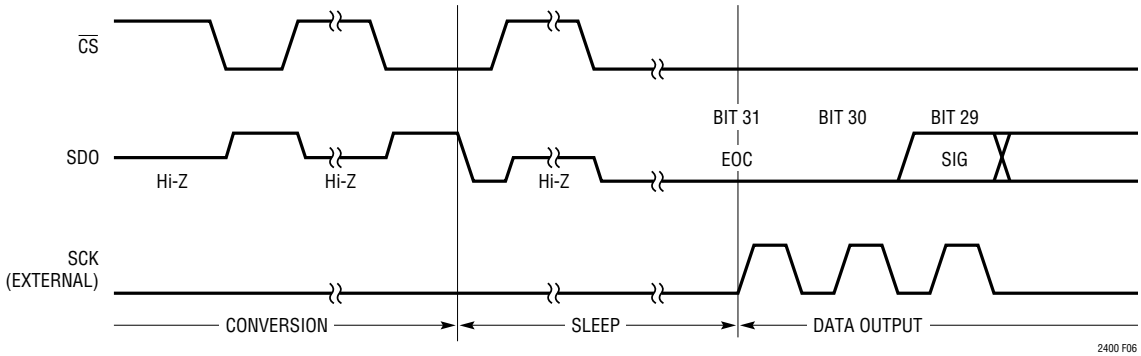

Figure 6. End of Conversion Test—External SCK Operation

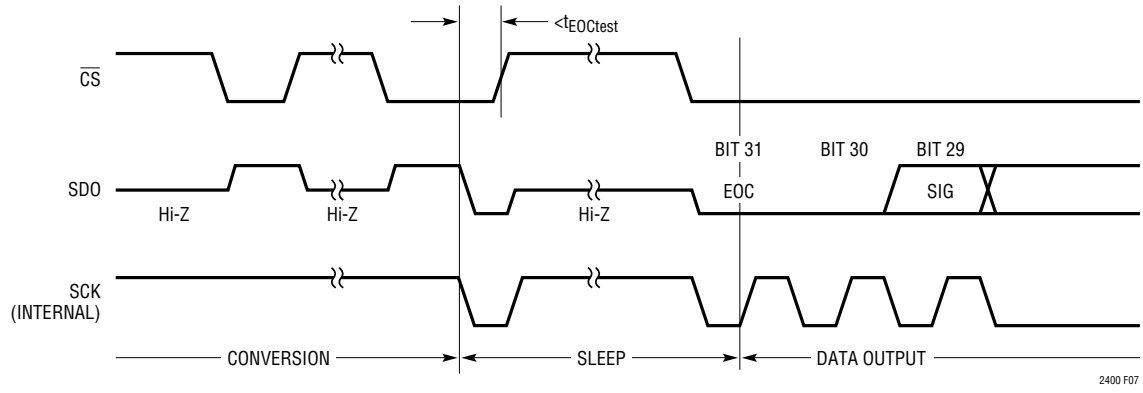

Figure 7. End of Conversion Test—Internal SCK Operation

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converter in Sleep mode $\overline{CS}$ must not remain LOW for longer than $T_{EOCtest}$. The third time $\overline{CS}$ is driven LOW the SDO signal changes from HIGH-Z to LOW indicating a completed conversion. After a $T_{EOCtest}$ time interval the SCK pin changes from a LOW to a HIGH thus terminating the Sleep state and beginning the Data Output state.

Chip Select Input $\overline{CS}$ (Figure 8)

The active low chip select, $\overline{CS}$ (Pin 5), is used to test the conversion status and to enable the data output transfer as described in the previous sections.

In addition, the $\overline{CS}$ signal can be used to trigger a new conversion cycle before the entire serial data transfer has been completed. The LTC2400 will abort any serial data transfer in progress and start a new conversion cycle anytime a LOW to HIGH transition is detected at the $\overline{CS}$ pin after the converter has entered the Data Output state (i.e. after the first rising edge of SCK which occurs while $\overline{CS}$ = LOW and SDO = LOW).

$\overline{CS}$ (Pin 5) can also be used to control the converter Autostart mode of operation. This configuration is described in Figure 12. After the completion of a conversion the LTC2400 enters the low power Sleep state. The time spent in this state is controlled by an internal 25nA current source which discharges an external capacitor connected to the $\overline{CS}$ pin. When this capacitor has been discharged to approximately 1.4V (1.1V for V_{CC} = 3V), the LTC2400 will start the serial data transfer followed by a new conversion cycle. The autostart is particularly useful when combined with the Internal SCK operation mode.

The $\overline{CS}$ waveform in Figure 12 shows the external capacitor charge and discharge cycles. The value of the external capacitor C_{EXT} determines the duration of the sleep cycle.

It should be noticed that the external capacitor discharge current is kept very small in order to decrease the converter power dissipation in the Sleep state. In the Autostart mode the analog voltage on the $\overline{CS}$ pin can not be observed without disturbing the converter operation using a regular oscilloscope probe. When using this configuration it is important to minimize the external leakage current at the $\overline{CS}$ pin by using a low leakage external capacitor and properly cleaning the PCB surface.

CONFIGURATION OPTIONS

This section describes the configuration details of the serial interface and conversion cycle control signals for the LTC2400 most significant operating modes. In all these cases the converter can use the internal oscillator (F_O = LOW or F_O = HIGH) or an external oscillator connected to the F_O pin.

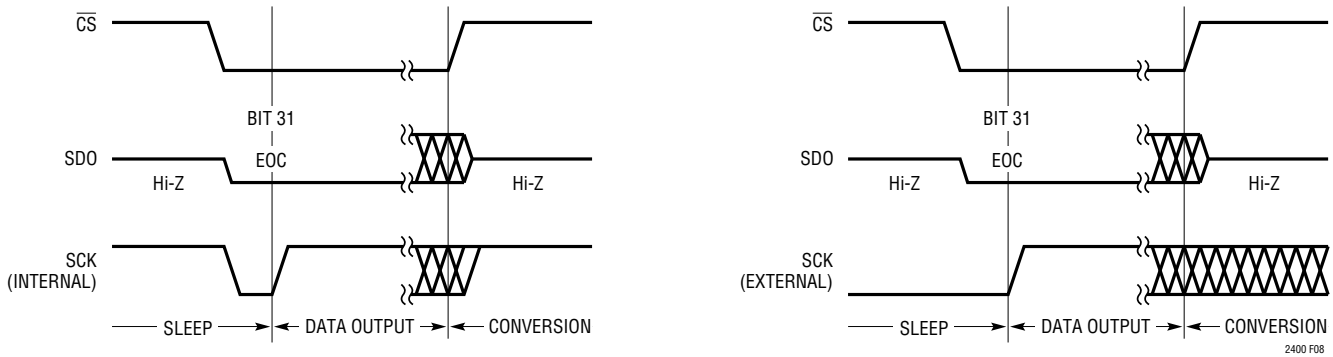

Figure 8. Data Output Abort

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A summary of the most common configuration options is shown in Table 4.

Internal Serial Clock, Continuous Operation (Figure 9)

In this configuration the converter creates its own serial clock and operates at the maximum possible conversion rate. Following a conversion the LTC2400 spends only a minimum amount of time in the Sleep state and immediately initiates the data output operation. After all 32 bits of the result are shifted out the converter starts a new cycle.

The $\overline{CS}$ pin is maintained at a LOW logic level. The Internal SCK mode is selected during power-on reset. It is important to ensure that there is no external driver that may be driving the SCK pin LOW during the power-up sequence. An external pull-up device at SCK is not required because the internal weak pull-up device is active.

Internal Serial Clock, Single Cycle Operation (Figure 10)

In this configuration the converter creates its own serial clock and an external controller driving the $\overline{CS}$ signal triggers each conversion operation. The LTC2400 enters the Sleep state following every conversion. When $\overline{CS}$ is driven LOW the converter initiates the data output operation. The $\overline{CS}$ signal remains low during the entire data output phase and is returned to a high state sometime during the Conversion state. After all 32 bits of the result are shifted out, the LTC2400 starts a new conversion.

An external controller can determine if the conversion is completed by driving $\overline{CS}$ to LOW and monitoring the SDO signal. If SDO = LOW a new conversion result is available. If the external controller wants to maintain the LTC2400 in the Sleep state it must limit the time $\overline{CS}$ is maintained LOW to less than $T_{EOCtest}$. For exact values of $T_{EOCtest}$ see the Serial Interface, Serial Data Output (SDO) section.

The Internal SCK mode is reselected on every falling edge of $\overline{CS}$. It is important to ensure that there is no external driver that may be driving the SCK pin LOW during the $\overline{CS}$ falling edge. In general a pull-up resistor at SCK is not required because the internal weak pull-up device is active.

The internal pull-up is disabled when an external driver has pulled SCK LOW while $\overline{CS}$ is HIGH. If this situation may occur (in a shared SCK configuration for example) and the external driver stops driving the SCK pin (enters a HIGH-Z state) while this pin is LOW the internal pull-up is not available to restore SCK to HIGH before the falling edge of $\overline{CS}$. One solution is to control the external driver such that it drives SCK HIGH immediately before entering a HIGH-Z state.

A similar problem may occur during the Sleep state when $\overline{CS}$ is pulsed HIGH-LOW-HIGH in order to test the conversion status. If SDO is LOW (the LTC2400 is in Sleep state) the SCK pin will also be driven LOW in preparation for the Data Output state. When $\overline{CS}$ is driven HIGH in a time shorter than $T_{EOCtest}$ with the desire to postpone the serial output operation, the SCK driver is turned off and the internal pull-up is activated. For a heavy capacitive load on the SCK pin the internal pull-up may not be adequate to return this line to a HIGH level fast enough. This is not a

Table 4. LTC2400 Configuration Options

Configuration	SCK Source	Data Output Length	Conversion Cycle Control	Data Output Control	Connection and Waveforms
Internal SCK, Continuous Conversion	Internal	32 Bits	Minimum	Internal	Figure 9
Internal SCK, Single Cycle Conversion	Internal	32 Bits	$\overline{CS}\downarrow$	$\overline{CS}\downarrow$	Figure 10
Internal SCK, Reduced Data Output	Internal	1 to 32 Bits	$\overline{CS}\downarrow$ and $\overline{CS}\uparrow$	$\overline{CS}\downarrow$ and $\overline{CS}\uparrow$	Figure 11
Internal SCK, Autostart Conversion	Internal	32 Bits	C_{EXT}	Internal	Figure 12
External SCK, Continuous Conversion	External	32 Bits	SCK	SCK	Figure 13
External SCK, Single Cycle Conversion	External	32 Bits	$\overline{CS}$ and SCK	$\overline{CS}$ and SCK	Figure 14
External SCK, Reduced Data Output	External	1 to 32 Bits	$\overline{CS}$ and SCK	$\overline{CS}$ and SCK	Figure 15

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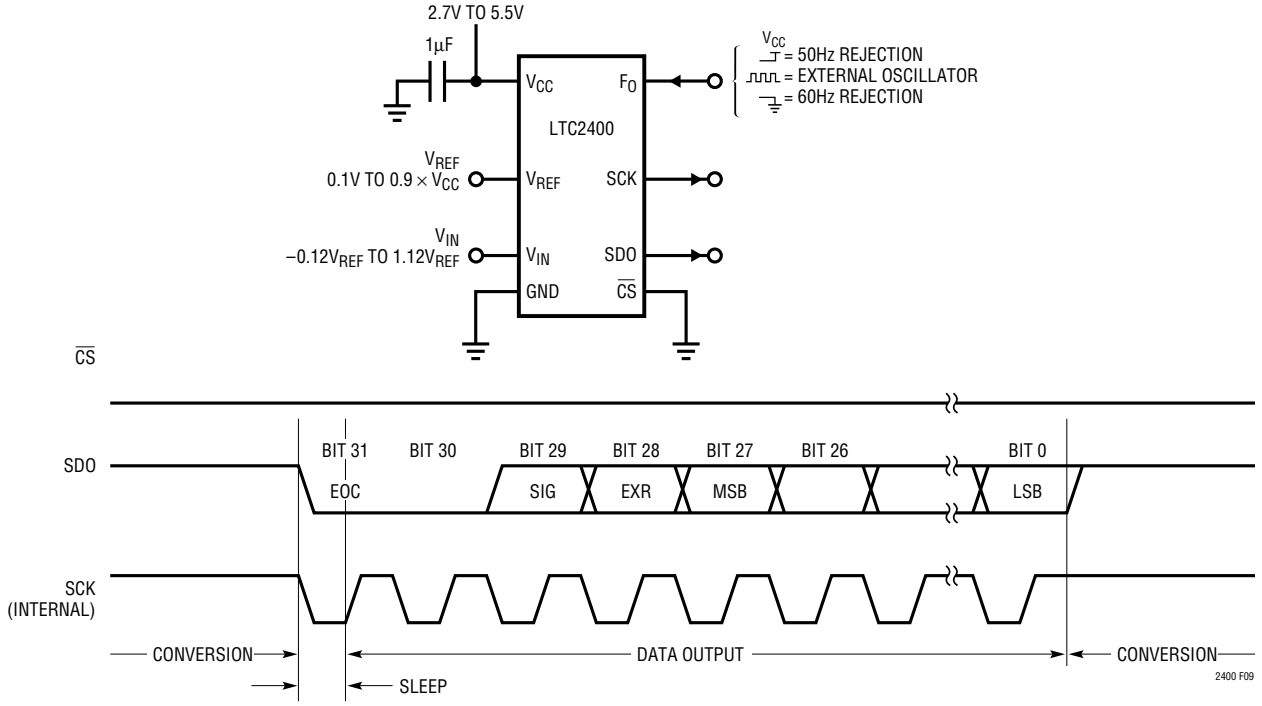

Figure 9. Internal Serial Clock, Continuous Operation

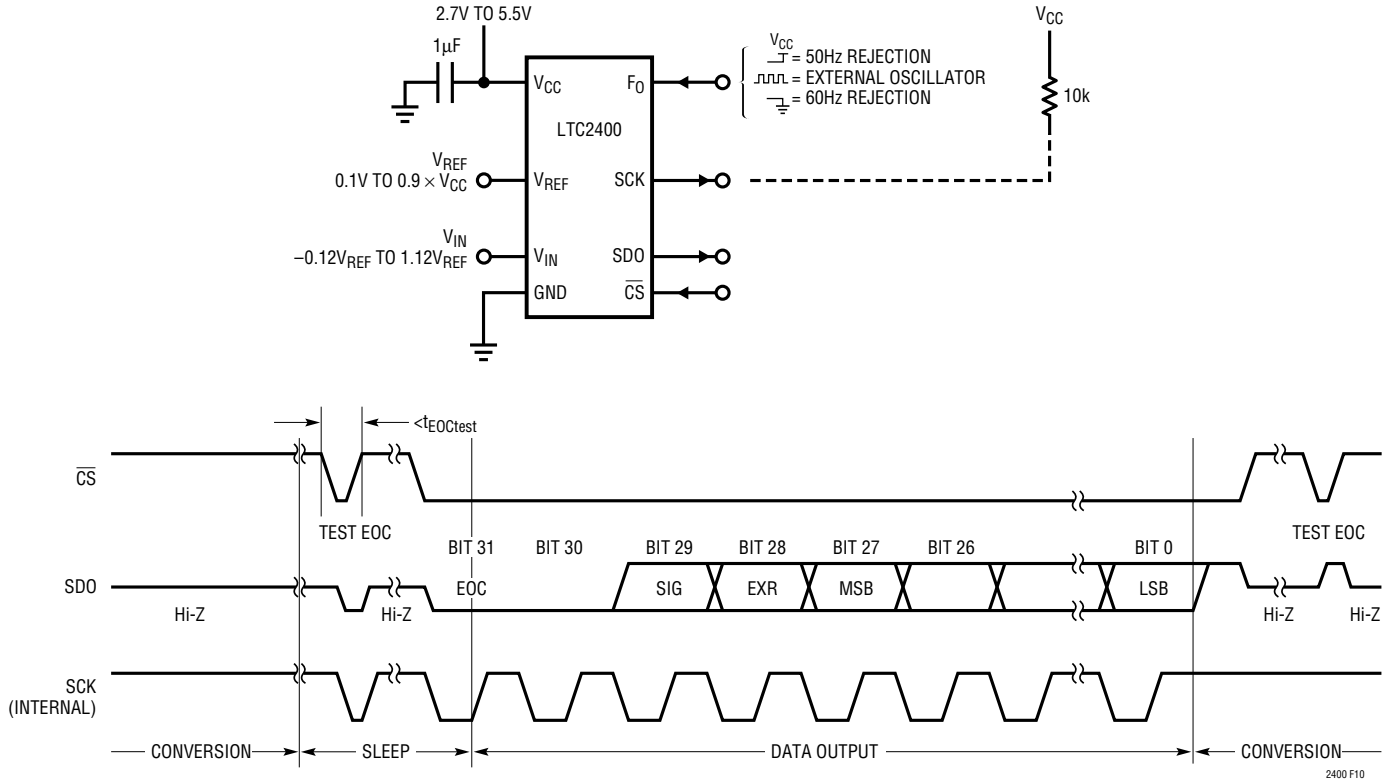

Figure 10. Internal Serial Clock, Single Cycle Operation

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concern if, upon detecting SDO = LOW the $\overline{CS}$ pin is maintained LOW and a serial data output process is initiated.

A solution for both these limit cases is to use an external 10k pull-up resistor on the SCK pin.

Internal Serial Clock, Reduced Data Output Length (Figure 11)

This mode of operation can be used if the result already stored in the converter is no longer relevant and a new result is required as soon as possible. The Data Output state can be aborted immediately after the first rising edge of SCK and a new conversion can be started with minimum delay. This operation mode can also be used when not all 32 bits of the output stream are required. For example when the external controller needs only the four status bits and the 20 most significant result bits the Data Output state can be interrupted following the 24th rising edge of SCK.

In this configuration the converter creates its own serial clock and an external controller driving the $\overline{CS}$ signal triggers each conversion operation. The LTC2400 enters the Sleep state following every conversion. When $\overline{CS}$ is driven LOW the converter initiates the data output operation. The $\overline{CS}$ signal must be maintained LOW until the first rising edge of SCK. After that $\overline{CS}$ is driven HIGH before all 32 bits of the result are shifted out. At this moment the LTC2400 aborts the Data Output state and starts a new conversion.

The Internal SCK mode is reselected on every falling edge of $\overline{CS}$. It is important to ensure that there is no external driver that may be driving the SCK pin LOW during the $\overline{CS}$ falling edge. In general a pull-up resistor at SCK is not required because the internal weak pull-up device is active.

The internal pull-up is disabled when an external driver has pulled SCK LOW while $\overline{CS}$ is HIGH. If this situation occurs (in a shared SCK configuration for example) and the

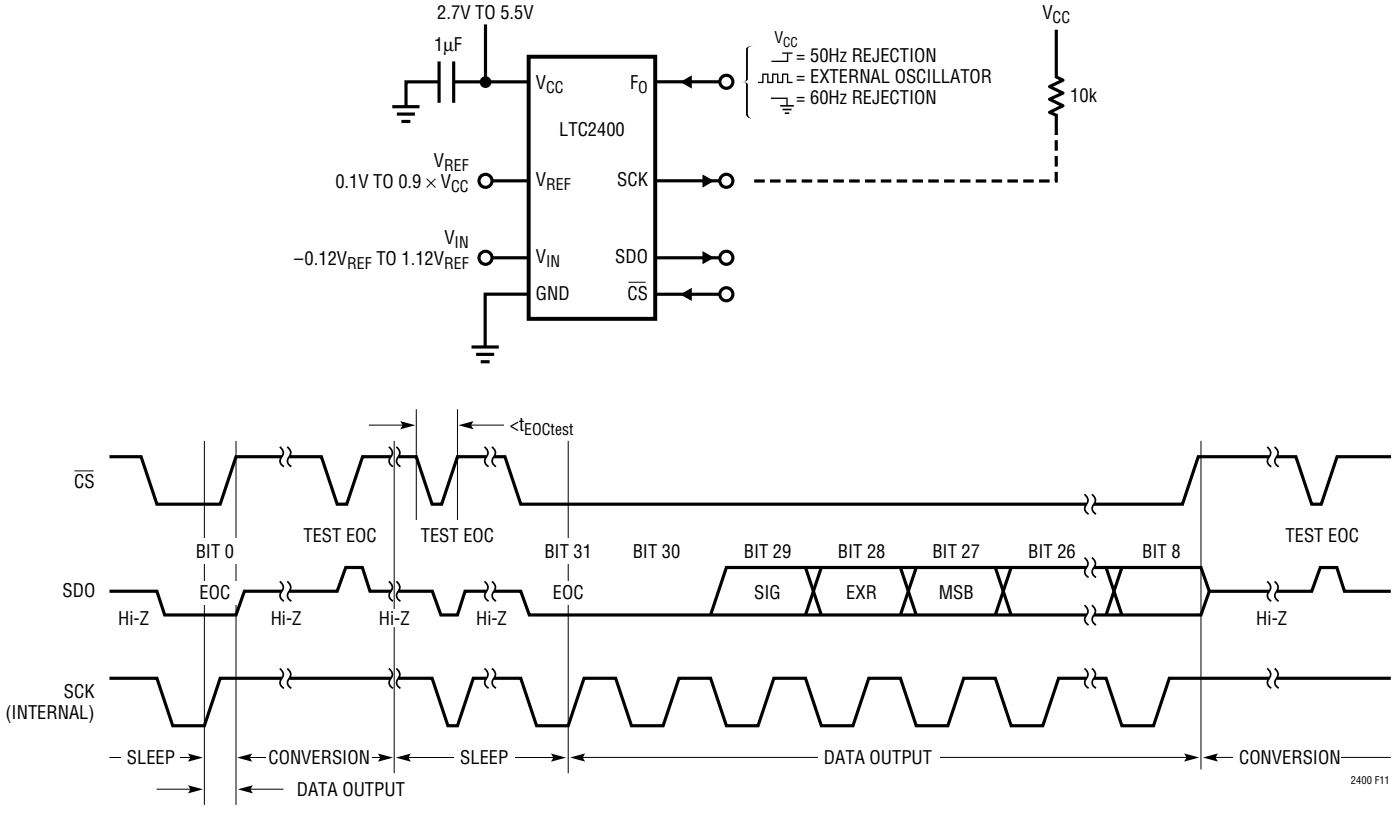

Figure 11. Internal Serial Clock, Reduced Data Output Length

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external driver stops driving the SCK pin (enters a HIGH-Z state) while this pin is LOW, the internal pull-up is not available to restore SCK to HIGH before the falling edge of $\overline{CS}$. A solution is to control the external driver such that it drives SCK HIGH immediately before entering a HIGH-Z state.

A similar problem may occur when $\overline{CS}$ is pulled HIGH (the Data Output state is terminated) while the converter is driving a LOW on the SCK pin. In this case the internal pull-up is again not available to restore SCK to HIGH before the falling edge of $\overline{CS}$. This situation can be avoided by driving $\overline{CS}$ high only following a rising edge of SCK.

An alternative solution for these two problems is to use an external 10k pull-up resistor on the SCK pin.

Internal Serial Clock, Autostart Operation (Figure 12)

In this configuration the converter creates its own serial clock and each conversion operation is triggered by the internal controlled discharge of an external timing capacitor connected to the $\overline{CS}$ pin. The LTC2400 enters the Sleep state following every conversion. The time the converter remains in the Sleep state is determined by the value of the external timing capacitor. Specific values are shown in the Typical Performance Characteristics section. The $\overline{CS}$ capacitor remains discharged during the Data Output state and is automatically recharged during the Conversion state. After all 32 bits of the result are shifted out, the LTC2400 starts a new conversion.

The Internal SCK mode is reselected every time the voltage on the $\overline{CS}$ pin traverses the pin receiver threshold from a high to a low value. It is important to ensure that there is no external driver that may be driving the SCK pin LOW during the $\overline{CS}$ falling edge. In general a pull-up resistor at SCK is not required because the internal weak pull-up device is active.

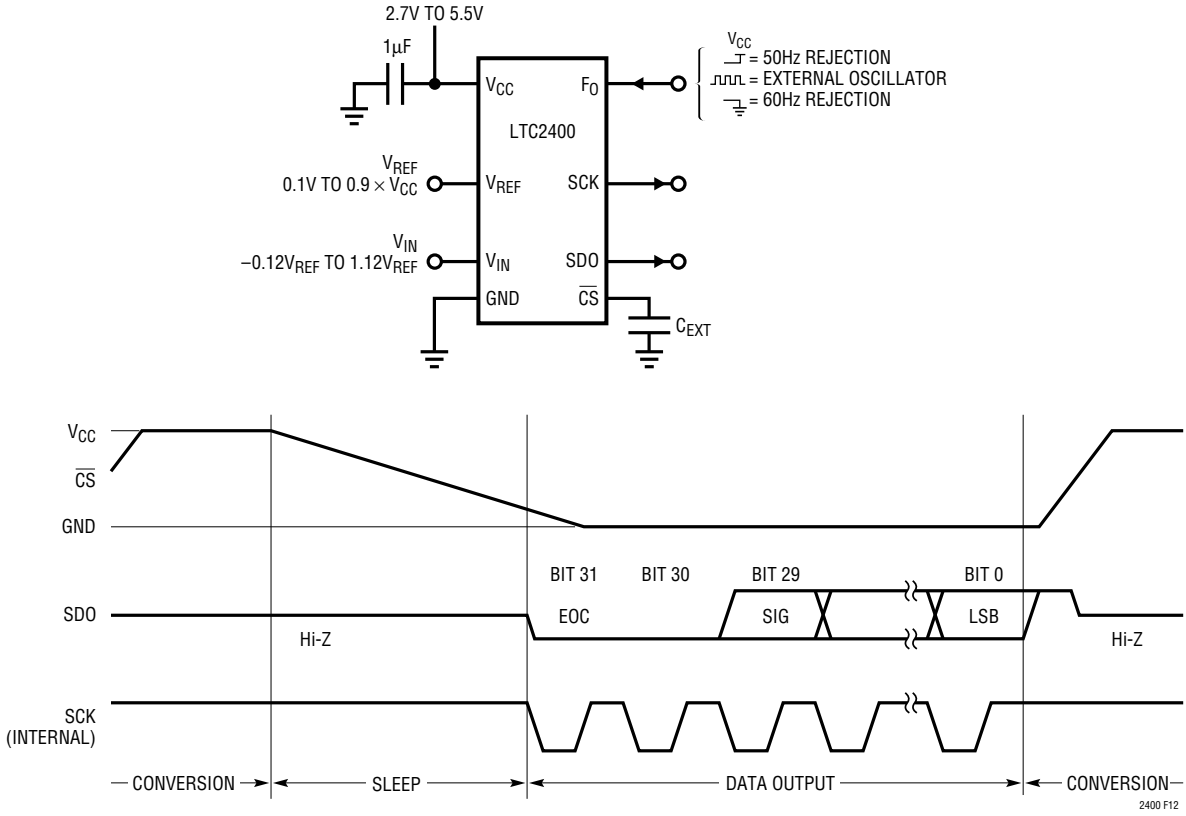

Figure 12. Internal Serial Clock, Autostart Operation

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External Serial Clock, $\overline{CS}$ = 0 Operation (Figure 13)

In this configuration an external controller using the SCK line only directs LTC2400 operation. Following a conversion the LTC2400 remains in the Sleep state until it detects the first rising edge on the SCK pin. After this event it enters the Data Output state where it remains until it detects 32 falling edges on the SCK pin. At this moment all 32 bits of the result have been shifted out and the converter starts a new cycle.

The $\overline{CS}$ pin is maintained at a LOW logic level. The External SCK mode is selected during power-on reset. It is important to ensure that an external driver is forcing the SCK pin LOW before the end of the power-up sequence.

The end of conversion can be detected by monitoring the SDO pin. Following the Data Output state (following the 32nd falling edge of SCK) the SDO pin is HIGH while a new conversion is in progress. As soon as the LTC2400 returns to the Sleep state the SDO pin becomes LOW. An external controller can monitor the voltage on the SDO pin or can use it as an interrupt signal to decide when a new conversion result is available.

External Serial Clock, Single Cycle Operation (Figure 14)

This is the most common configuration for LTC2400. Following a conversion the LTC2400 enters the Sleep state. The converter will remain in this state until it detects the first rising edge of SCK while $\overline{CS}$ is driven LOW. The $\overline{CS}$ signal remains low during the entire data output phase and is returned to a HIGH state sometime during the Conversion state. After all 32 bits of the result are shifted out, the LTC2400 starts a new conversion.

The External SCK mode is reselected on every falling edge of $\overline{CS}$. It is important to ensure that the SCK pin is driven LOW during the $\overline{CS}$ falling edge.

The end of conversion can be detected by testing the SDO pin. Anytime during the Conversion or Sleep states the SDO can be observed after $\overline{CS}$ is driven LOW.

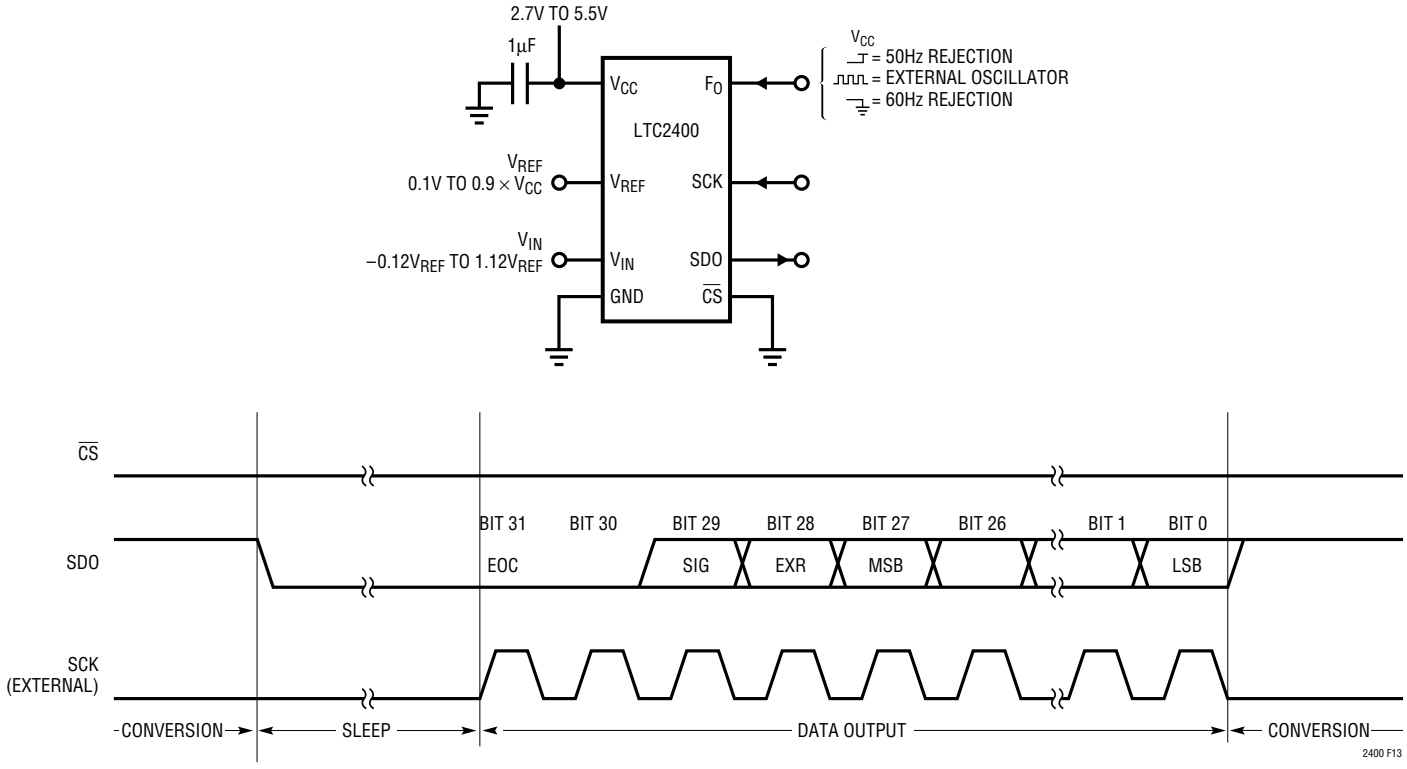

Figure 13. External Serial Clock, $\overline{CS}$ = 0 Operation

APPLICATIONS INFORMATION

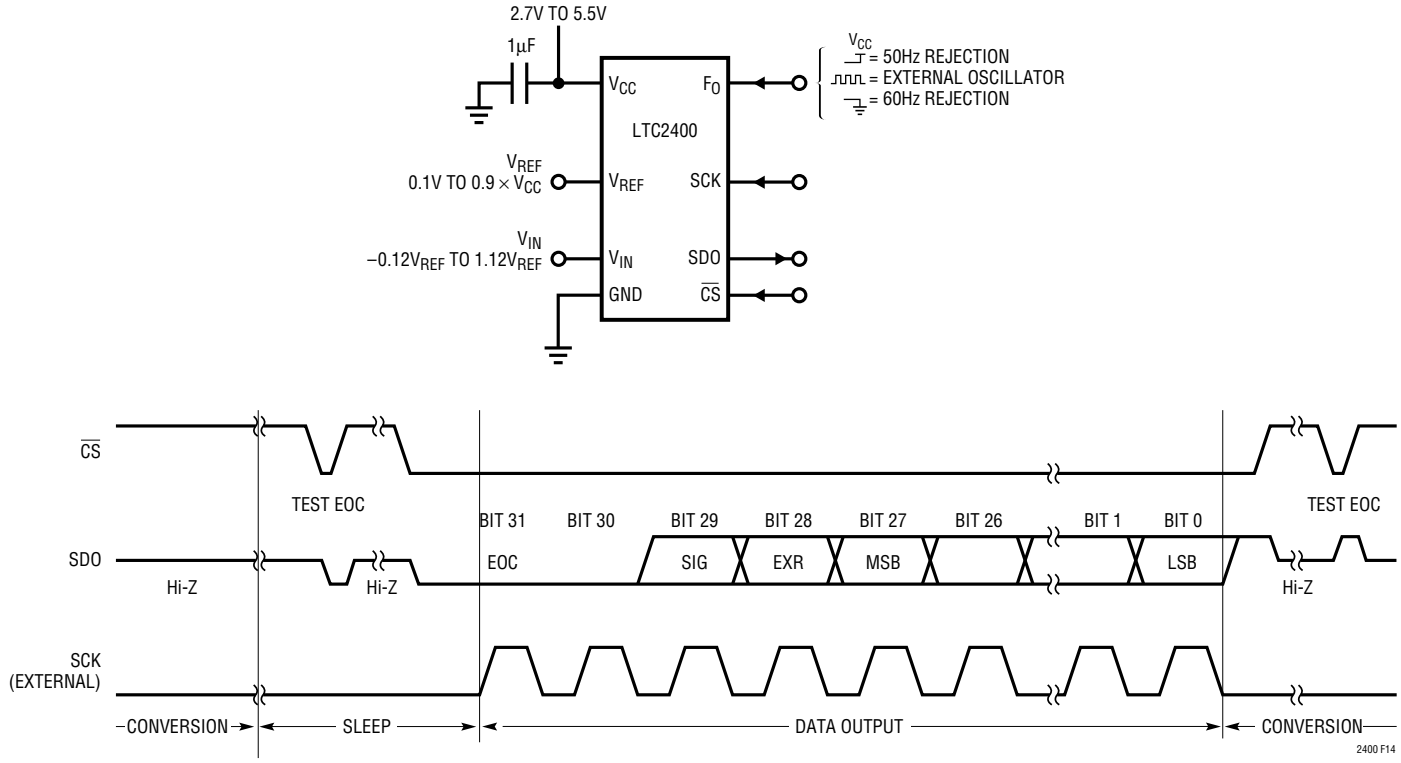

Figure 14. External Serial Clock, Single Cycle Operation

If SDO = HIGH the conversion is not yet completed. If SDO = LOW a new result is available and the Data Output state can be initiated at any time.

External Serial Clock, Reduced Data Output Length (Figure 15)

This mode of operation can be used if the result already stored in the converter is no longer relevant and a new result is required as soon as possible. The Data Output state can be aborted immediately after the first SCK rising edge and a new conversion can be started with minimum delay. This operation mode can also be used when not all 32 bits of the output stream are required. For example, when the external controller needs only the four status bits and the 20 most significant result bits the Data Output state can be interrupted following the 23rd falling edge of SCK.

Following a conversion the LTC2400 enters the Sleep state. The converter will remain in this state until it detects the first rising edge of SCK while $\overline{CS}$ is driven LOW. After that $\overline{CS}$ is driven HIGH before all 32 bits of the result are shifted out. At this moment the LTC2400 aborts the Data Output state and starts a new conversion.

The External SCK mode is reselected on every falling edge of $\overline{CS}$. It is important to ensure that the SCK pin is driven LOW during the $\overline{CS}$ falling edge.

The end of conversion can be detected by testing the SDO pin. Anytime during the Conversion or Sleep states the SDO can be observed after $\overline{CS}$ is driven LOW. If SDO = HIGH the conversion is not yet completed. If SDO = LOW a new result is available and the Data Output state can be initiated at any time.

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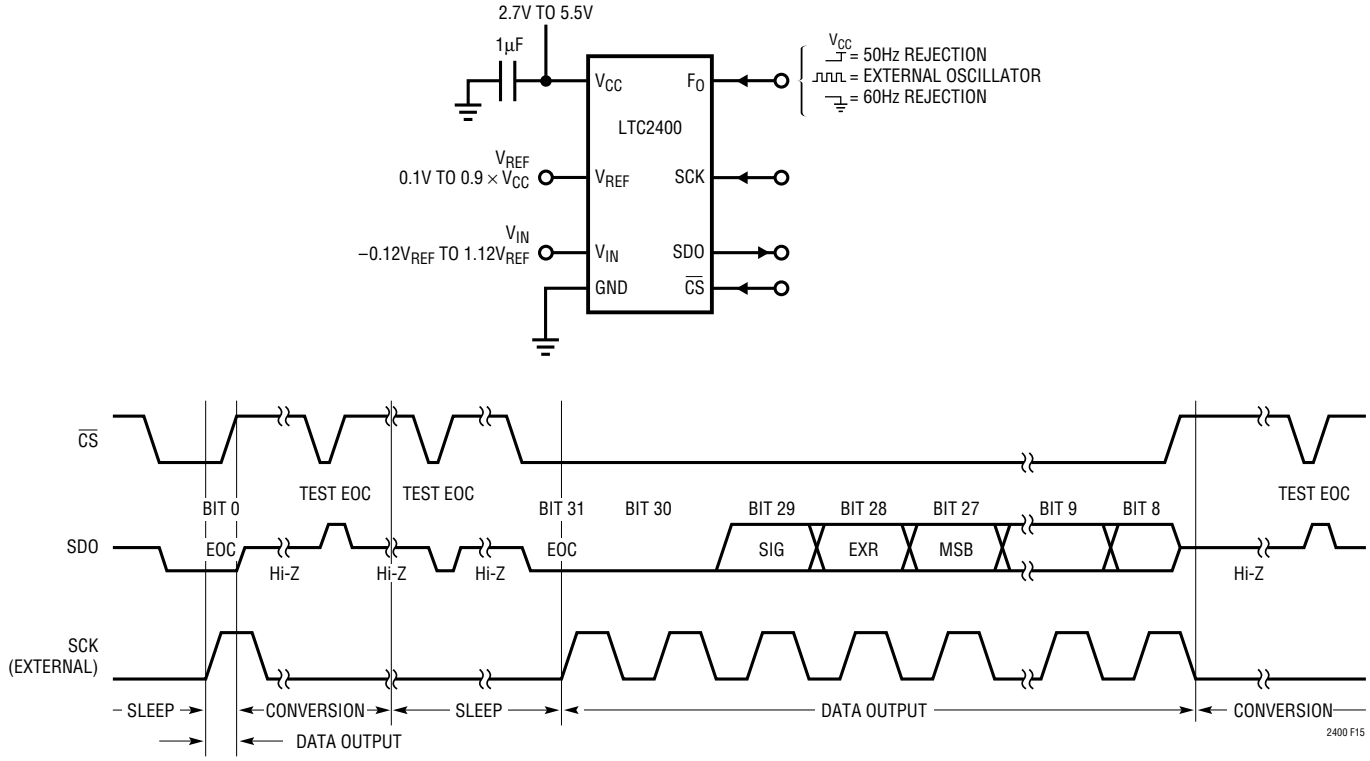
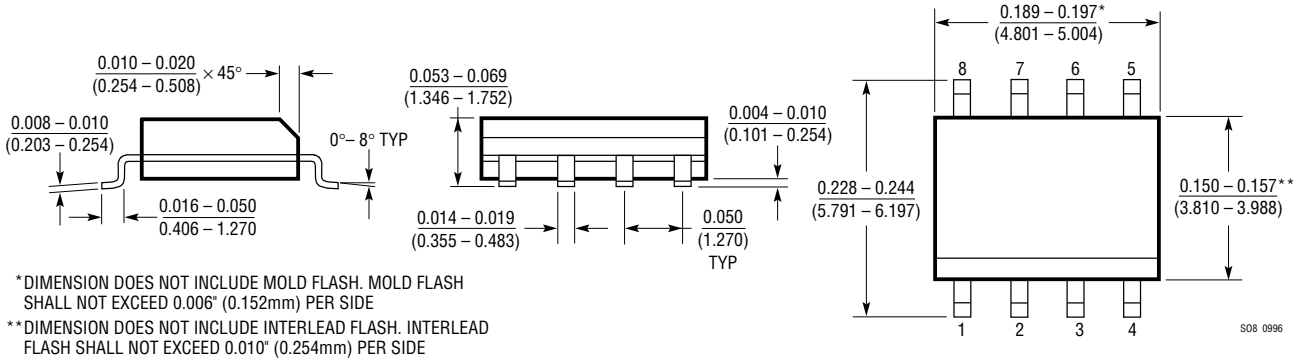


Figure 15. External Serial Clock, Reduced Data Output Length

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1460	Micropower Series Reference	0.075% Max, 10ppm/°C Max Drift, 2.5V, 5V and 10V Versions, MSOP, PDIP, SO-8, SOT-23 and TO-92 Packages
LT1236A-5	Precision Bandgap Reference, 5V	0.05% Max, 5ppm/°C Drift

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