CMOS IC

LC72321N, 72322N, 72323N

Single-Chip Microcontrollers with Built-in LCD Driver and PLL Circuits

Overview

The LC72321N, LC72322N, and LC72323N are single-chip microcontrollers designed for electronic tuning in radio receivers and include an on-chip LCD driver circuit and a PLL circuit that operates at 150 MHz. These microcontrollers feature a large program ROM capacity, an efficient instruction set, and powerful hardware. Note that the LC72321N, LC72322N, and LC72323N provide functions equivalent to the LC72321, LC72322, and LC72323, and are software compatible with those products.

Functions

- Serial I/O (LC72321N only)
- Timers: 80 μs, 1 ms, 2 ms, and 5 ms periods
- Stack levels: 8 levels
- Beep tone outputs:
  Six frequencies (2.08, 2.25, 2.5, 3.0, 3.75, and 4.17 kHz) (LC72321N only)
- High-speed programmable divider
- General-Purpose counters
  HCTR: Frequency measurement
  LCTR: Frequency or period measurement
- LCD drive circuit: Drives 56 segments with 1/2-duty 1/2-bias drive
- Program memory (ROM):
  16 bits × 4095 words (8K bytes) LC72321N and LC72322N
  16 bits × 3071 words (6K bytes) LC72323N
- Data memory (RAM): 4 bits × 256 words
- All instructions are single-word instructions.

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- Cycle times: 2.67 μs, 13.33 μs, or 40.00 μs (option)
- Unlock flip-flop: 0.55 μs and 1.1 μs detection
- Timer flip-flop: 1 ms, 5 ms, 25, ms, and 125 ms
- Input ports*: One dedicated key input port, and one high-voltage port
- Output ports*:
  Two dedicated key output ports, one high-voltage open-drain port
  Two CMOS output ports (one of which can be switched over to function as an LCD driver output)
  Seven CMOS output ports (Switching these ports over to function as LCD driver outputs is supported as an option.)
- I/O ports*:
  One port switchable between input and output in 4-bit units
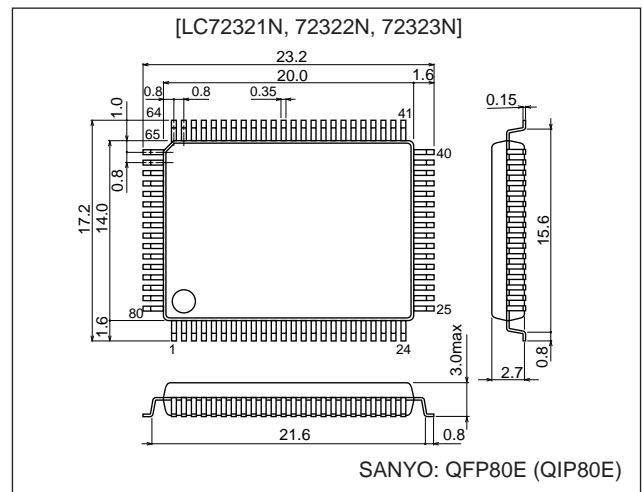 One port switchable between input and output in 1-bit units

*: Each port consists of 4 bits.

Package Dimensions

unit: mm

3174-QFP80E

[LC72321N, 72322N, 72323N]

SANYO: QFP80E (QIP80E)

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- Function that detects uncontrolled looping and jumps to a specified address
- Voltage detection reset circuit
- One 6-bit A/D converter
- Two 8-bit A/D converters (PWM) (LC72321N and LC72322N only)
- One external interrupt (The external interrupt can be selected to be one of the following: an external interrupt,

an internal timer interrupt, or the serial I/O circuit (in the LC72321N).)

- RAM data retention in hold mode
- Sensing flip-flop for hot/cold start discrimination
- PLL: 4.5 to 5.5 V
- CPU: 3.5 to 5.5 V
- RAM: 1.3 to 5.5 V

Pin Assignment
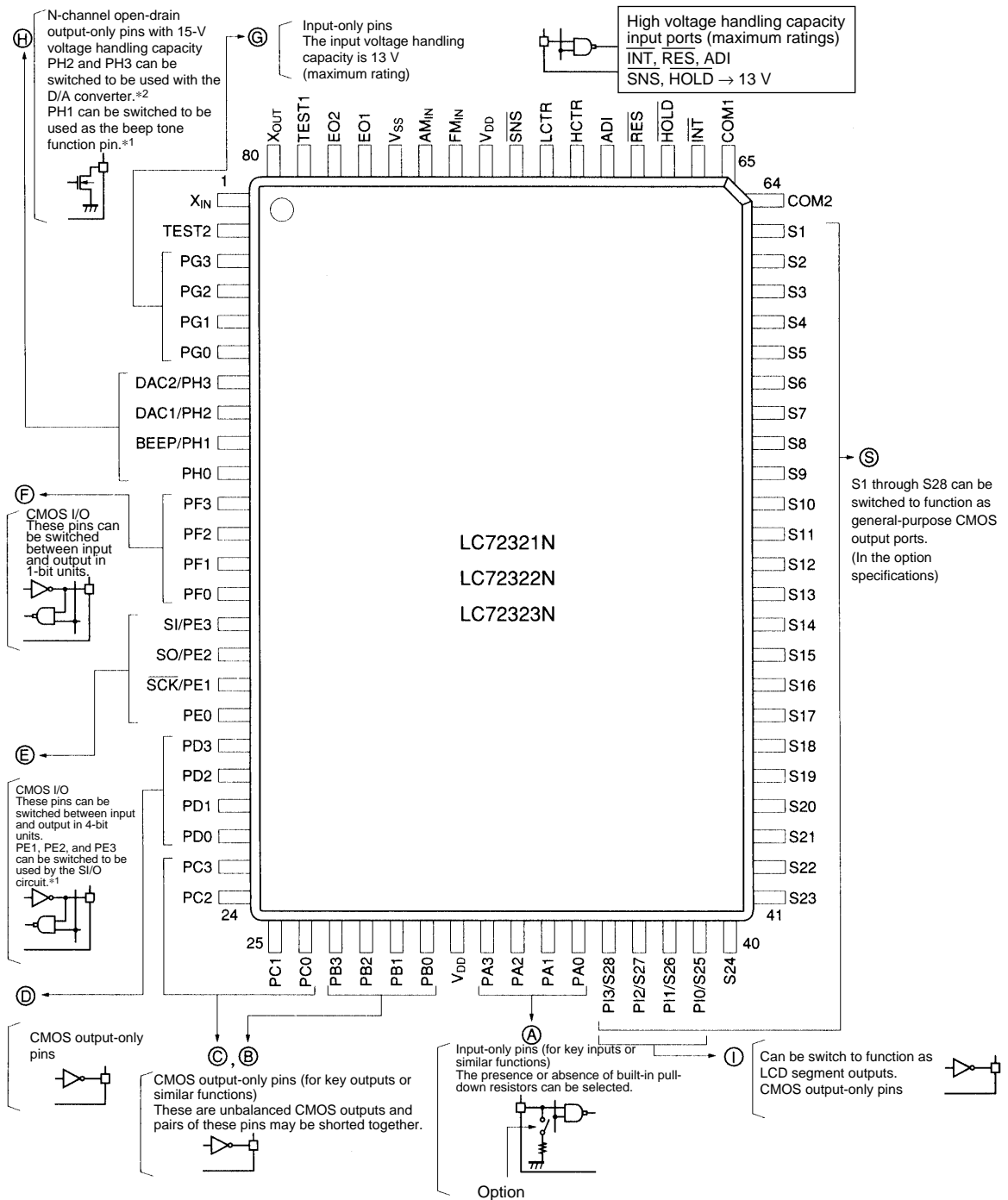
Notes: *1. Only possible with the LC72321N
*2. Only possible with the LC72321N and LC72322N

Block Diagram
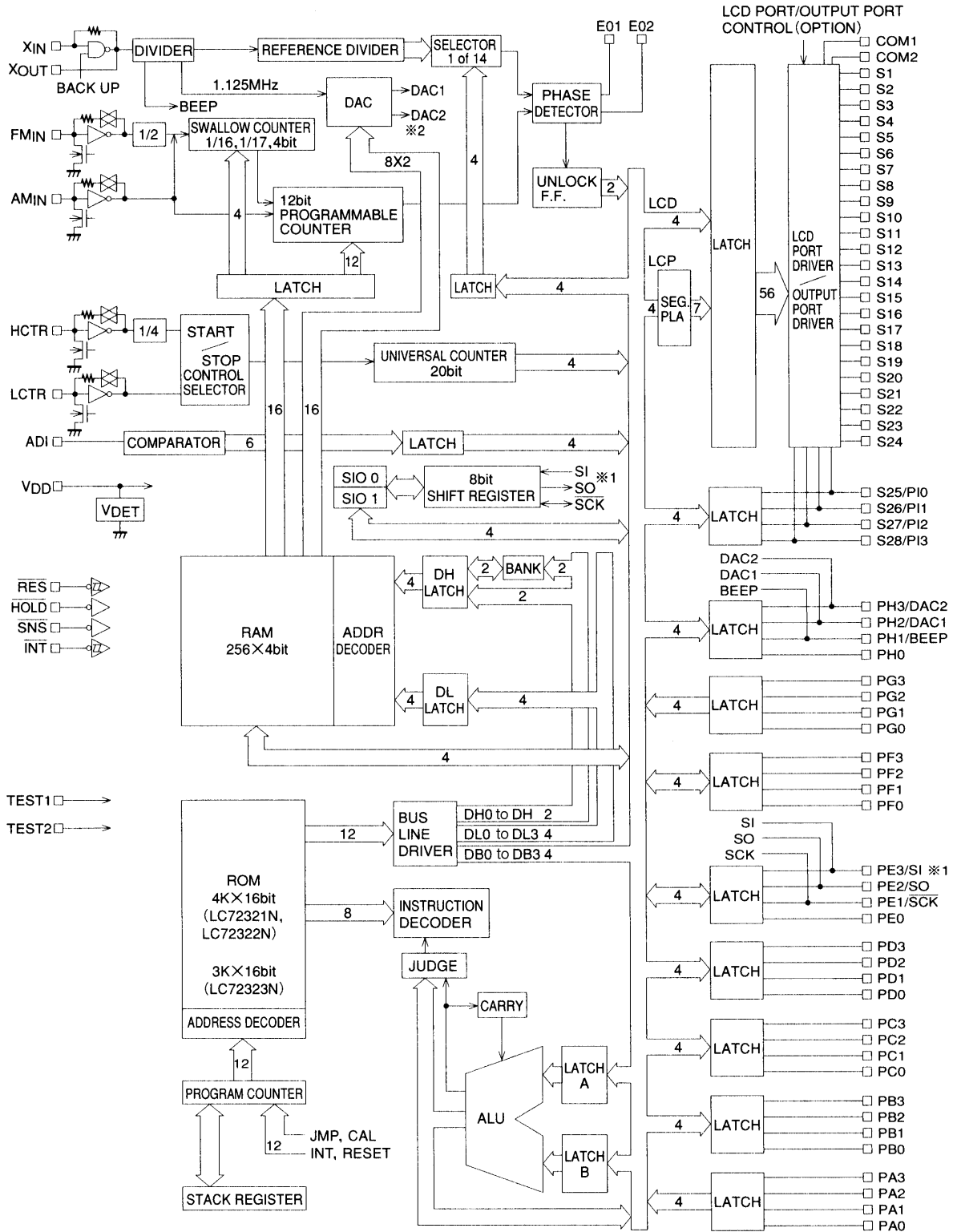
Notes:*1. Only possible with the LC72321N
*2. Only possible with the LC72321N and LC72322N

Specifications

Absolute Maximum Ratings at $Ta = 25°C$, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	Rating	Unit
Maximum supply voltage	V_{DD} max		−0.3 to +6.5	V
Input voltage	$V_{IN}1$	$\overline{HOLD}$, $\overline{INT}$, $\overline{RES}$, ADI, $\overline{SNS}$ Port G	−0.3 to +13	V
	$V_{IN}2$	Inputs other than $V_{IN}1$	−0.3 to V_{DD} + 0.3	V
Output voltage	$V_{OUT}1$	Port H	−0.3 to +15	V
	$V_{OUT}2$	Outputs other than $V_{OUT}1$	−0.3 to V_{DD} + 0.3	V
Output current	$I_{OUT}1$	All the port D and H pins	0 to 5	mA
	$I_{OUT}2$	All the port E and F pins	0 to 3	mA
	$I_{OUT}3$	All the port B and C pins	0 to 1	mA
	$I_{OUT}4$	S1 to S28 and port I	0 to 1	mA
Allowable power dissipation	Pd max	$Ta = −40$ to +85°C	300	mW
Operating temperature	Topr		−40 to +85	°C
Storage temperature	Tstg		−45 to +125	°C

Allowable Operating Ranges at $Ta = –40$ to $+85°C$, $V_{DD} = 3.5$ to 5.5 V

Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
Supply voltage	$V_{DD}1$	CPU and PLL operating	4.5		5.5	V
	$V_{DD}2$	CPU operating	3.5		5.5	V
	$V_{DD}3$	Memory retention	1.3		5.5	V
High-level input voltage	$V_{IH}1$	Port G	$0.7 V_{DD}$		8.0	V
	$V_{IH}2$	$\overline{RES}$, $\overline{INT}$, $\overline{HOLD}$	$0.8 V_{DD}$		8.0	V
	$V_{IH}3$	$\overline{SNS}$	2.5		8.0	V
	$V_{IH}4$	Port A	$0.6 V_{DD}$		V_{DD}	V
	$V_{IH}5$	Ports E and F	$0.7 V_{DD}$		V_{DD}	V
	$V_{IH}6$	LCTR (period measurement), $V_{DD}1$, PE1, and PE3	$0.8 V_{DD}$		V_{DD}	V
Low-level input voltage	$V_{IL}1$	Port G	0		$0.3 V_{DD}$	V
	$V_{IL}2$	$\overline{RES}$, $\overline{INT}$, PE1, PE3	0		$0.2 V_{DD}$	V
	$V_{IL}3$	$\overline{SNS}$	0		1.3	V
	$V_{IL}4$	Port A	0		$0.2 V_{DD}$	V
	$V_{IL}5$	PE0, PE2, and port F	0		$0.3 V_{DD}$	V
	$V_{IL}6$	LCTR (period measurement) and $V_{DD}1$	0		$0.2 V_{DD}$	V
	$V_{IL}7$	$\overline{HOLD}$	0		$0.4 V_{DD}$	V
Input frequency	$f_{IN}1$	XIN	4.0	4.5	5.0	MHz
	$f_{IN}2$	FMIN, $V_{IN}2$, $V_{DD}1$	10		130	MHz
	$f_{IN}3$	FMIN, $V_{IN}3$, $V_{DD}1$	10		150	MHz
	$f_{IN}4$	AMIN (L), $V_{IN}4$, $V_{DD}1$	0.5		10	MHz
	$f_{IN}5$	AMIN (H), $V_{IN}5$, $V_{DD}1$	2.0		40	MHz
	$f_{IN}6$	HCTR, $V_{IN}6$, $V_{DD}1$	0.4		12	MHz
	$f_{IN}7$	LCTR (frequency), $V_{IN}7$, and $V_{DD}1$	100		500	kHz
	$f_{IN}8$	LCTR (period), $V_{IH}6$, $V_{IL}6$, and $V_{DD}1$	1		20×10^3	Hz
Input amplitude	$V_{IN}1$	XIN	0.50		1.5	Vrms
	$V_{IN}2$	FMIN	0.10		1.5	Vrms
	$V_{IN}3$	FMIN	0.15		1.5	Vrms
	$V_{IN}4, 5$	AMIN	0.10		1.5	Vrms
	$V_{IN}6, 7$	LCTR, HCTR	0.10		1.5	Vrms
Input voltage range	$V_{IN}8$	ADI	0		V_{DD}	V

### Electrical Characteristics in the Allowable Operating Ranges

Parameter	Symbol	Conditions	min	typ	max	Unit
				Ratings		
Hysteresis	V_H	LCTR(period), $\overline{RES}$, $\overline{INT}$, PE1, PE3　　　　0.1 V_{DD}			V	
Rejected pulse width	P_{REJ}	$\overline{SNS}$			50	µs
Power down detection voltage	V_{DET}		2.7	3.0	3.3	V
High-level input current	$I_{IH}1$	$\overline{INT}$, $\overline{HOLD}$, $\overline{RES}$, ADI, $\overline{SNS}$, port G: $V_I = 5.5$ V			3.0	µA
	$I_{IH}2$	Ports A, E, and F: with ports E and F set to output off, with the port A R_{PD} disabled, $V_I = V_{DD}$			3.0	µA
	$I_{IH}3$	XIN: $V_I = V_{DD} = 5.0$ V	2.0	5.0	15	µA
	$I_{IH}4$	FMIN, AMIN, HCTR, LCTR: $V_I = V_{DD} = 5.0$ V	4.0	10	30	µA
	$I_{IH}5$	Port A: R_{PD} enabled, $V_I = V_{DD} = 5.0$ V		50		µA
Low-level input current	$I_{IL}1$	$\overline{INT}$, $\overline{HOLD}$, $\overline{RES}$, ADI, $\overline{SNS}$, port G: $V_I = V_{SS}$			3.0	µA
	$I_{IL}2$	Ports A, E, and F: with ports E and F set to output off, with the port A R_{PD} disabled, $V_I = V_{SS}$			3.0	µA
	$I_{IL}3$	XIN: $V_{IN} = V_{SS}$	2.0	5.0	15	µA
	$I_{IL}4$	FMIN, AMIN, HCTR, LCTR: $V_I = V_{SS}$	4.0	10	30	µA
Input floating voltage	V_{IF}	Port A: R_{PD} enabled			0.05 V_{DD}	V
Pull-down resistance	R_{PD}	Port A: R_{PD} enabled, $V_{DD} = 5.0$ V	75	100	200	kΩ
High-level output off leakage current	$I_{OFFH}1$	EO1, EO2: $V_O = V_{DD}$		0.01	10	nA
	$I_{OFFH}2$	Ports B, C, D, E, F, and I: $V_O = V_{DD}$			3.0	µA
	$I_{OFFH}3$	Port H: $V_O = 13$ V			5.0	µA
Low-level output off leakage current	$I_{OFFL}1$	EO1, EO2: $V_O = V_{SS}$		0.01	10	nA
	$I_{OFFL}2$	Ports B, C, D, E, F, and I: $V_O = V_{SS}$			3.0	µA
High-level output voltage	$V_{OH}1$	Ports B and C: $I_O = 1$ mA	$V_{DD} - 2.0$	$V_{DD} - 1.0$	$V_{DD} - 0.5$	V
	$V_{OH}2$	Ports E and F: $I_O = 1$ mA	$V_{DD} - 1.0$			V
	$V_{OH}3$	EO1, EO2: $I_O = 500$ µA	$V_{DD} - 1.0$			V
	$V_{OH}4$	XOUT: $I_O = 200$ µA	$V_{DD} - 1.0$			V
	$V_{OH}5$	S1 to S28 and port I: $I_O = -0.1$ mA	$V_{DD} - 1.0$			V
	$V_{OH}6$	Port D: $I_O = 5$ mA	$V_{DD} - 1.0$			V
	$V_{OH}7$	COM1, COM2: $I_O = 25$ µA	$V_{DD} - 0.75$	$V_{DD} - 0.5$	$V_{DD} - 0.3$	V
Low-level output voltage	$V_{OL}1$	Ports B and C: $I_O = 50$ µA	0.5	1.0	2.0	V
	$V_{OL}2$	Ports E and F: $I_O = 1$ mA			1.0	V
	$V_{OL}3$	EO1, EO2: $I_O = 500$ µA			1.0	V
	$V_{OL}4$	XOUT: $I_O = 200$ µA			1.0	V
	$V_{OL}5$	S1 to S28 and port I: $I_O = 0.1$ mA			1.0	V
	$V_{OL}6$	Port D: $I_O = 5$ mA			1.0	V
	$V_{OL}7$	COM1, COM2: $I_O = 25$ µA	0.3	0.5	0.75	V
	$V_{OL}8$	Port H: $I_O = 5$ mA	(150 Ω) 0.75		(400 Ω) 2.0	V
Output middle level voltage A/D converter error	$V_{M}1$	COM1, COM2: $V_{DD} = 5.0$ V, $I_O = 20$ µA	2.0	2.5	3.0	V
		ADI: $V_{DD}1$	$-1/2$		$+1/2$	LSB
Current drain	$I_{DD}1$	$V_{DD}1$, $f_{IN}2 = 130$ MHz		15	20	mA
	$I_{DD}2$	$V_{DD}2$, PLL circuit stopped, CT = 2.67 µs (hold mode, see figure 1)		1.5		mA
	$I_{DD}3$	$V_{DD}2$, PLL circuit stopped, CT = 13.33 µs (hold mode, see figure 1)		1.0		mA
	$I_{DD}4$	$V_{DD}2$, PLL circuit stopped, CT = 40.00 µs (hold mode, see figure 1)		0.7		mA
	$I_{DD}5$	$V_{DD} = 5.5$ V, oscillator circuit stopped, Ta = 25°C (backup mode, see figure 2)			5	µA
		$V_{DD} = 2.5$ V, oscillator circuit stopped, Ta = 25°C (backup mode, see figure 2)			1	µA

Test Circuit Diagrams
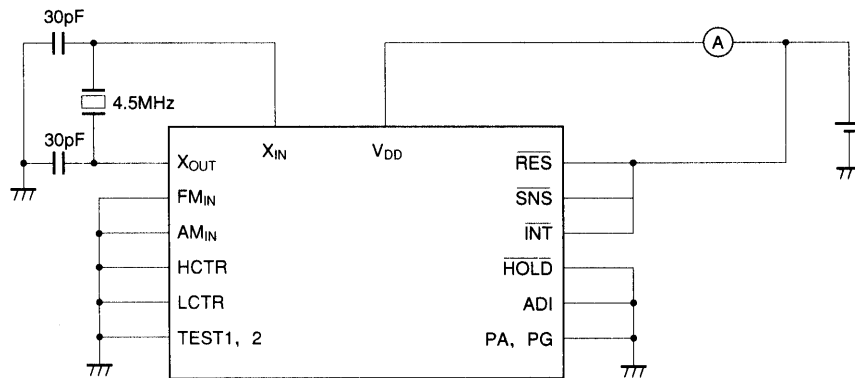
Note: PB to PF, PH, and PI must all be left open. However, PE and PF should be selected for output.

Figure 1 $I_{DD}2$ to $I_{DD}4$ in Hold Mode
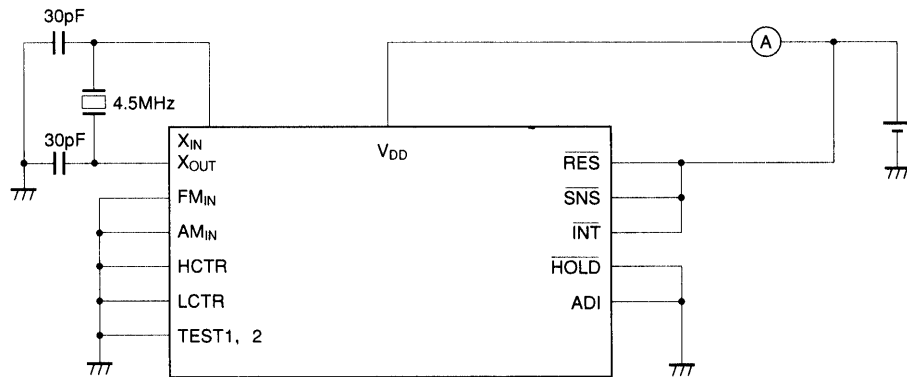
Note: PA to PI, S1 to S24, COM1, and COM2 must all be left open.

Figure 2 $I_{DD}5$ in Backup Mode

Pin Function

Pin No.	Pin	Description	I/O	I/O circuit
35 34 33 32	PA0 PA1 PA2 PA3	Low-threshold input-only port. Can be used for functions such as key data acquisition. Pull-down resistors can be specified as an option. This option is specified in a 4-pin unit, and cannot be specified in single pin units. Input is disabled in backup mode.	Input	BACK UP Option
30 29 28 27 26 25 24 23	PB0 PB1 PB2 PB3 PC0 PC1 PC2 PC3	Output-only ports. Since the output transistor circuits are unbalanced CMOS outputs, these outputs can be effectively used for functions such as key scan timing. These ports go to the high-impedance state in backup mode. These ports output a low level after a reset (when $\overline{RES}$ is set low).	Output	BACK UP
22 21 20 19	PD0 PD1 PD2 PD3	Output-only port. These are normal CMOS outputs. This port goes to the high-impedance state in backup mode. This port outputs a low level after a reset (when $\overline{RES}$ is set low).		
18 17 16 15	PE0 PE1/$\overline{SCK}$ PE2/SO PE3/SI	I/O port. The input/output state is selected as follows: Once an input instruction (IN, TPT, or TPF) is executed, the port switches to the input state and remains in that state. Once an output instruction (OUT, SPB, RPB) is executed, the port switches to the output state and remains in that state. Note that PE1, PE2, and PE3 are also used as the serial I/O port. These pins go to the input state after a reset. This port goes to the input state with input disabled in backup mode.	I/O	PE1,PE3 BACK UP Other pins BACK UP
14 13 12 11	PF0 PF1 PF2 PF3	I/O port. The FPC instruction is used for switching the port function between input and output. Input or output can be specified in single pin units. This port is set to its input function after a reset. This port goes to the input state with input disabled in backup mode.		
6 5 4 3	PG0 PG1 PG2 PG3	Input-only port. Input is disabled in backup mode.	Input	BACK UP

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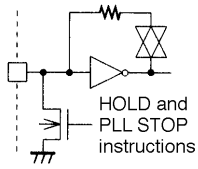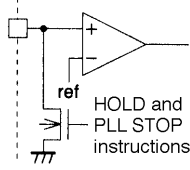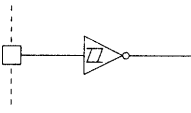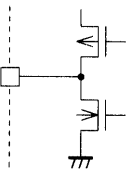
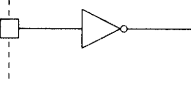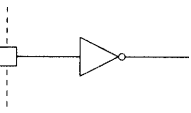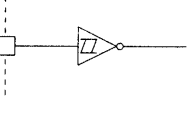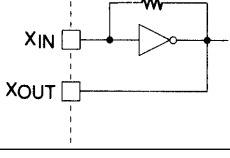| Pin No.	Pin	Description	I/O	I/O circuit
10 9 8 7	PH0 PH1/BEEP*1 PH2/DAC1*2 PH3/DAC2*2	Output-only port. Since these ports are high-voltage handling n-channel transistor open-drain outputs, they are effective for use in band power supply switching. Note that PH1, PH2, and PH3 have shared functions as the BEEP*1, DAC1, and DAC2 outputs, respectively.*2 This port goes to the high-impedance state in backup mode and after a reset (when the $\overline{\text{RES}}$ pin is set low).	Output	
39 38 37 36	PI0/S25 PI1/S26 PI2/S27 PI3/S28	Output-only port. These pins are CMOS outputs, but can be switched to function as LCD driver outputs. The SS and RS instructions are used to switch the port function. The port function cannot be switched in single pin units. The LCD driver function is selected and a display off signal is output when $\overline{\text{RES}}$ is low and when power is first applied. In backup mode the output is held at the low level. Note that when use as a general-purpose port is specified as an option, the contents of IPORT are output when LPC is 1, and the contents of the general-purpose output port latch is are output when LPC is 0.	Output	
63 to 40	S1 to S24	LCD driver segment outputs. The fame frequency is 100 Hz. The drive type is 1/2-duty 1/2-bias drive. A display off signal is output when $\overline{\text{RES}}$ is low and when power is first applied. In backup mode the outputs are held at the low level. An option is available that allows these pins to be used as general-purpose outputs.	Output	
65 64	COM1 COM2	LCD driver common outputs. The drive type is 1/2-duty 1/2-bias drive. These pins output the same signal as is output during normal operation when $\overline{\text{RES}}$ is low and when power is first applied. In backup mode these outputs are held at the low level.	Output	
74	FM IN	FM VCO (local oscillator) input. Input must be supplied through a coupling capacitor. The input frequency range is 10 to 130 MHz.	Input	
75	AM IN	AM VCO (local oscillator) input. Input must be supplied through a coupling capacitor. The pin frequency band can be selected with the PLL instruction CW1 bit. High (2 to 40 MHz) → SW Low (0.5 to 10 MHz) → LW and MW		

Notes: *1. Only supported by the LC72321N
  *2. Only supported by the LC72321N and LC72322N

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| Pin No.	Pin	Description	I/O	I/O circuit
70	HCTR	Universal counter input. Input must be supplied through a coupling capacitor. The input frequency range is 0.4 to 12 MHz This pin can be used effectively for FM IF or AM IF counting.	Input	HOLD and PLL STOP instructions
71	LCTR	Universal counter input. Input must be supplied through a coupling capacitor when the input frequency is in the range 100 to 500 kHz. No input coupling capacitor is required when the input frequency is in the range 1 Hz to 20 kHz. This pin can be used effectively for AM IF counting. This pin can also be used as a normal input port.		
69	ADI	A/D converter input. This converter requires 1.28 ms to perform a 6-bit sequential comparison conversion. Full scale (a data value of 3F (hexadecimal)) corresponds to (63/96) time V_{DD}.	Input	ref HOLD and PLL STOP instructions
66	$\overline{INT}$	External interrupt request input. An interrupt occurs when the INTEN flag is set with the SS instruction and a falling edge is input. This pin can also be used as a normal input port.	Input	
77 78	EO1 EO2	These pins are used as the reference frequency output and the phase comparator error output for the programmable divider. A charge pump circuit is built in. EO1 and EO2 are the same.	Output	
72	$\overline{SNS}$	Input used to recognize power failures when the IC is in backup mode. This pin can also be used as a normal input port.	Input	
67	$\overline{HOLD}$	Input used to set the IC to hold mode. The IC switches to hold mode when the HOLDEN flag is set with the SS instruction and the $\overline{HOLD}$ pin is set low. A high-voltage handling circuit is used so that this pin can be linked to the power switch in typical systems.	Input	
68	$\overline{RES}$	System reset input. Applications must hold this input low for at least 75 ms to effect a power on reset. To start a reset, this pin must be held low for a full 6 base clock cycles.	Input	
1 80	XIN XOUT	Crystal oscillator connections (4.5 MHz) Feedback resistors are built in.	Input Output	X_{IN} X_{OUT}
2 79	TEST1 TEST2	IC test pins. These pins must be either left open or connected to V_{SS}.	—	—
31, 73 76	V_{DD} V_{SS}	Power supply	—	—

Mask Options

Option	Selections
WDT (watchdog timer) selection	WDT present
	WDT absent
Port A (key input port) pull-down resistor selection	Pull-down resistors enabled
	Pull-down resistors disabled
Cycle time selection (3 options)	2.67 μs
	13.33 μs
	40.00 μs
Switching of the LCD segment driver pins to function as general-purpose output ports	LCD ports
	General-purpose output ports

Development Environment

- The LC72P321 is used as the OTP version.
- The LC72EV321 is used as the evaluation chip.
- A total debugging system is available in which an evaluation board (TB-72EV32) and a multi-function emulator (RE32) are controlled by a personal computer.
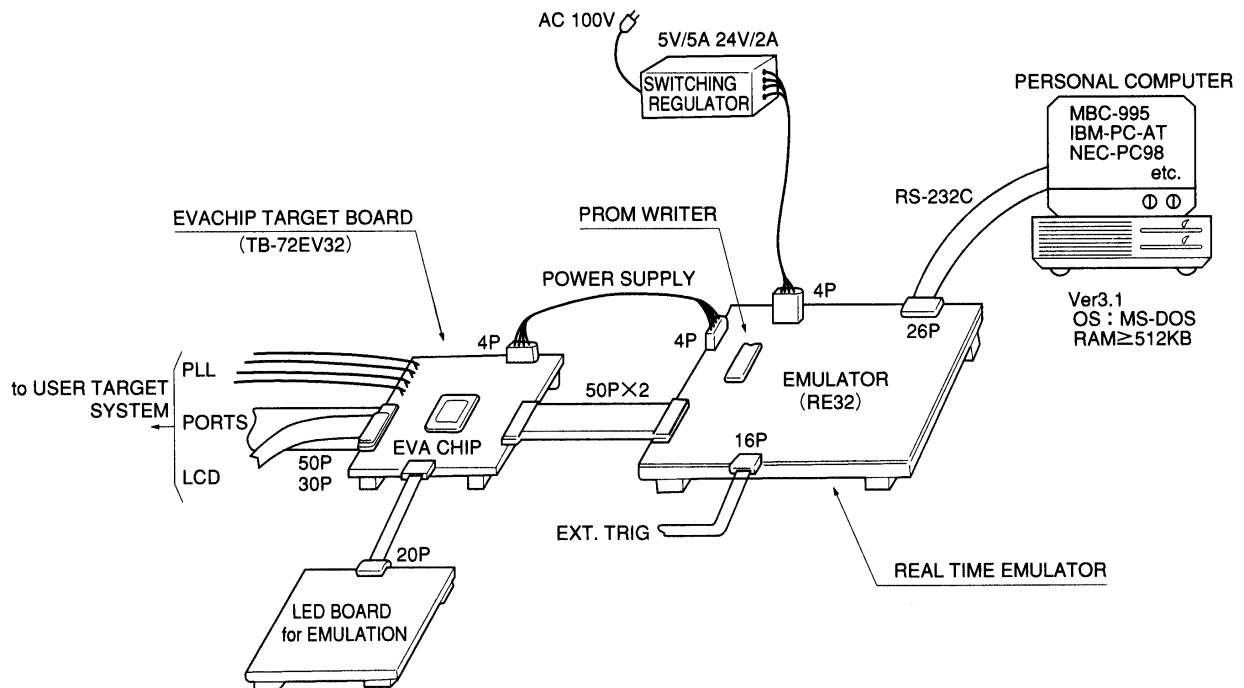
LC72321N, LC72322N, and LC72323N Instruction Set

Abbreviations:
ADDR : Program memory address [12 bits]
b : Borrow
B : Bank number [2 bits]
C : Carry
DH : Data memory address high (Row address) [2 bits]
DL : Data memory address low (Column address) [4 bits]
I : Immediate data [4 bits]
M : Data memory address
N : Bit position [4 bits]
Pn : Port number [4 bits]
r : General register (One of the locations 00 to 0FH in bank 0)
( ) : Contents of register or memory
( )N : Contents of bit N of register or memory

Instruction group	Mnemonic	Operands 1st	Operands 2nd	Function	Operation	Machine code D15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 D0
Addition instructions	AD	r	M	Add M to r	$r \leftarrow (r) + (M)$	0 1 0 0	0 0 DH	DL	Rn
	ADS	r	M	Add M to r, then skip if carry	$r \leftarrow (r) + (M)$ skip if carry	0 1 0 0	0 1 DH	DL	Rn
	AC	r	M	Add M to r with carry	$r \leftarrow (r) + (M) + C$	0 1 0 0	1 0 DH	DL	Rn
	ACS	r	M	Add M to r with carry then skip if carry	$r \leftarrow (r) + (M) + C$ skip if carry	0 1 0 0	1 1 DH	DL	Rn
	AI	M	I	Add I to M	$M \leftarrow (M) + I$	0 1 0 1	0 0 DH	DL	I
	AIS	M	I	Add I to M, then skip if carry	$M \leftarrow (M) + I$ skip if carry	0 1 0 1	0 1 DH	DL	I
	AIC	M	I	Add I to M with carry	$M \leftarrow (M) + I + C$	0 1 0 1	1 0 DH	DL	I
	AICS	M	I	Add I to M with carry, then skip if carry	$M \leftarrow (M) + I + C$ skip if carry	0 1 0 1	1 1 DH	DL	I
Subtraction instructions	SU	r	M	Subtract M from r	$r \leftarrow (r) - (M)$	0 1 1 0	0 0 DH	DL	Rn
	SUS	r	M	Subtract M from r, then skip if borrow	$r \leftarrow (r) - (M)$ skip if carry	0 1 1 0	0 1 DH	DL	Rn
	SB	r	M	Subtract M from r with borrow	$r \leftarrow (r) - (M) - b$	0 1 1 0	1 0 DH	DL	Rn
	SBS	r	M	Subtract M from r with borrow, then skip if borrow	$r \leftarrow (r) - (M) - b$ skip if borrow	0 1 1 0	0 0 DH	DL	Rn
	SI	M	I	Subtract I from M	$M \leftarrow (M) - I$	0 1 1 1	0 0 DH	DL	I
	SIS	M	I	Subtract I from M, then skip if borrow	$M \leftarrow (M) - I$ skip if borrow	0 1 1 1	0 1 DH	DL	I
	SIB	M	I	Subtract I from M with borrow	$M \leftarrow (M) - I - b$	0 1 1 1	1 0 DH	DL	I
	SIBS	M	I	Subtract I from M with borrow, then skip if borrow	$M \leftarrow (M) - I - b$ skip if borrow	0 1 0 1	1 1 DH	DL	I
Comparison instructions	SEQ	r	M	Skip if r equals M	$r \leftarrow M$ skip if zero	0 0 0 0	0 1 DH	DL	Rn
	SGE	r	M	Skip if r is greater than or equal to M	$r \leftarrow M$ skip if not borrow $(r) \geq (M)$	0 0 0 0	1 1 DH	DL	Rn
	SEQI	M	I	Skip if M equal to I	$M - I$ skip if zero	0 0 1 1	0 1 DH	DL	I
	SGEI	M	I	Skip if M is greater then or equal to I	$M - I$ skip if not borrow $(M) \geq I$	0 0 1 1	1 1 DH	DL	I

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Instruction group	Mnemonic	Operands 1st	Operands 2nd	Function	Operation	Machine code D15 14 13 12	11 10	9 8	7 6 5 4	3 2 1 D0
Logical operation instructions	AND	M	I	AND I with M	M ← (M) ∧ I	0 0 1 1	0 0	DH	DL	I
	OR	M	I	OR I with M	M ← (M) ∧ I	0 0 1 1	1 0	DH	DL	I
	EXL	r	M	Exclusive OR M with r	r ← (r) ⊕ (M)	0 0 1 0	0 0	DH	DL	Rn
Transfer instructions	LD	r	M	Load M to r	r ← (M)	1 0 0 0	0 0	DH	DL	Rn
	ST	M	r	Store r to M	M ← (r)	1 0 0 0	0 1	DH	DL	Rn
	MVRD	r	M	Move M to destination M referring to r in the same row	(DH, Rn) ← (M)	1 0 0 0	1 0	DH	DL	Rn
	MVRS	M	r	Move source M referring to r to M in the same row	M ← (DH, Rn)	1 0 0 0	1 1	DH	DL	Rn
	MVSR	M1	M2	Move M to M in the same row	(DH, DL1) ← (DH, DL2)	1 0 0 1	0 0	DH	DL1	DL2
	MV1	M	I	Move I to M	M ← I	1 0 0 1	0 1	DH	DL	I
	PLL	M	r	Load M to PLL registers	PLL r ← PLL DATA	1 0 0 1	1 0	DH	DL	Rn
Bit test instructions	TMT	M	N	Test M bits, then skip if all bits specified are true	if M (N) = all 1, then skip	1 0 1 0	0 1	DH	DL	N
	TMF	M	N	Test M bits, then skip if all bits specified are false	if M (N) = all 0, then skip	1 0 1 0	1 1	DH	DL	N
Jump and subroutine instructions	JMP	ADDR		Jump to the address	PC ← ADDR	1 0 1 1	ADDR (12 bits)			
	CAL	ADDR		Call subroutine	Stack ← (PC) + 1	1 1 0 0	ADDR (12 bits)			
	RT			Return from subroutine	PC ← Stack	1 1 0 1	0 1 0 0		0 0 0 0	0 0 0 0
	RTI			Return from interrupt	PC ← Stack BANK ← Stack CARRY ← Stack	1 1 0 1	0 1 0 1		0 0 0 0	0 0 0 0
Flip-flop test instructions	TTM	N		Test timer F/F then skip if it has not been set	if timer F/F = 0, then skip	1 1 0 1	0 1 1 0		0 0 0 0	N
	TUL	N		Test unlock F/F then skip if it has not been set	if UL F/F = 0, then skip	1 1 0 1	0 1 1 1		0 0 0 0	N
Status register instructions	SS	N		Set status register	(Status register 1) N ← 1	1 1 0 1	1 1 0 0		0 0 0 0	N
	RS	N		Reset status register	(Status register 1) N ← 0	1 1 0 1	1 1 0 1		0 0 0 0	N
	TST	N		Test status register true	if (Status register 2) N = all 1, then skip	1 1 0 1	1 1 1 0		0 0 0 0	N
	TSF	N		Test status register false	if (Status register 2) N = all 0, then skip	1 1 0 1	1 1 1 1		0 0 0 0	N
Bank switching instructions	BANK	B		Select Bank	BANK ← B	1 1 0 1	0 0	B	0 0 0 0	0 0 0 0

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Instruction group	Mnemonic	Operands		Function	Operation	Machine code			
		1st	2nd			D15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 D0
I/O instructions	LCD	M	I	Output segment pattern to LCD digit direct	LCD (DIGIT) ← M	1 1 1 0	0 0 DH	DL	DIGIT
	LCP	M	I	Output segment pattern to LCD digit through PLA	LCD (DIGIT) ← PLA ← M	1 1 1 0	0 1 DH	DL	DIGIT
	IN	M	P	Input port data to M	M ← (Port (P))	1 1 1 0	1 0 DH	DL	P
	OUT	M	P	Output contents of M to port	(Port (P)) ← M	1 1 1 0	1 1 DH	DL	P
	SPB	P	N	Set port bits	(Port (P)) N ← 1	1 1 1 1	0 0 0 0	P	N
	RPB	P	N	Reset port bits	(Port (P)) N ← 0	1 1 1 1	0 1 0 1	P	N
	TPT	P	N	Test port bits, then skip if all bits specified are true	if (Port (P)) N = all 1, then skip	1 1 1 1	1 0 1 0	P	N
	TPF	P	N	Test port bits, then skip if all bits specified are false	if (Port (P)) N = all 0, then skip	1 1 1 1	1 1 1 1	P	N
Universal counter instructions	UCS	I		Set I to UCCW1	UCCW1 ← I	0 0 0 0	0 0 0 1	0 0 0 0	I
	UCC	I		Set I to UCCW2	UCCW2 ← I	0 0 0 0	0 0 1 1	0 0 0 0	I
Other instructions	FPC	N		F port I/O control	FPC Latch ← N	0 0 0 1	0 0 0 0	0 0 0 0	N
	CKSTP			Clock stop	Stop clock if $\overline{HOLD}$ = 0	0 0 0 1	0 0 0 1	0 0 0 0	0 0 0 0
	DAC	I		Load M to D/A registers	DAreg ← DAC DATA	0 0 0 0	0 0 1 0	0 0 0 0	I
	SIO	I1	I2	Serial I/O control	SIOCW ← I1, I2	0 0 0 1	0 0 1 1	I1	I2
	SIOL	M	I	Load SIOreg to M	M ← SIOreg	0 0 0 1	1 0 DH	DL	I
	SIOS	M	I	Store M to SIOreg	SIOreg ← M	0 0 0 1	0 1 DH	DL	I
	BEEP	I		Beep control	BEEPreg ← I	0 0 0 1	0 0 1 0	0 0 0 0	I
	NOP			No operation		0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0