



# FAST CMOS 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

**IDT74FCT16601AT/CT**

## FEATURES:

- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- Low input and output leakage  $\leq 1\mu A$  (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 5V \pm 10\%$
- High drive outputs (-32mA  $I_{OH}$ , 64mA  $I_{OL}$ )
- Power off disable outputs permit "live insertion"
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1.0V at  $V_{cc} = 5V$ ,  $T_A = 25^\circ C$
- Available in SSOP and TSSOP packages

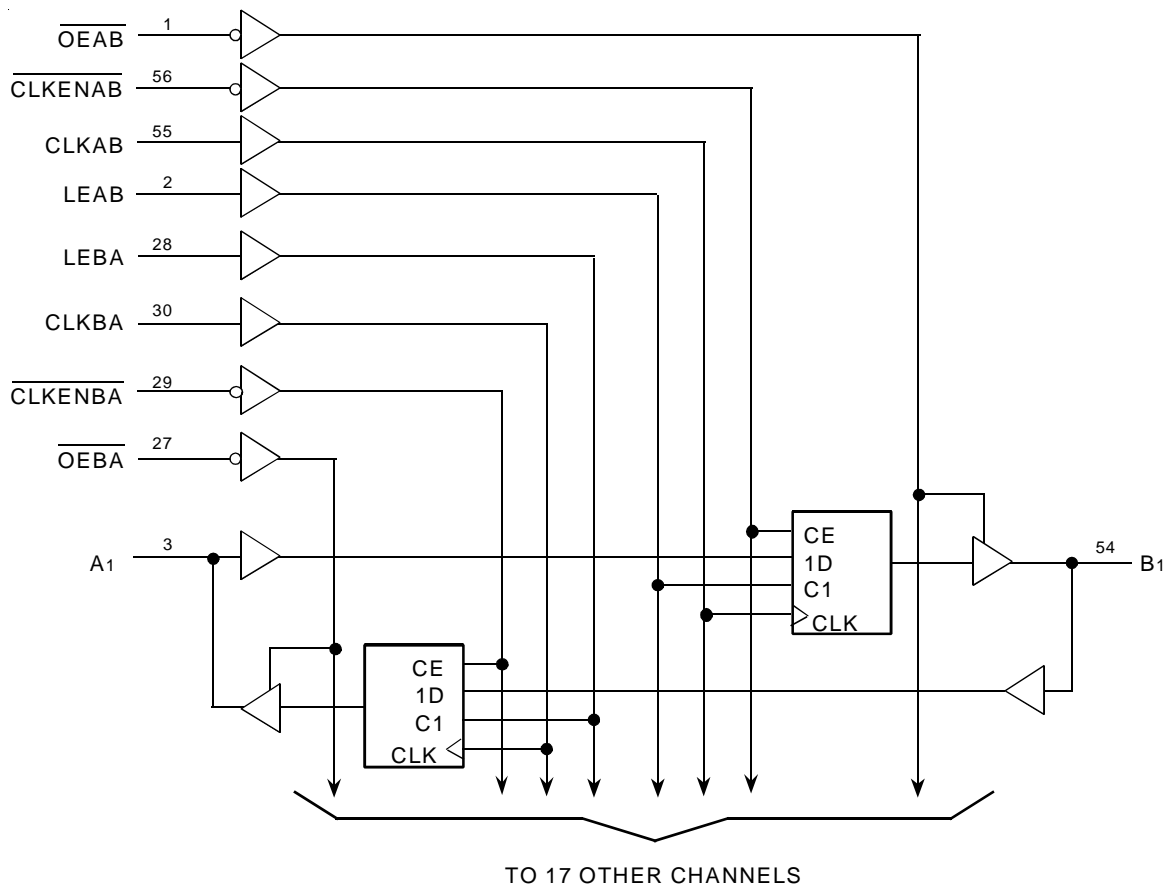
## DESCRIPTION:

The FCT16601T 18-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power 18-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in either direction in a transparent, latched or clocked mode. Each direction has an independent latch enable, an independent clock with a clock enable, and an independent output enable. The package is organized with a flow-through signal pin organization to ease board layout. All inputs are designed with hysteresis for improved noise margin.

This transceiver is ideally suited for high speed memory interfaces which utilize high speed synchronous writes, by clocking the data into a high speed register. Reads can then be performed in a transparent or latched mode utilizing the same transceiver.

The FCT16601T are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

## FUNCTIONAL BLOCK DIAGRAM

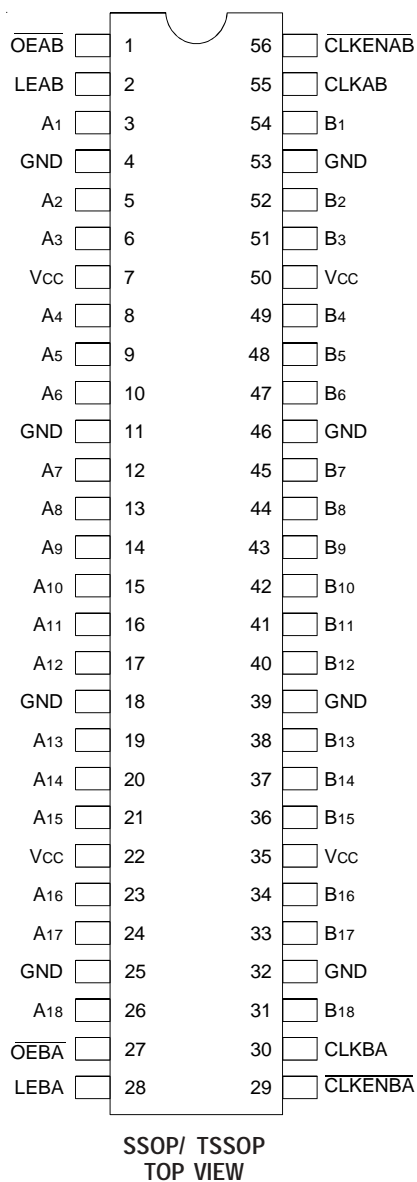


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INDUSTRIAL TEMPERATURE RANGE

MAY 2001

## PIN CONFIGURATION



## PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A <sub>x</sub>	A-to-B Data Inputs or B-to-A 3-State Outputs
B <sub>x</sub>	B-to-A Data Inputs or A-to-B 3-State Outputs
CLKENAB	A to B Clock Enable Input
CLKENBA	B to A Clock Enable Input

## ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V <sub>TERM</sub> (2)	Terminal Voltage with Respect to GND	-0.5 to +7	V
V <sub>TERM</sub> (3)	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-60 to +120	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXX Output and I/O terminals.
- Output and I/O terminals for FCT162XXX.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	3.5	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	3.5	8	pF

### NOTE:

- This parameter is measured at characterization but not tested.

## FUNCTION TABLE (1, 4)

Inputs				Outputs	
CLKENAB	$\overline{OEAB}$	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B <sup>(2)</sup>
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B <sup>(2)</sup>
L	L	L	H	X	B <sup>(3)</sup>

### NOTES:

- A-to-B data flow is shown. B-to-A data flow is similar but uses  $\overline{OEBA}$ , LEBA, and CLKBA.
- Output level before the indicated steady-state input conditions were established.
- Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance  
↑ = LOW-to-HIGH Transition

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current (Input pins)	$V_{CC} = \text{Max.}$	$V_i = V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
	Input HIGH Current (I/O pins)			—	—	$\pm 1$	
$I_{IL}$	Input LOW Current (Input pins)		$V_i = \text{GND}$	—	—	$\pm 1$	
	Input LOW Current (I/O pins)			—	—	$\pm 1$	
$I_{OZH}$	High Impedance Output Current (3-State Output pins)	$V_{CC} = \text{Max.}$	$V_o = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$			$V_o = 0.5\text{V}$	—	—	$\pm 1$	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_o = \text{GND}^{(3)}$		-80	-140	-250	mA
$V_H$	Input Hysteresis	—		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$ or $V_{CC}$		—	5	500	$\mu\text{A}$

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_o$	Output Drive Current	$V_{CC} = \text{Max.}, V_o = 2.5\text{V}^{(3)}$		-50	—	-180	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -3\text{mA}$	2.5	3.5	—	V
			$I_{OH} = -15\text{mA}$	2.4	3.5	—	
			$I_{OH} = -32\text{mA}^{(4)}$	2	3	—	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 64\text{mA}$	—	0.2	0.55	V
$I_{OFF}$	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}, V_{IN}$ or $V_o \leq 4.5\text{V}$		—	—	$\pm 1$	$\mu\text{A}$

### NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open $\overline{OEAB} = V_{CC}$ , $\overline{OEBA} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	75	120	$\mu A/$ MHz
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open $f_{CP} = 10\text{MHz}$ (CLKBA) 50% Duty Cycle $\overline{OEAB} = V_{CC}$ $\overline{OEBA} = \text{GND}$ LEAB = GND $\overline{CLKENBA} = \text{GND}$ One Bit Toggling $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.8	1.7	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.3	3.2	
		$V_{CC} = \text{Max.}$ , Outputs Open $f_{CP} = 10\text{MHz}$ (CLKBA) 50% Duty Cycle $\overline{OEAB} = V_{CC}$ $\overline{OEBA} = \text{GND}$ LEBA = GND $\overline{CLKENBA} = \text{GND}$ Eighteen Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	6.5 <sup>(5)</sup>	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	8.5	20.8 <sup>(5)</sup>	

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ C$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V)$   
 $D_H = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at } D_H$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$   
 $f_i = \text{Input Frequency}$   
 $N_i = \text{Number of Inputs at } f_i$

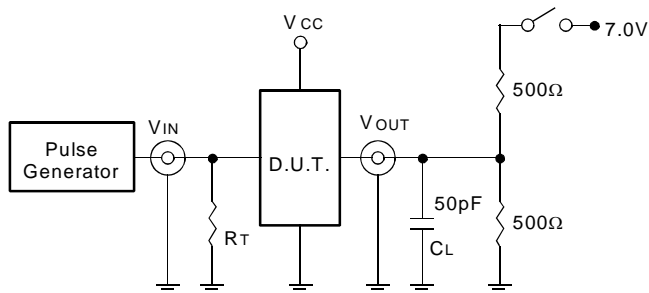
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition <sup>(1)</sup>	FCT16601AT		FCT16601CT		Unit	
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.		
f <sub>MAX</sub>	CLKAB or CLKBA frequency <sup>(3)</sup>	CL = 50pF RL = 500Ω	—	150	—	150	MHz	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ax to Bx or Bx to Ax		1.5	4.9	1.5	4	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEBA to Ax, LEAB to Bx		1.5	5.2	1.5	4.2	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CLKBA to Ax, CLKAB to Bx		1.5	4.7	1.5	4.2	ns	
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\overline{OEBA}$ to Ax, $\overline{OEAB}$ to Bx		1.5	5.8	1.5	4.8	ns	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time $\overline{OEBA}$ to Ax, $\overline{OEAB}$ to Bx		1.5	6.2	1.5	5.2	ns	
t <sub>SU</sub>	Set-up Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA		4	—	2.4	—	ns	
t <sub>H</sub>	Hold Time, HIGH or LOW Ax after CLKAB, Bx after CLKBA		0	—	0	—	ns	
t <sub>SU</sub>	Set-up Time, HIGH or LOW Ax to LEAB, Bx to LEBA		Clock LOW	1	—	1	—	ns
			Clock HIGH	2.5	—	1.5	—	ns
t <sub>H</sub>	Hold Time HIGH or LOW Ax after LEAB, Bx after LEBA		2	—	0.5	—	ns	
t <sub>SU</sub>	Set-up Time, $\overline{CLKEN}$ to CLK		2.5	—	2	—	ns	
t <sub>H</sub>	Hold Time, $\overline{CLKEN}$ after CLK		0	—	0	—	ns	
t <sub>w</sub>	LEAB or LEBA Pulse Width HIGH <sup>(3)</sup>		2.5	—	2.5	—	ns	
t <sub>w</sub>	CLKAB or CLKBA Pulse Width HIGH or LOW <sup>(3)</sup>	3	—	3	—	ns		
t <sub>SK(o)</sub>	Output Skew <sup>(4)</sup>	—	0.5	—	0.5	ns		

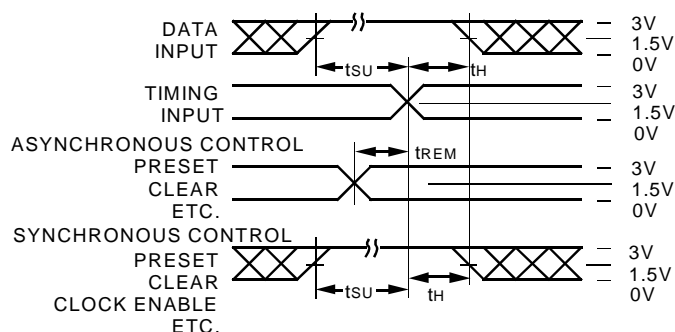
NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

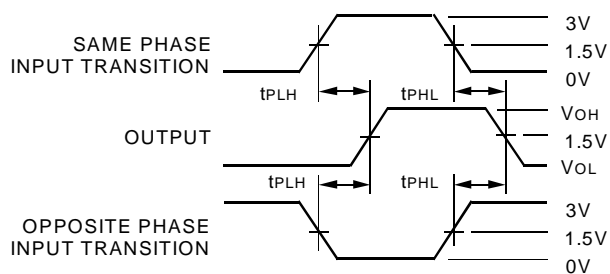
## TEST CIRCUITS AND WAVEFORMS



*Test Circuits for All Outputs*



*Set-up, Hold, and Release Times*



*Propagation Delay*

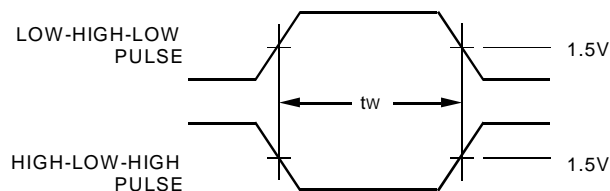
## SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

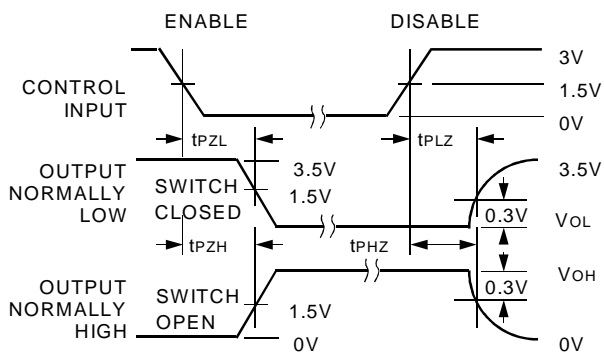
### DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to Zout of the Pulse Generator.



*Pulse Width*

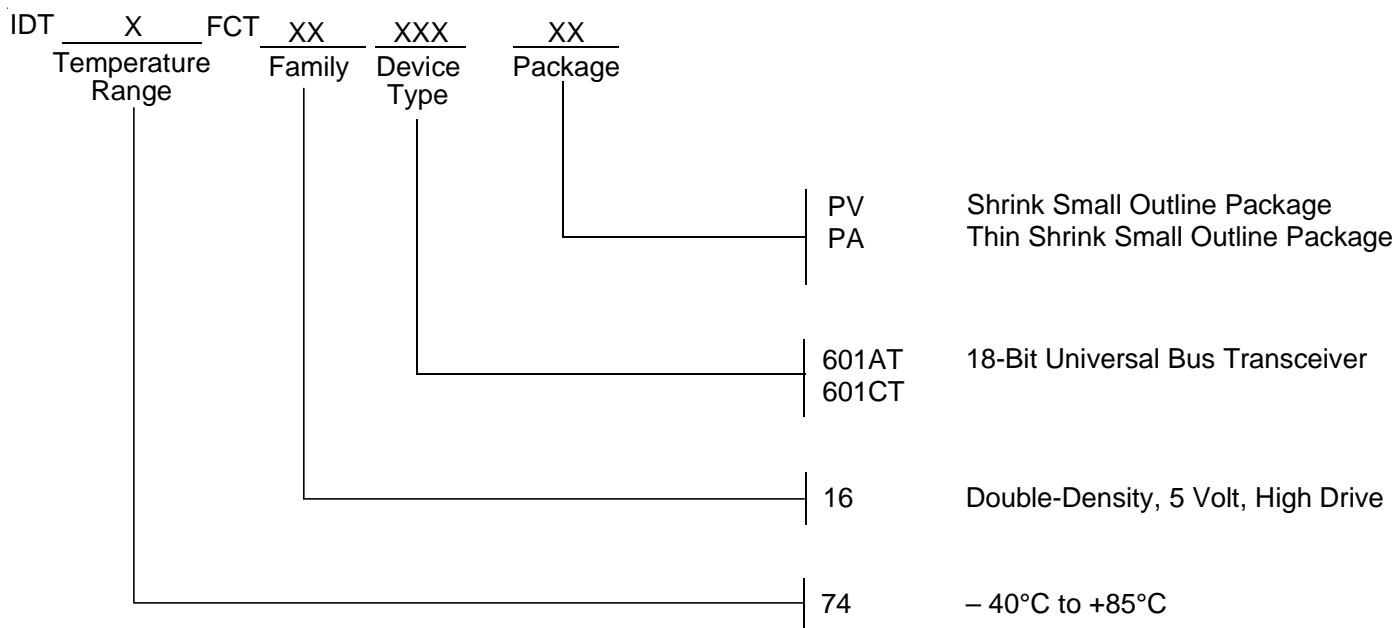


*Enable and Disable Times*

### NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$ .

## ORDERING INFORMATION



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