PRELIMINARY

Integrated Circuit Systems, Inc.

ICS843001I-22

FEMTOCLOCKS™ CRYSTAL/LVCMOS-TO-3.3V, 2.5V LVPECL FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The ICS843001I-22 is a a highly versatile, low phase noise LVPECL/LVCMOS Synthesizer which can generate low jitter reference clocks for a variety of communications applications and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. The dual crystal interface allows the synthesizer to support up to two communications standards in a given application (i.e. 1GB Ethernet with a 25MHz crystal and 1Gb Fibre Channel using a 25.5625MHz crystal). The rms phase jitter performance is typically less than 1ps, thus making the device acceptable for use in demanding applications such as OC48 SONET and 10Gb Ethernet. The ICS843001I-22 is packaged in a small 24-pin TSSOP package.

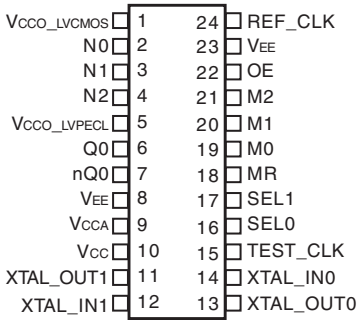
FEATURES

- One 3.3V or 2.5V LVPECL output pair and one LVCMOS/LVTTL output
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- VCO range: 490MHz - 640MHz
- Output frequency range: 490MHz - 640MHz
- Supports the following applications: SONET, Ethernet, Fibre Channel, Serial ATA, and HDTV
- RMS phase jitter @ 622.08MHz (12kHz - 20MHz): 0.80ps (typical)
- Full 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Lead-Free package fully RoHS compliant

CONTROL INPUT FUNCTION TABLE

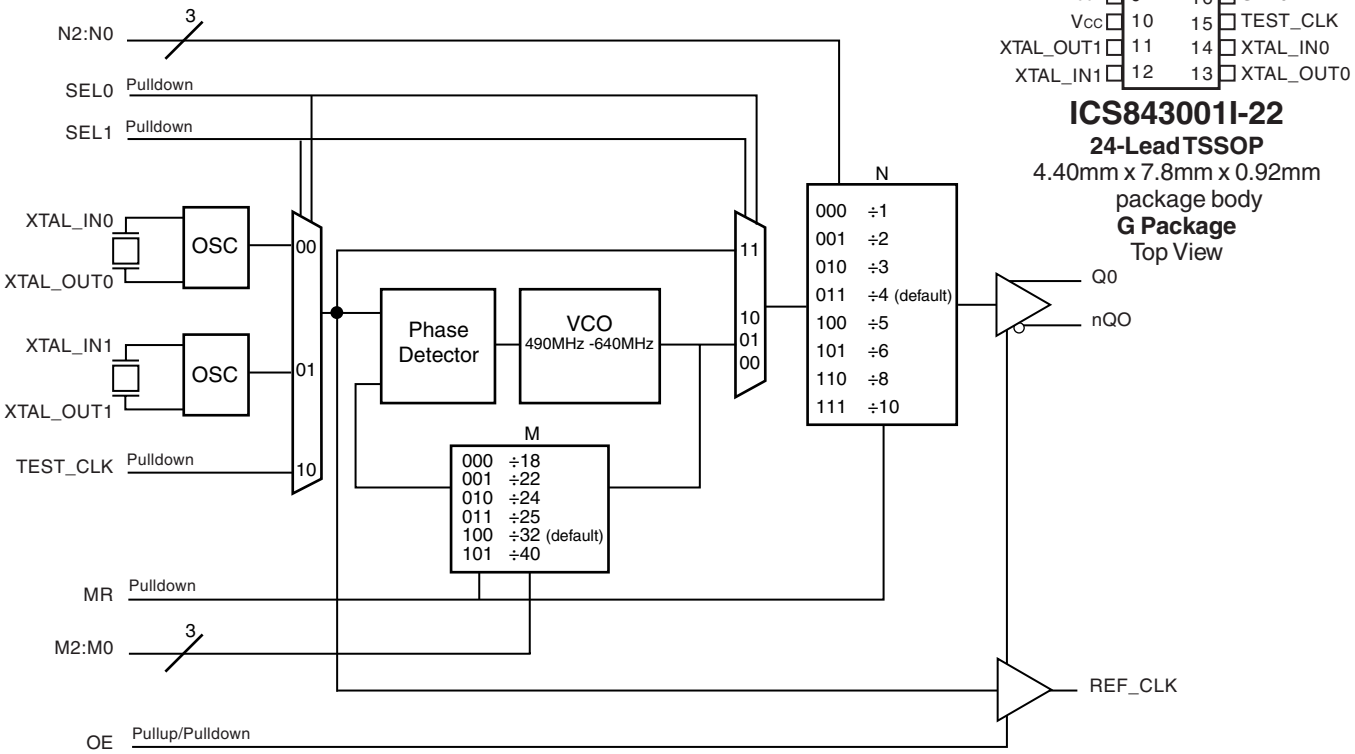
Control Input	Outputs
OE	State
0	Q0/nQ0, REF_CLK = High-Z
1	Q0/nQ0 = High-Z, REF_CLK = Active
FLOAT	Q0/nQ0 = Active, REF_CLK = High-Z

PIN ASSIGNMENT



ICS843001I-22
24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm package body
G Package
Top View

BLOCK DIAGRAM



The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 5	V_{CCO_LVCMOS}, V_{CCO_LVPECL}	Power		Output supply pins.
2, 3	N0, N1	Input	Pullup	Output divider select pins. Default value = ÷4. LVCMOS/LVTTL interface levels. See Table 3C.
4	N2	Input	Pulldown	
6, 7	Q0, nQ0	Ouput		Differential output pair. LVPECL interface levels.
8, 23	V_{EE}	Power		Negative supply pin.
9	V_{CCA}	Power		Analog supply pin.
10	V_{CC}	Power		Core supply pin.
11 12	XTAL_OUT1, XTAL_IN1	Input		Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input.
13 14	XTAL_OUT0, XTAL_IN0	Input		Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input.
15	TEST_CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
16, 17	SEL0, SEL1	Input	Pulldown	Input MUX select pins. LVCMOS/LVTTL interface levels. See Table 3D.
18	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true output Q0 to go low and the inverted output nQ0 to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
19, 20	M0, M1	Input	Pulldown	Feedback divider select pins. Default value = ÷32. LVCMOS/LVTTL interface levels. See Table 3B.
21	M2	Input	Pullup	
22	OE	Input	Pullup/ Pulldown	3-State clock output enable, (High/Low/Float). LVCMOS/LVTTL interface levels. See page 1, Control Input Function Table.
24	REF_CLK	Output		Reference clock output. LVCMOS/LVTTL interface levels.

NOTE: *Pulldown and Pullup* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ
R_{out}	Output Impedance	REF_CLK		15		Ω

TABLE 3A. COMMON CONFIGURATIONS TABLE

Input Reference Clock (MHz)	M Divider Value	N Divider Value	VCO (MHz)	Output Frequency (MHz)	Application
27	22	8	594	74.25	HDTV
22.4	25	8	560	70	
24.75	24	8	594	74.25	HDTV
25	24	3	600	200	
14.8351649	40	8	593.4066	74.1758245	HDTV
19.44	32	4	622.08	155.52	SONET
19.44	32	8	622.08	77.76	SONET
19.44	32	1	622.08	622.08	SONET
19.44	32	2	622.08	311.04	SONET
19.53125	32	4	625	156.25	10 GigE
20	25	2	500	250	Ethernet
25	25	5	625	125	1 GigE
25	25	10	625	62.5	1 GigE
25	24	6	600	100	PCI Express
25	24	4	600	150	SATA
25	24	8	600	75	SATA
26.5625	24	6	637.5	106.25	Fibre Channel 1
26.5625	24	3	637.5	212.5	4 Gig Fibre Channel
26.5625	24	4	637.5	159.375	10 Gig Fibre Channel
31.25	18	3	562.5	187.5	12 Gig Ethernet

TABLE 3B. PROGRAMMABLE M OUTPUT DIVIDER FUNCTION TABLE

Inputs			M Divider Value	Input Frequency (MHz)	
M2	M1	M0		Minimum	Maximum
0	0	0	18	27.22	35.56
0	0	1	22	22.27	29.09
0	1	0	24	20.41	26.67
0	1	1	25	19.6	25.6
1	0	0	32	15.31	20
1	0	1	40	12.25	16

TABLE 3C. PROGRAMMABLE N OUTPUT DIVIDER FUNCTION TABLE

Inputs			N Divide Value
N2	N1	N0	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4 (default)
1	0	0	5
1	0	1	6
1	1	0	8
1	1	1	10

TABLE 3D. BYPASS MODE FUNCTION TABLE

Inputs		Reference Input	PLL Mode
SEL1	SEL0		
0	0	XTAL0	Active
0	1	XTAL1	Active
1	0	TEST_CLK	Active
1	1	TEST_CLK	Bypass

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL)	
Continuous Current	50mA
Surge Current	100mA
Outputs, V_O (LVCMOS)	-0.5V to V_{CCO} + 0.5V
Package Thermal Impedance, θ_{JA}	70°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO\_LVCMOS}$, V_{CCO_LVPECL} = 3.3V±10%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.97	3.3	3.63	V
V_{CCA}	Analog Supply Voltage		2.97	3.3	3.63	V
$V_{CCO\_LVPECL, \_LVCMOS}$	Output Supply Voltage		2.97	3.3	3.63	V
I_{EE}	Power Supply Current			115		mA
$I_{CCO\_LVPECL, \_LVCMOS}$	Output Supply Current			5		mA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO\_LVCMOS}$, V_{CCO_LVPECL} = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		2.375	2.5	2.625	V
$V_{CCO\_PECL, \_LVCMOS}$	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			110		mA
$I_{CCO\_PECL, \_LVCMOS}$	Output Supply Current			5		mA

TABLE 4C. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO\_LVCMOS}$ = 3.3V±10% OR 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V ± 10%	2		V_{CC} + 0.3	V
			V_{CC} = 2.5V ± 5%	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V ± 10%	-0.3		0.8	V
			V_{CC} = 2.5V ± 5%	-0.3		0.7	V
I_{IH}	Input High Current	TEST_CLK, SEL0, SEL1, MR, M0, M1, N2, OE	$V_{CC} = V_{IN}$ = 3.63V or 2.625V			150	µA
		M2, N0, N1	$V_{CC} = V_{IN}$ = 3.63V or 2.625V			5	µA
I_{IL}	Input Low Current	TEST_CLK, SEL0, SEL1, MR, M0, M1, N2, OE	V_{CC} = 3.63V or 2.625V, V_{IN} = 0V	-5			µA
		M2, N0, N1	V_{CC} = 3.63V or 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{CCO_LVCMOS} = 3.63V	2.6			V
			V_{CCO_LVCMOS} = 2.625V	1.8			V
V_{OL}	Output Low Voltage: Note 1		V_{CCO_LVCMOS} = 3.63V or 2.625V			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO\_LVCMOS}/2$. See Parameter Measurement Information Section, "Output Load Test Circuit Diagram".

TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO\_LVPECL}$ = 3.3V±10% OR 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO_PECL} - 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			MHz
Frequency		12		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6A. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO\_LVCMOS}$, V_{CCO_LVPECL} = 3.3V±10%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		49		640	MHz
$t$jit(Ø)	RMS Phase Jitter, (Random); NOTE 1, 2	622.08MHz (12kHz - 20MHz)		0.80		ps
f_{VCO}	PLL VCO Lock Range		490		640	MHz
t_R / t_F	Output Rise/Fall Time	20% to 80%		450		ps
odc	Output Duty Cycle			50		%

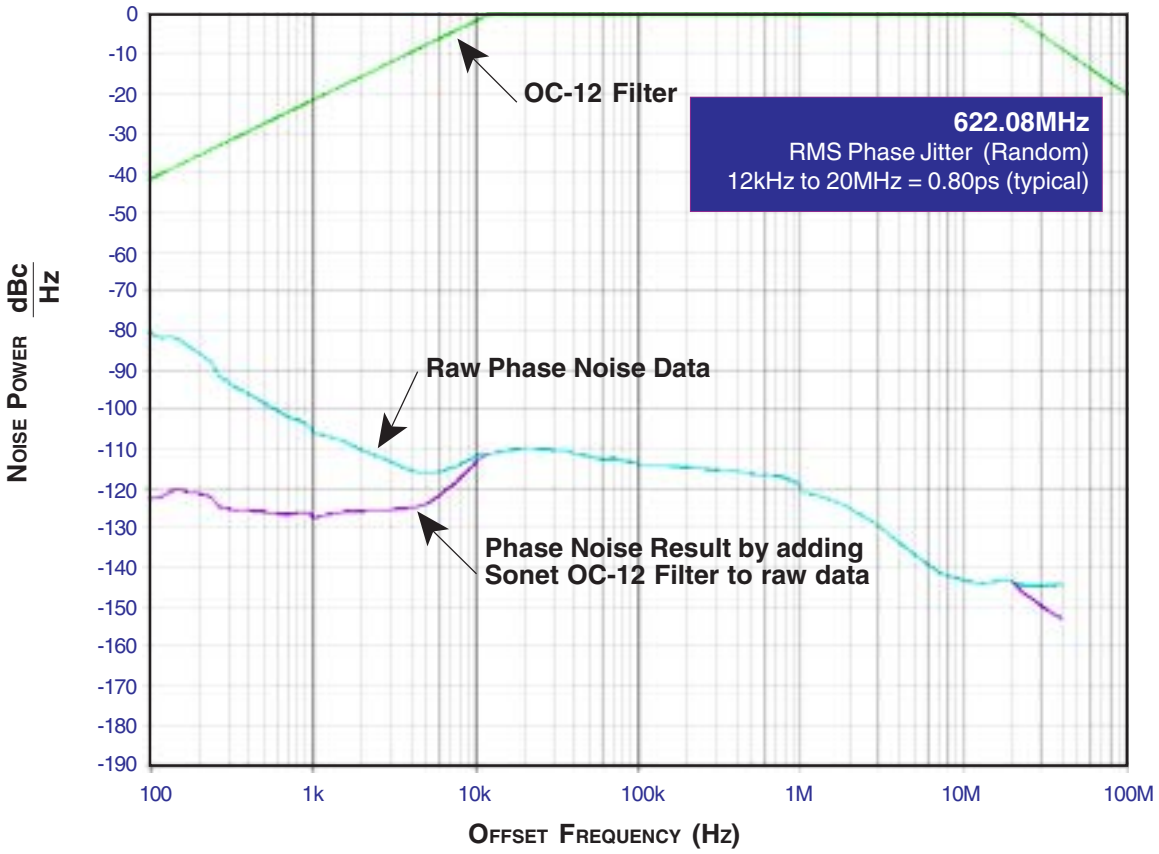
NOTE 1: Phase jitter using a crystal interface.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6B. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO\_LVCMOS}$, V_{CCO_LVPECL} = 2.5V±5%, TA = -40°C TO 85°C

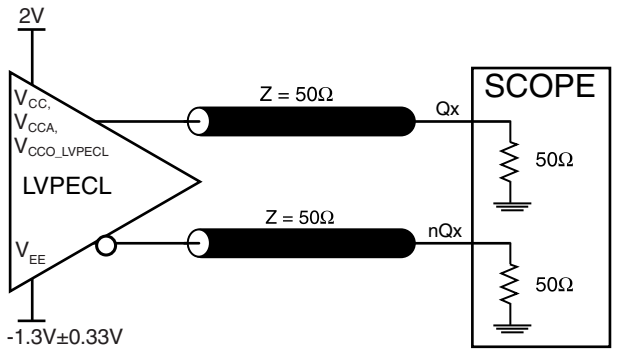
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		49		640	MHz
$t$jit(Ø)	RMS Phase Jitter, (Random); NOTE 1, 2	622.08MHz (12kHz - 20MHz)		0.80		ps
f_{VCO}	PLL VCO Lock Range		490		640	MHz
t_R / t_F	Output Rise/Fall Time	20% to 80%		450		ps
odc	Output Duty Cycle			50		%

NOTE 1: Phase jitter using a crystal interface.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

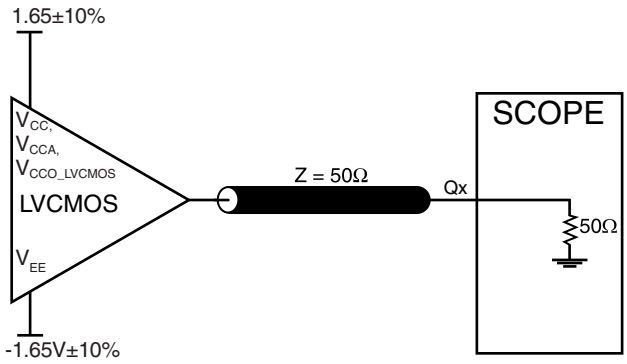
TYPICAL PHASE NOISE AT 622.08MHZ



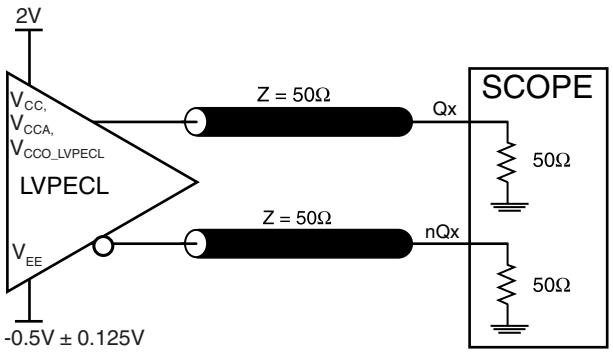
PARAMETER MEASUREMENT INFORMATION



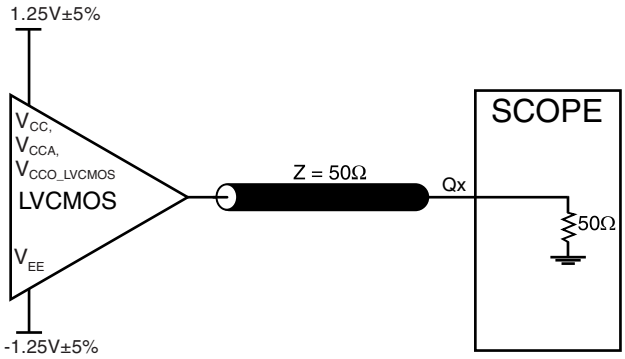
3.3V LVPECL OUTPUT LOAD AC TEST CIRCUIT



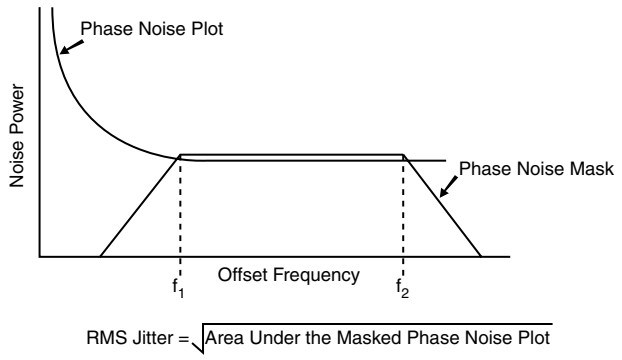
3.3V LVCMOS OUTPUT LOAD AC TEST CIRCUIT



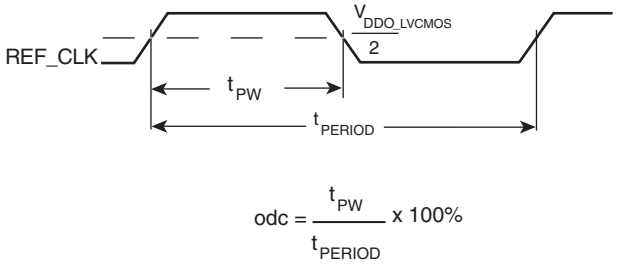
2.5V LVPECL OUTPUT LOAD AC TEST CIRCUIT



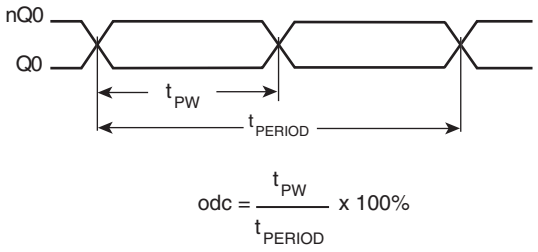
2.5V LVCMOS OUTPUT LOAD AC TEST CIRCUIT



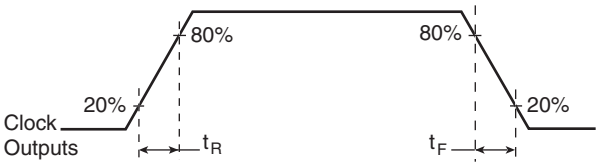
RMS PHASE JITTER



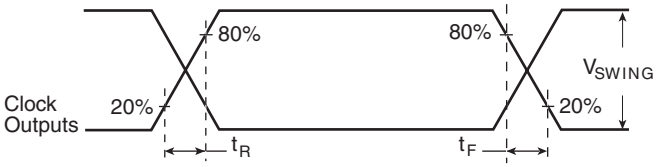
LVCMOS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



LVPECL OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



LVCMOS OUTPUT RISE/FALL TIME



LVPECL OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843001I-22 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO_x} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA}.

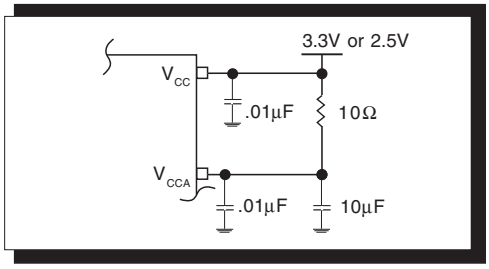


FIGURE 1. POWER SUPPLY FILTERING

TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

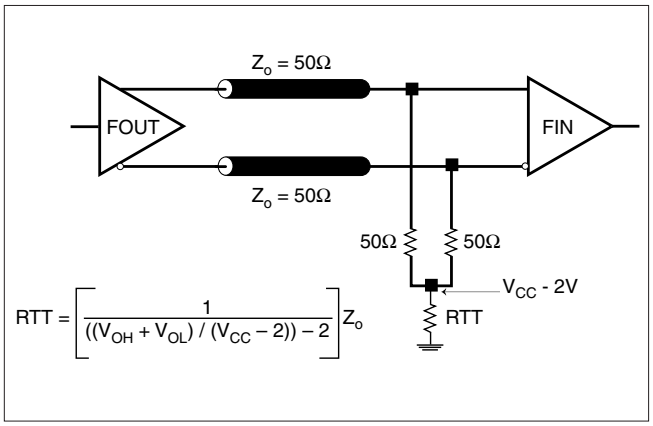


FIGURE 2A. LVPECL OUTPUT TERMINATION

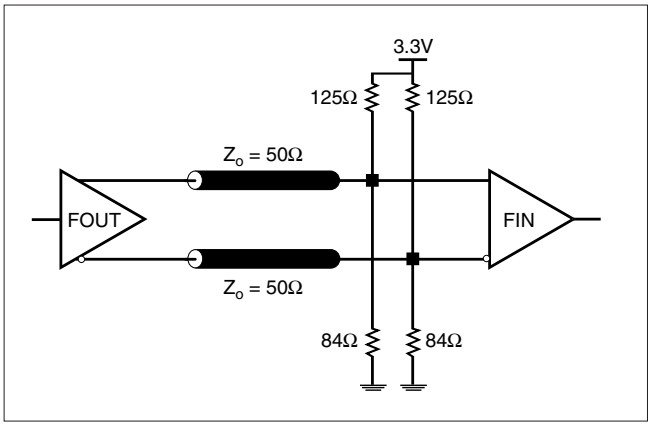


FIGURE 2B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 3A and *Figure 3B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CCO} = 2.5V, the V_{CCO} - 2V is very close to ground level. The R3 in Figure 3B can be eliminated and the termination is shown in *Figure 3C.*

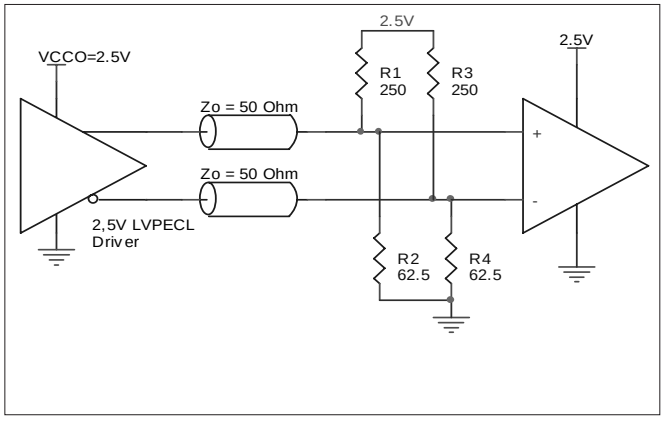


FIGURE 3A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

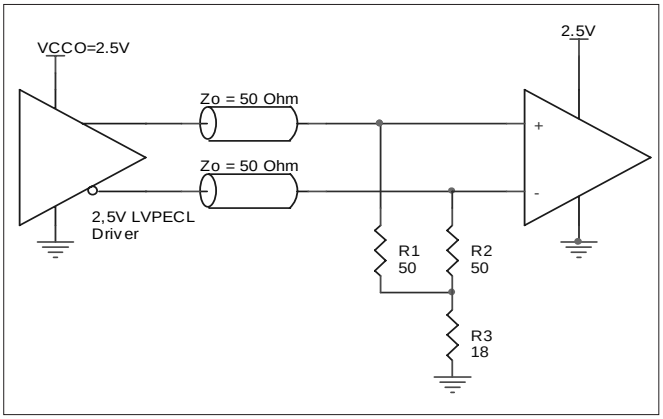


FIGURE 3B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

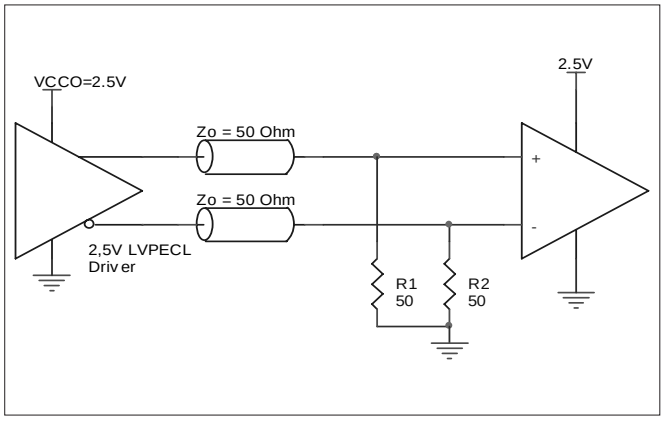


FIGURE 3C. 2.5V LVPECL TERMINATION EXAMPLE

CRYSTAL INPUT INTERFACE

The ICS843001I-22 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 4* below were determined using a 26.5625MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

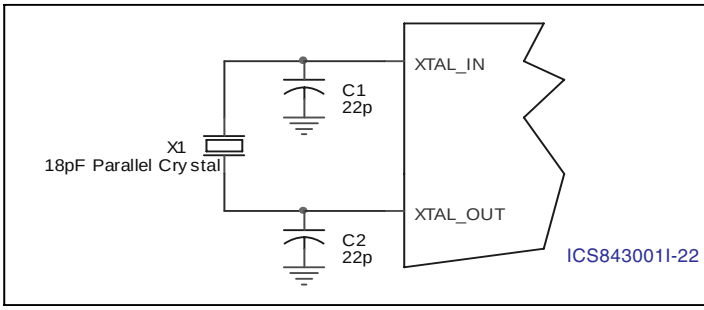


Figure 4. CRYSTAL INPUT INTERFACE

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for ICS843001I-22 is: 3881

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

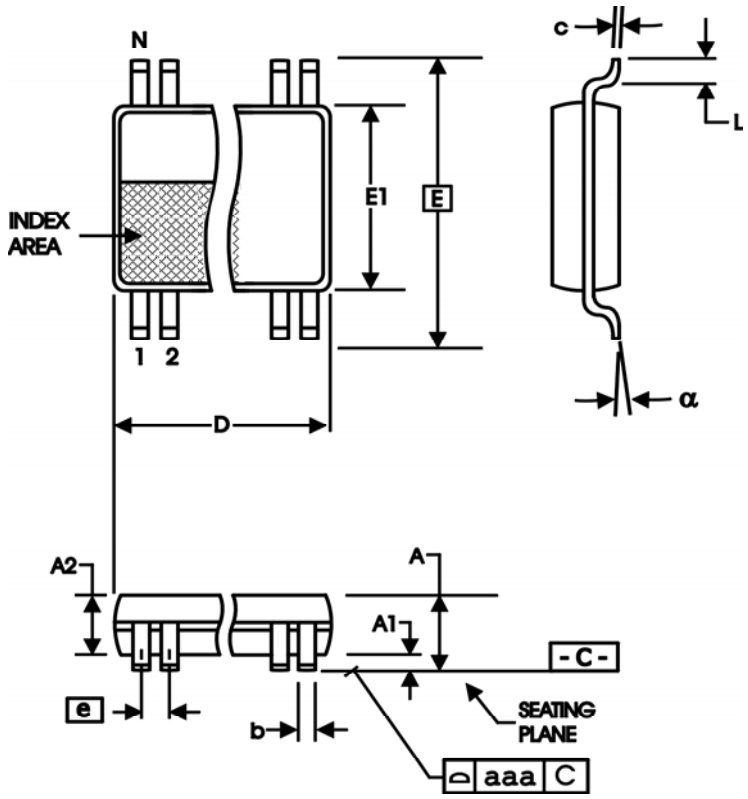


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843001AGI-22	ICS843001AI22	24 Lead TSSOP	tube	-40°C to 85°C
ICS843001AGI-22T	ICS843001AI22	24 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS843001AGI-22LF	ICS43001AI22L	24 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS843001AGI-22LFT	ICS43001AI22L	24 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.