Document Title

128Kx16 bit 1.8V and Ultra Low Power CMOS Static RAM

Revision History

Revision No	History	Draft Date	Remark
0A	Initial Draft	April 23,2002	Preliminary

128K x 16 1.8V ULTRA LOW POWER CMOS STATIC RAM

FEATURES

- High-speed access times: 70, 100 ns
- CMOS low power operation
  I_{CC1}=7mA (typical)* operating
  I_{SB2}=0.5µA (typical)* CMOS standby
- * Typical values are measured at V_{CC}=1.8V, T_A=25°C
- TTL compatible interface levels
- Single 1.65V-2.2V Vcc power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- Available in the 44-pin TSOP-2 and 48-pin 6*8mm TF-BGA

DESCRIPTION

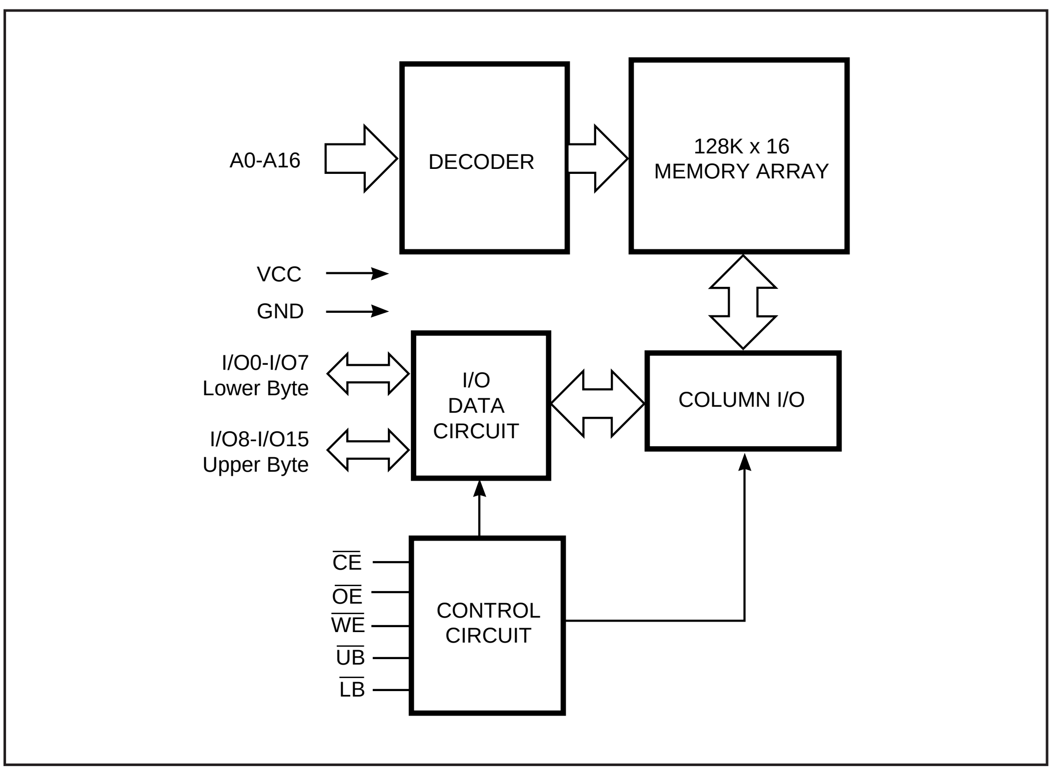
The *ICSI* IC62VV12816L and IC62VV12816LL are low-power, 2,097,152 bit static RAMs organized as 131,072 words by 16 bits. They are fabricated using *ICSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CE}$ is HIGH (deselected) or both $\overline{LB}$ and $\overline{UB}$ are HIGH, the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

Easy memory expansion is provided by using Chip Enable Output and Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

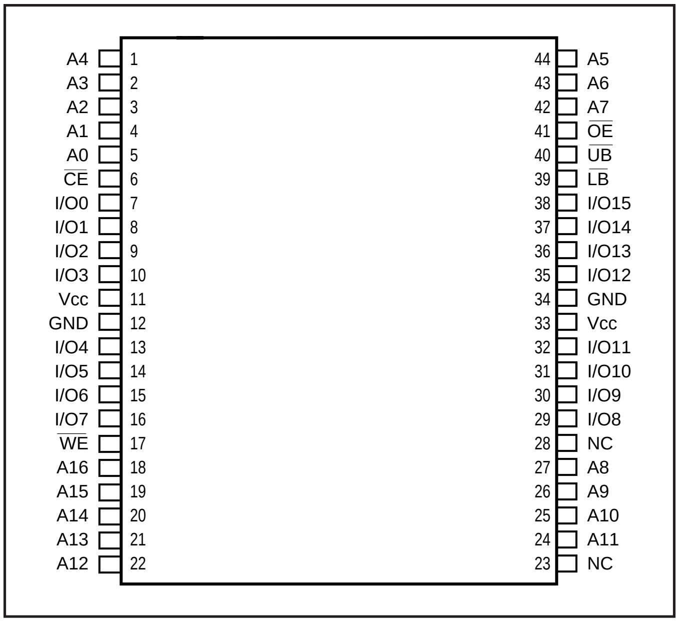
The IC62VV12816L and IC62VV12816LL are packaged in the JEDEC standare 44-pin TSOP-2 and 48-pin 6*8mm TF-BGA.

FUNCTIONAL BLOCK DIAGRAM

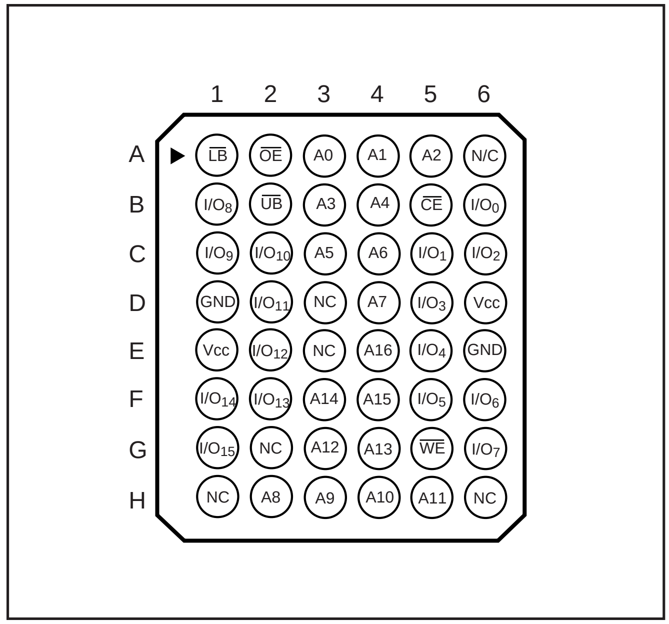


PIN CONFIGURATIONS

44-Pin TSOP-2



48-Pin TF-BGA (TOP View)



PIN DESCRIPTIONS

A0-A16	Address Inputs
I/O0-I/O15	Data Input/Output
$\overline{\text{CE}}$	Chip Enable Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{WE}}$	Write Enable Input
$\overline{\text{LB}}$	Lower-byte Control (I/O0-I/O7)
$\overline{\text{UB}}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
Vcc	Power
GND	Ground

TRUTH TABLE

						I/O PIN		
Mode	**$\overline{\text{WE}}$**	**$\overline{\text{CE}}$**	**$\overline{\text{OE}}$**	**$\overline{\text{LB}}$**	**$\overline{\text{UB}}$**	**I/O0/-I/O7**	**I/O8-I/O15**	**Power**
Not Selected	X	H	X	X	X	High-Z	High-Z	Stand by
	X	L	X	H	H	High-Z	High-Z	Stand by
Output Disabled	H	L	H	X	X	High-Z	High-Z	Active
	X	L	X	H	H	High-Z	High-Z	Stand by
Read	H	L	L	L	H	DOUT	High-Z	Active
	H	L	L	H	L	High-Z	DOUT	
	H	L	L	L	L	DOUT	DOUT	
Write	L	L	X	L	H	DIN	High-Z	Active
	L	L	X	H	L	High-Z	DIN	
	L	L	X	L	L	DIN	DIN	

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	1.65V- 2.2V
Industrial	–40°C to +85°C	1.65V - 2.2V

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to Vcc + 0.4	V
T_{BIAS}	Temperature Under Bias	–40 to + 85	°C
V_{CC}	Vcc related to GND	–0.3 to + 2.4	V
T_{STG}	Storage Temperature	–65 to + 150	°C
P_T	Power Dissipation	1.0	W

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	1.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	—	0.2	V
V_{IH}[1]	Input HIGH Voltage		1.4	V_{CC} + 0.2	V
V_{IL}[2]	Input LOW Voltage		–0.2	0.4	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Outputs Disabled	–1	1	µA

Notes:
1. V_{IH}(max.) = V_{CC}+2.0V for pulse width less than 10 ns.
2. V_{IL}(min.) = –2.0V for pulse width less than 10 ns.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0.4V to 1.4V
Input Rise and Fall Times	5 ns
Input Reference Level	0.9V
Output Reference Level	0.9V
Output Load	See Figures 1

AC TEST LOADS

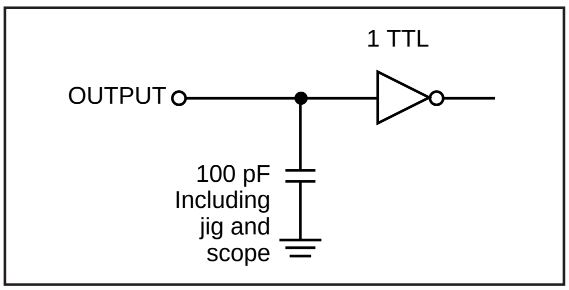


Figure 1

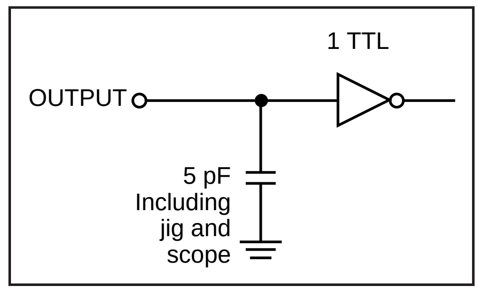


Figure 2

IC62VV12816L POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-70 Min.	-70 Max.	-100 Min.	-100 Max.	Unit
I_{CC1}	Vcc Dynamic Operating Supply Current	V_{CC} = 1.8V, I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	15	—	10	mA
			Ind.	—	15	—	10	
I_{CC2}	Vcc Dynamic Operating Supply Current	V_{CC} =1.8V, I_{OUT} = 0 mA, f = 1MHz	Com.	—	2	—	2	mA
			Ind.	—	2	—	2	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., Other inputs= 0 - V_{CC} 1) $\overline{CE} \geq V_{CC} - 0.2V$ ($\overline{CE}$ controlled) 2) $\overline{LB}$/ $\overline{UB} \geq V_{CC} - 0.2V$ ($\overline{LB}$/ $\overline{UB}$ controlled)	Com.	—	35	—	35	µA
			Ind.	—	50	—	50	

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

IC62VV12816LL POWER SUPPLY CHARACTERISTICS(1) (Over Operating Range)

Symbol	Parameter	Test Conditions		-70 Typ(2).	-70 Max.	-100 Typ(2).	-100 Max.	Unit
I_{CC1}	Vcc Dynamic Operating Supply Current	V_{CC} = 1.8V, $\overline{CE} \leq V_{IL}$ I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind.	7 7	15 15	4 4	10 10	mA
I_{CC2}	Vcc Dynamic Operating Supply Current	V_{CC} = 1.8V, $\overline{CE} \leq V_{IL}$ I_{OUT} = 0 mA, f = 1MHz	Com. Ind.	— —	2 2	— —	2 2	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., Other inputs= 0 - V_{CC} 1) $\overline{CE} \geq V_{CC} - 0.2V$ ($\overline{CE}$ controlled) 2) $\overline{LB}$/ $\overline{UB} \geq V_{CC} - 0.2V$ ($\overline{LB}$/ $\overline{UB}$ controlled)	Com. Ind.	0.5 —	5 10	0.5 —	5 10	µA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at Vcc=1.8V, Ta=25°C, and are not guaranteed or tested.

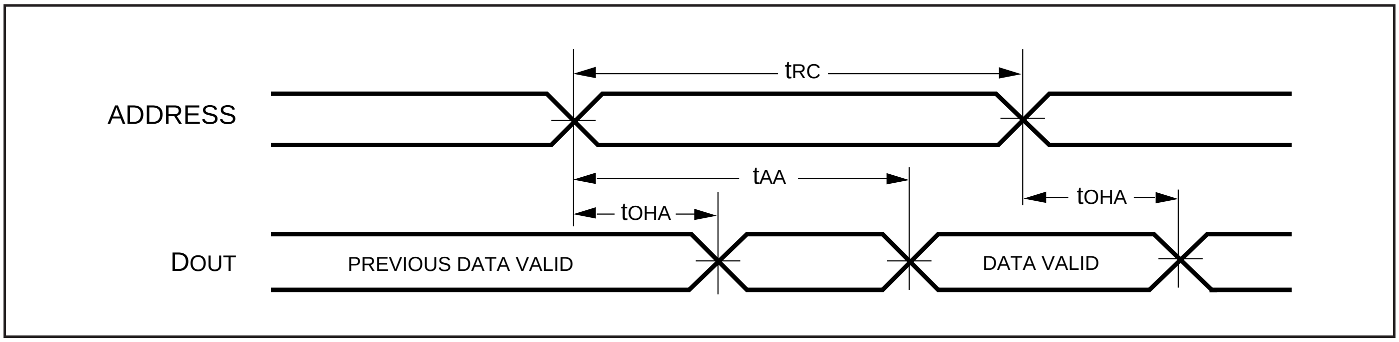
READ CYCLE SWITCHING CHARACTERISTICS(1) (Over Operating Range)

Symbol	Parameter	-70 Min.	-70 Max.	-100 Min.	-100 Max.	Unit
t_{RC}	Read Cycle Time	70	—	100	—	ns
t_{AA}	Address Access Time	—	70	—	100	ns
t_{OHA}	Output Hold Time	10	—	15	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	70	—	100	ns
t_{DOE}	$\overline{OE}$ Access Time	—	35	—	50	ns
t_{HZOE}(2)	$\overline{OE}$ to High-Z Output	—	25	—	30	ns
t_{LZOE}(2)	$\overline{OE}$ to Low-Z Output	5	—	5	—	ns
t_{HZCE}(2)	$\overline{CE}$ to High-Z Output	0	25	0	30	ns
t_{LZCE}(2)	$\overline{CE}$ to Low-Z Output	10	—	10	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	70	—	100	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ o High-Z Output	0	25	0	35	ns
t_{LZB}	$\overline{LB}$. $\overline{UB}$ to Low-Z Output	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, input pulse levels of 0.4V to 1.4V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

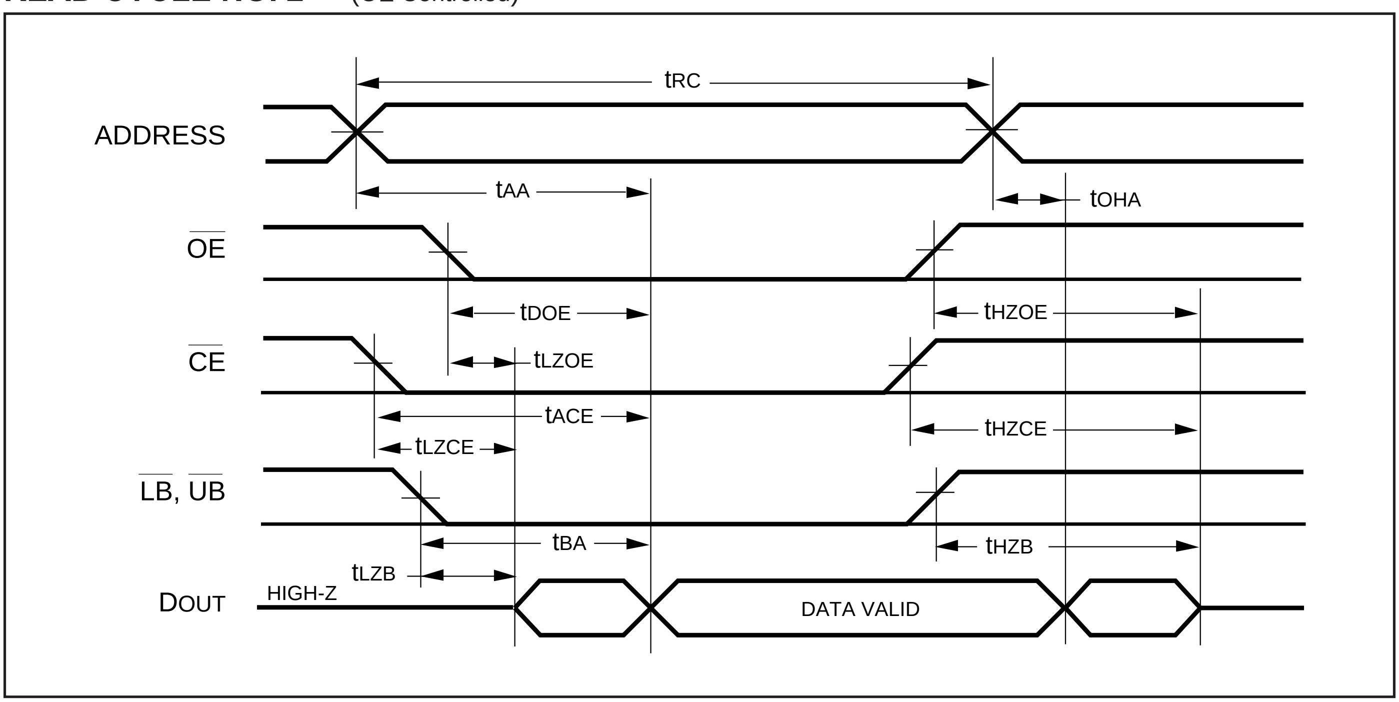
AC TEST LOADS

READ CYCLE NO.1(1,2) (Address Controlled) ($\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL})



AC WAVEFORMS

READ CYCLE NO. 2(1,3) ($\overline{OE}$ Controlled)



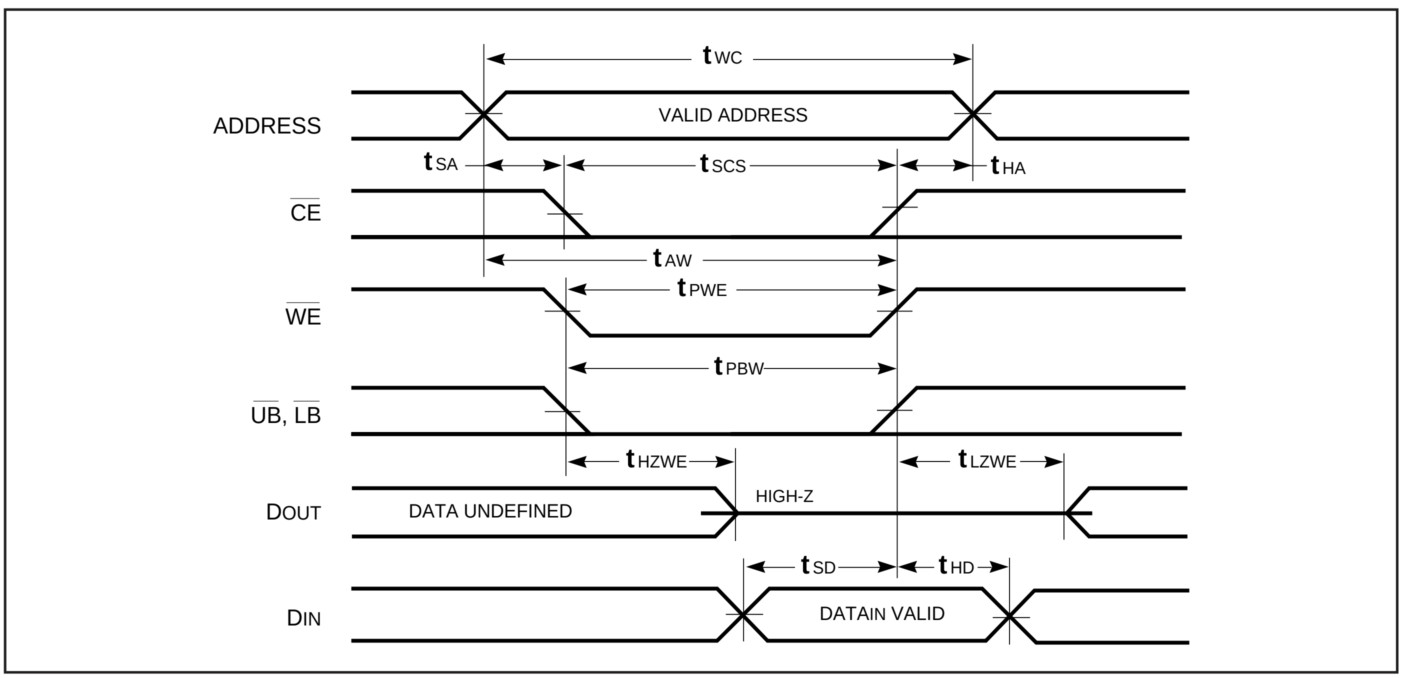
Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{UB}$, or $\overline{LB}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

Symbol	Parameter	-70 Min.	-70 Max.	-100 Min.	-100 Max	Unit
t_{WC}	Write Cycle Time	70	—	100	—	ns
t_{SCE}	$\overline{CE}$ to Write End	65	—	80	—	ns
t_{AW}	Address Setup Time to Write End	65	—	80	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	60	—	80	—	ns
t_{PWE}	$\overline{WE}$ Pulse Width	55	—	80	—	ns
t_{SD}	Data Setup to Write End	30	—	40	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	30	—	40	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	ns

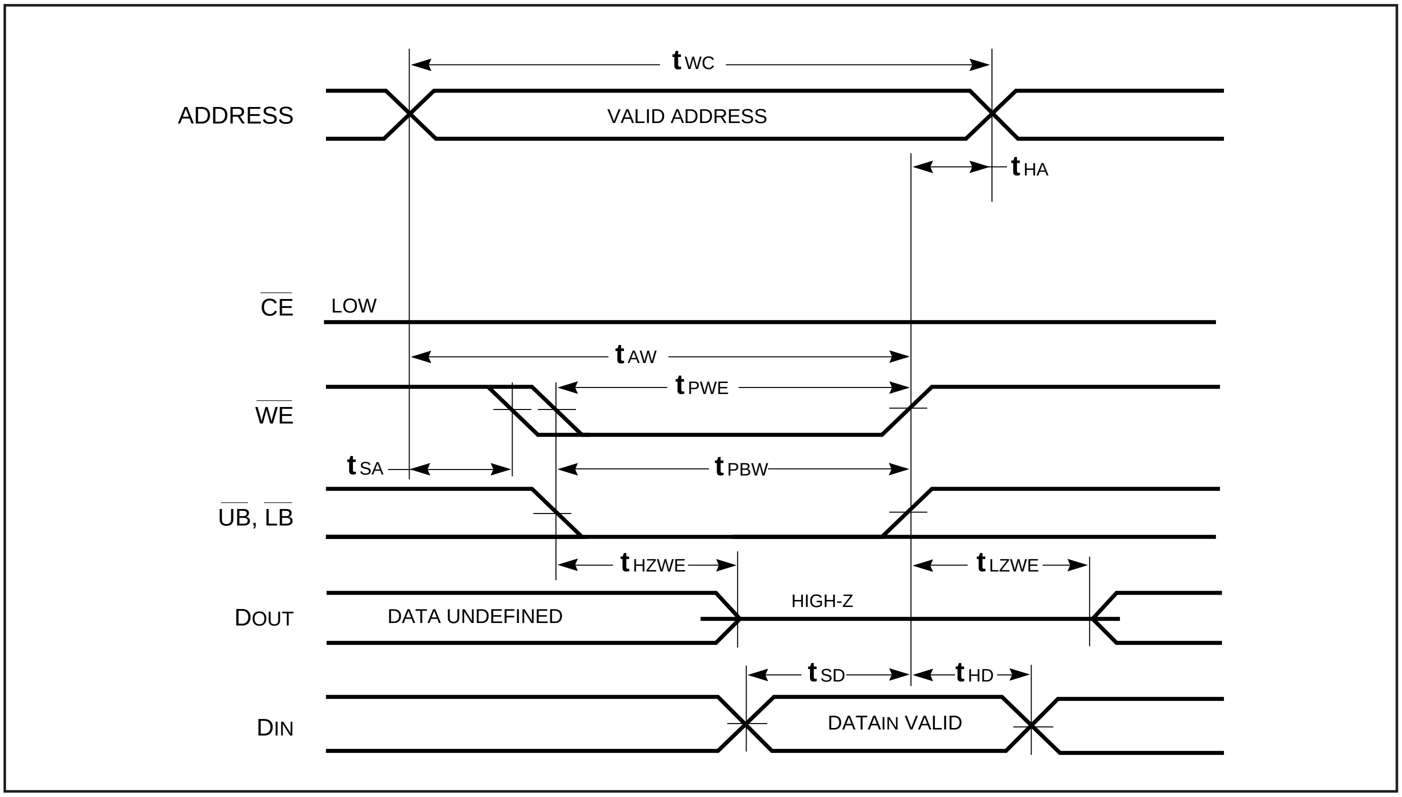
Notes:
1. Test conditions assume signal transition times of 5 ns or less, input pulse levels of 0.4V to 1.4V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CE}$ LOW, and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS
WRITE CYCLE NO. 1[1,2] ($\overline{CE}$ Controlled)

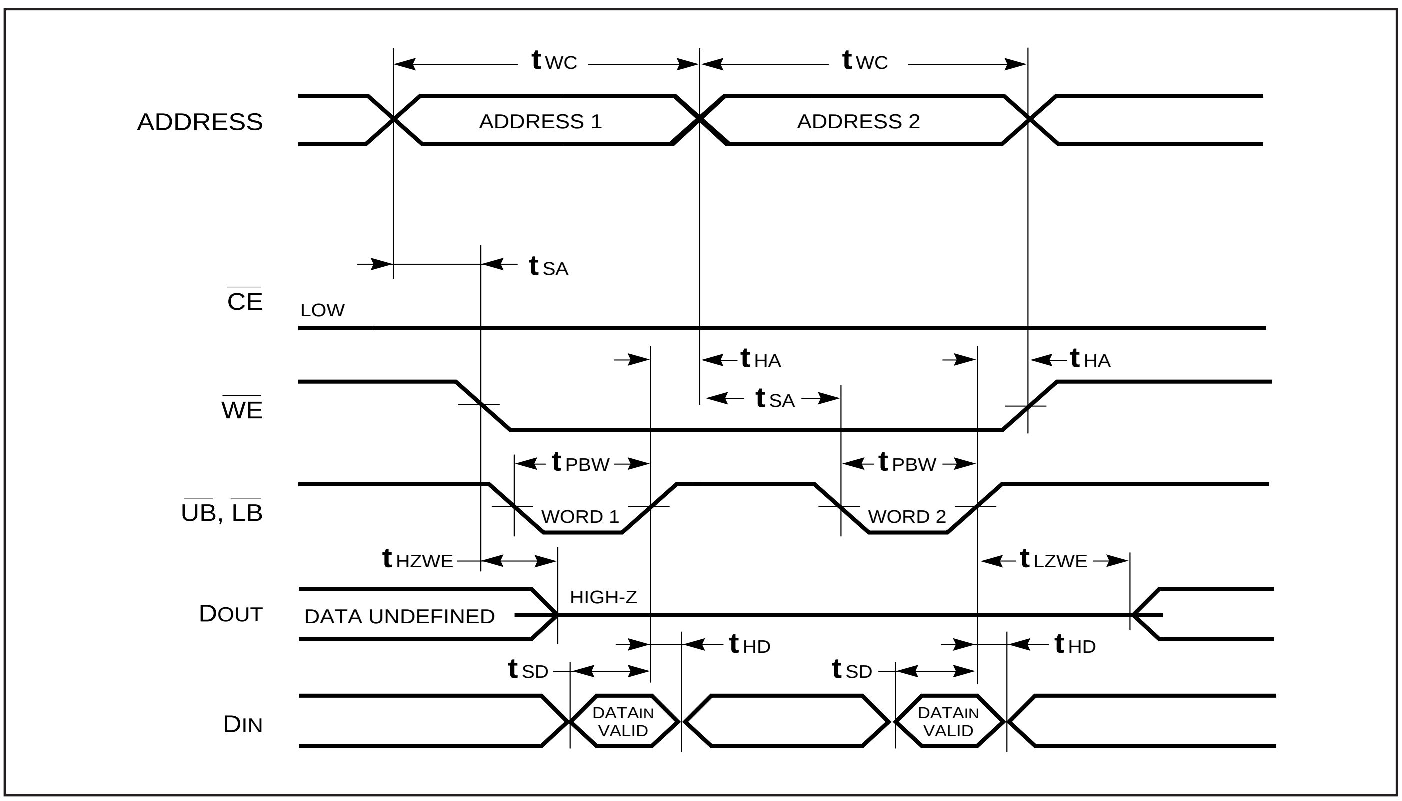


Notes:
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CE}$ and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CE}$) [($\overline{LB}$) = ($\overline{UB}$)] ($\overline{WE}$).

WRITE CYCLE NO. 2 (WE Controlled)



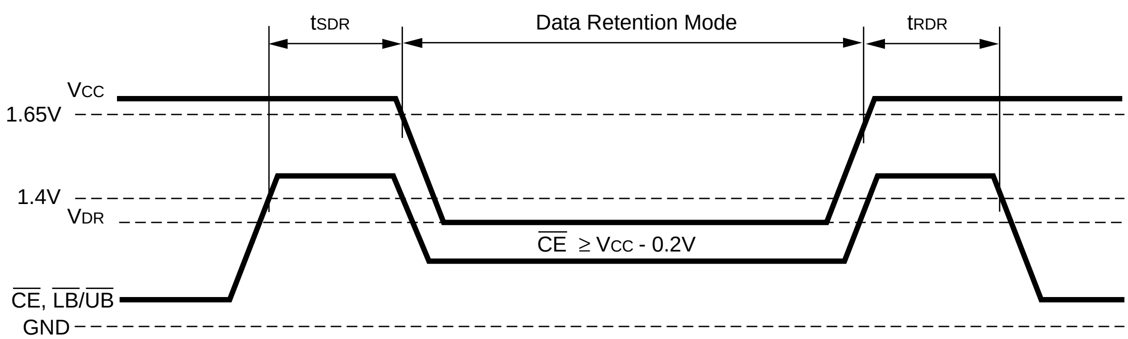
WRITE CYCLE NO. 3 (UB / LB Controlled)



DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_{DR}	Vcc for Data Retention	See Data Retention Waveform		1.0	2.2	V
I_{DR}	Data Retention Current	Vcc = 1.2V, $\overline{CE} \geq$ Vcc – 0.2V	Com. (-L)	—	15	µA
			Com. (-LL)	—	3	
			Ind. (-L)	—	20	
			Ind. (-LL)	—	5	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		5	—	ns

DATA RETENTION WAVEFORM ($\overline{CE}$ or LB/UB Controlled)



ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
70	IC62VV12816L-70T IC62VV12816L-70B	TSOP-2 6*8mmTF-BGA
100	IC62VV12816L-100T IC62VV12816L-100B	TSOP-2 6*8mmTF-BGA

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
70	IC62VV12816L-70TI IC62VV12816L-70BI	TSOP-2 6*8mmTF-BGA
100	IC62VV12816L-100TI IC62VV12816L-100BI	TSOP-2 6*8mmTF-BGA

ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
70	IC62VV12816LL-70T IC62VV12816LL-70B	TSOP-2 6*8mmTF-BGA
100	IC62VV12816LL-100T IC62VV12816LL-100B	TSOP-2 6*8mmTF-BGA

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
70	IC62VV12816LL-70TI IC62VV12816LL-70BI	TSOP-2 6*8mmTF-BGA
100	IC62VV12816LL-100TI IC62VV12816LL-100BI	TSOP-2 6*8mmTF-BGA

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