

### Advanced Information

- 2 097 152 words by 8-bit organization
- 0 to 70 °C operating temperature
- Performance:

		-50	-60	-70	
t <sub>RAC</sub>	$\overline{\text{RAS}}$ access time	50	60	70	ns
t <sub>CAC</sub>	$\overline{\text{CAS}}$ access time	13	15	20	ns
t <sub>AA</sub>	Access time from address	25	30	35	ns
t <sub>RC</sub>	Read/Write cycle time	90	110	130	ns
t <sub>PC</sub>	Fast page mode cycle time	35	40	45	ns

- Single + 3.3 V ( $\pm 0.3V$ ) supply
- Low power dissipation
  - max. 432 active mW (-50 version)
  - max. 396 active mW (-60 version)
  - max. 360 active mW (-70 version)
  - 7.2 mW standby (LV-TTL)
  - 3.6 mW standby (CMOS)
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify-write,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh,  $\overline{\text{RAS}}$ -only refresh, hidden refresh, self refresh and test mode
- Fast page mode capability
- All inputs, outputs and clocks fully LVTTTL-compatible
- 2048 refresh cycles / 32 ms
- Plastic Package: P-SOJ-28-3 400 mil

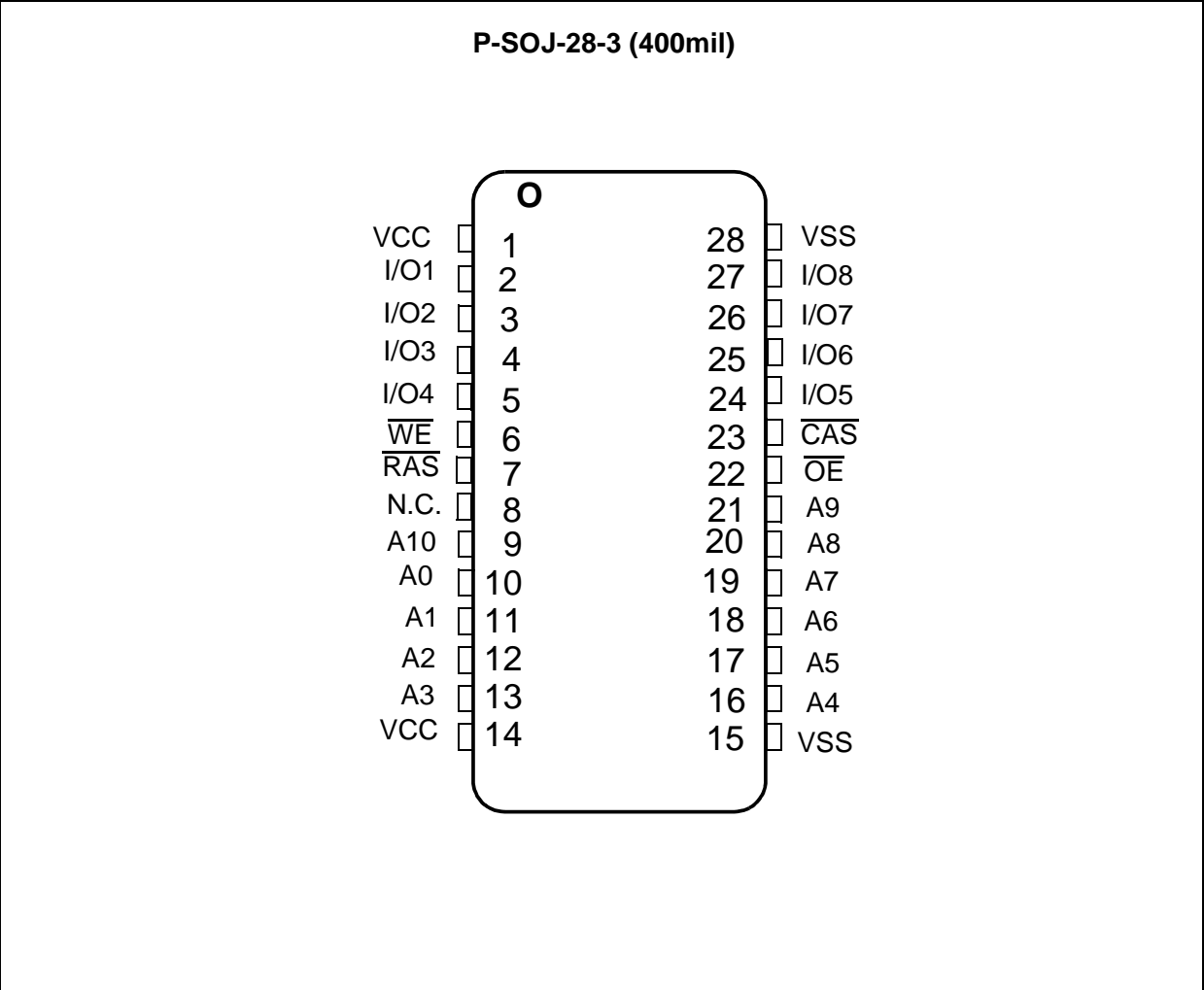
The HYB 3117800BSJ is a 16 MBit dynamic RAM organized as 2097152 words by 8-bits. The HYB 3117800BSJ utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 3117800BSJ to be packaged in a standard SOJ 28 400 mil plastic package. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 3.3 V ( $\pm 0.3V$ ) power supply, direct interfacing with high-performance logic device families.

### Ordering Information

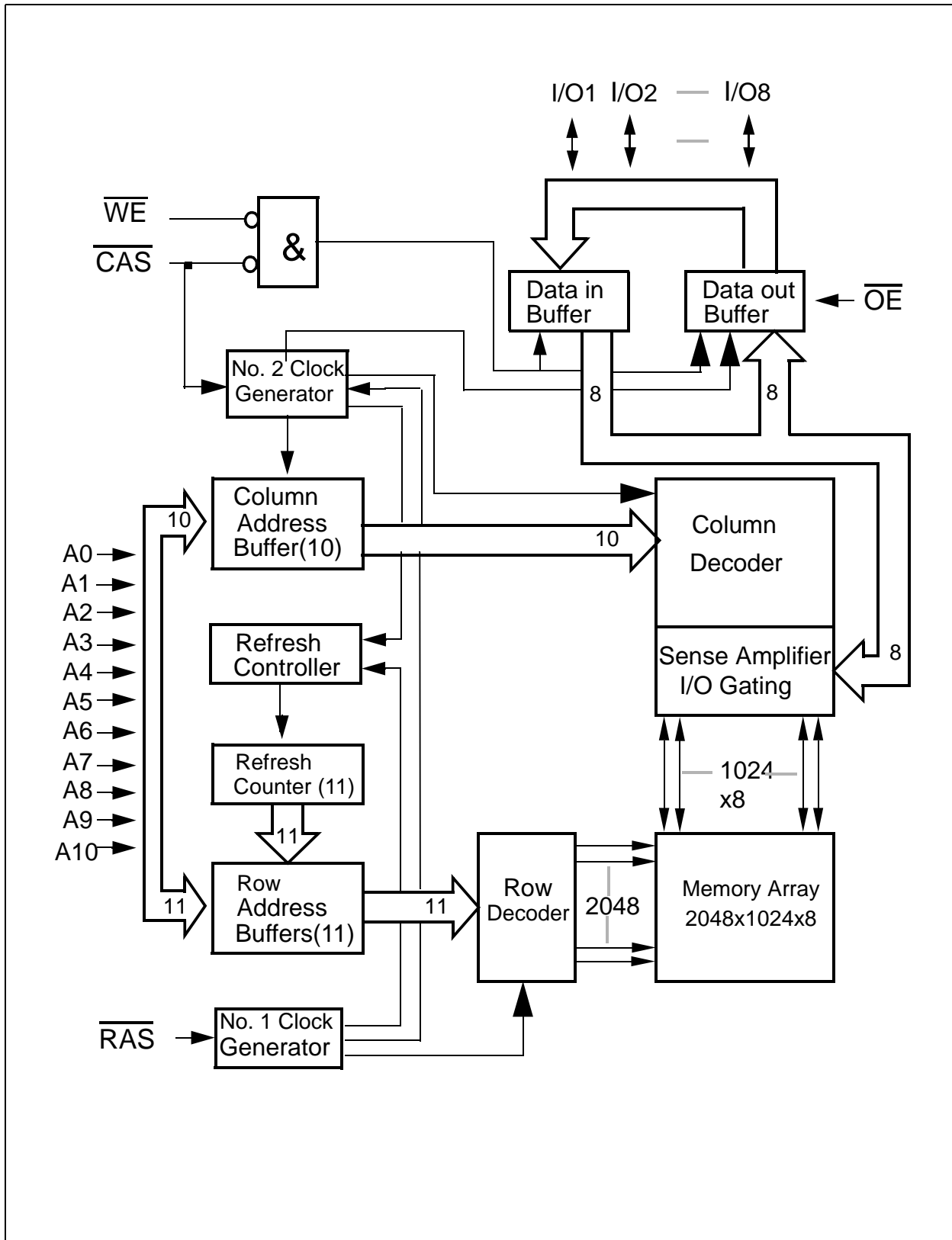
Type	Ordering Code	Package	Descriptions
HYB 3117800BSJ-50	Q67100-Q1147	P-SOJ-28-3 400 mil	3.3V DRAM (access time 50 ns)
HYB 3117800BSJ-60	Q67100-Q1148	P-SOJ-28-3 400 mil	3.3V DRAM (access time 60 ns)
HYB 3117800BSJ-70		P-SOJ-28-3 400 mil	3.3V DRAM (access time 70 ns)

### Pin Names

A0 to A10	Row Address Inputs
A0 to A9	Column Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O8	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
$V_{CC}$	Power Supply (+ 3.3 V)
$V_{SS}$	Ground (0 V)
N.C.	not connected



Pin Configuration



Block Diagram

### Absolute Maximum Ratings

Operating temperature range .....	0 to 70 °C
Storage temperature range.....	- 55 to 150 °C
Input/output voltage .....	-0.5 to min (V <sub>CC</sub> +0.5, 4.6) V
Power supply voltage.....	-1.0V to 4.6 V
Power dissipation.....	0.5 W
Data out current (short circuit) .....	50 mA

### Note:

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC Characteristics

T<sub>A</sub> = 0 to 70 °C, V<sub>SS</sub> = 0 V, V<sub>CC</sub> = 3.3 V ± 0.3V, t<sub>T</sub> = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V <sub>IH</sub>	2.0	V <sub>CC</sub> +0.5	V	1)
Input low voltage	V <sub>IL</sub>	- 0.5	0.8	V	1)
LVTTL Output high voltage (I <sub>OUT</sub> = -2 mA)	V <sub>OH</sub>	2.4	-	V	1)
LVTTL Output low voltage (I <sub>OUT</sub> = 2 mA)	V <sub>OL</sub>	-	0.4	V	1)
CMOS Output high voltage (I <sub>OUT</sub> = -100 μA)	V <sub>OH</sub>	V <sub>CC</sub> -0.2	-	V	
CMOS Output low voltage (I <sub>OUT</sub> = 100 μA)	V <sub>OL</sub>	-	0.2	V	)
Input leakage current, any input (0 V ≤ V <sub>IH</sub> ≤ V <sub>CC</sub> + 0.3V, all other pins = 0 V)	I <sub>I(L)</sub>	- 10	10	μA	1)
Output leakage current (DO is disabled, 0 V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> + 0.3V)	I <sub>O(L)</sub>	- 10	10	μA	1)
Average V <sub>CC</sub> supply current: -50 ns version -60 ns version -70 ns version ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , address cycling, t <sub>RC</sub> = t <sub>RC</sub> min.)	I <sub>CC1</sub>	-	120 110 100	mA mA mA	2) 3) 4) 2) 3) 4) 2) 3) 4)
Standby V <sub>CC</sub> supply current ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$ )	I <sub>CC2</sub>	-	2	mA	-
Average V <sub>CC</sub> supply current, during $\overline{\text{RAS}}$ -only refresh cycles: -50 ns version -60 ns version -70 ns version ( $\overline{\text{RAS}}$ cycling: $\overline{\text{CAS}} = V_{IH}$ , t <sub>RC</sub> = t <sub>RC</sub> min.)	I <sub>CC3</sub>	-	120 110 100	mA mA mA	2) 4) 2) 4) 2) 4)

### DC Characteristics *(cont'd)*

$T_A = 0$  to  $70$  °C,  $V_{SS} = 0$  V,  $V_{CC} = 3.3$  V  $\pm$  0.3V,  $t_T = 5$  ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average $V_{CC}$ supply current, during fast page mode: -50 ns version -60 ns version -70 ns version ( $\overline{RAS} = V_{IL}$ , $\overline{CAS}$ , address cycling, $t_{PC} = t_{PC}$ min.)	$I_{CC4}$	–	40 35 30	mA mA mA	2) 3) 4) 2) 3) 4) 2) 3) 4)
Standby $V_{CC}$ supply current ( $\overline{RAS} = \overline{CAS} = V_{CC} - 0.2$ V)	$I_{CC5}$	–	1	mA	1)
Average $V_{CC}$ supply current, during $\overline{CAS}$ -before-RAS refresh mode: -50 ns version -60 ns version -70 ns version ( $\overline{RAS}$ , $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min.)	$I_{CC6}$	–	120 110 100	mA mA mA	2) 4) 2) 4) 2) 4)
Average Self Refresh Current  (CBR cycle with $t_{RAS} > t_{RASmin.}$ , $\overline{CAS}$ held low, $\overline{WE} = V_{CC} - 0.2$ V, Address and $Din = V_{CC} - 0.2$ V or 0.2V)	$I_{CC7}$	–	1	mA	

### Capacitance

$T_A = 0$  to  $70$  °C,  $V_{CC} = 3.3$  V  $\pm$  0.3V,  $f = 1$  MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10)	$C_{I1}$	–	5	pF
Input capacitance ( $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , $\overline{OE}$ )	$C_{I2}$	–	7	pF
I/O capacitance (I/O1-I/O8)	$C_{IO}$	–	7	pF

### AC Characteristics <sup>5)6)</sup>

16F

$T_A = 0$  to  $70$  °C,  $V_{CC} = 3.3$  V  $\pm$  0.3 V,  $t_T = 5$  ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		

#### *common parameters*

Random read or write cycle time	$t_{RC}$	90	–	110	–	130	–	ns	
$\overline{RAS}$ precharge time	$t_{RP}$	30	–	40	–	50	–	ns	
$\overline{RAS}$ pulse width	$t_{RAS}$	50	10k	60	10k	70	10k	ns	
$\overline{CAS}$ pulse width	$t_{CAS}$	13	10k	15	10k	20	10k	ns	
Row address setup time	$t_{ASR}$	0	–	0	–	0	–	ns	
Row address hold time	$t_{RAH}$	8	–	10	–	10	–	ns	
Column address setup time	$t_{ASC}$	0	–	0	–	0	–	ns	
Column address hold time	$t_{CAH}$	10	–	15	–	15	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$t_{RCD}$	18	37	20	45	20	50		
$\overline{RAS}$ to column address delay time	$t_{RAD}$	13	25	15	30	15	35	ns	
$\overline{RAS}$ hold time	$t_{RSH}$	13		15	–	20	–	ns	
$\overline{CAS}$ hold time	$t_{CSH}$	50		60	–	70	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	$t_{CRP}$	5	–	5	–	5	–	ns	
Transition time (rise and fall)	$t_T$	3	50	3	50	3	50	ns	7
Refresh period	$t_{REF}$	–	32	–	32	–	32	ms	

#### *Read Cycle*

Access time from $\overline{RAS}$	$t_{RAC}$	–	50	–	60	–	70	ns	8, 9
Access time from $\overline{CAS}$	$t_{CAC}$	–	13	–	15	–	20	ns	8, 9
Access time from column address	$t_{AA}$	–	25	–	30	–	35	ns	8,10
$\overline{OE}$ access time	$t_{OEA}$	–	13	–	15	–	20	ns	
Column address to $\overline{RAS}$ lead time	$t_{RAL}$	25	–	30	–	35	–	ns	
Read command setup time	$t_{RCS}$	0	–	0	–	0	–	ns	
Read command hold time	$t_{RCH}$	0	–	0	–	0	–	ns	11
Read command hold time referenced to $\overline{RAS}$	$t_{RRH}$	0	–	0	–	0	–	ns	11
$\overline{CAS}$ to output in low-Z	$t_{CLZ}$	0	–	0	–	0	–	ns	8
Output buffer turn-off delay	$t_{OFF}$	0	13	0	15	0	20	ns	12

### AC Characteristics (cont'd) 5)6)

16F

 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}, V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, t_T = 5 \text{ ns}$ 

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
Output buffer turn-off delay from $\overline{\text{OE}}$	$t_{\text{OEZ}}$	0	13	0	15	0	20	ns	12
Data to $\overline{\text{OE}}$ low delay	$t_{\text{DZO}}$	0	–	0	–	0	–	ns	13
$\overline{\text{CAS}}$ high to data delay	$t_{\text{CDD}}$	13	–	15	–	20	–	ns	14
$\overline{\text{OE}}$ high to data delay	$t_{\text{ODD}}$	13	–	15	–	20	–	ns	14

### Write Cycle

Write command hold time	$t_{\text{WCH}}$	8	–	10	–	10	–	ns	
Write command pulse width	$t_{\text{WP}}$	8	–	10	–	10	–	ns	
Write command setup time	$t_{\text{WCS}}$	0	–	0	–	0	–	ns	15
Write command to $\overline{\text{RAS}}$ lead time	$t_{\text{RWL}}$	13	–	15	–	20	–	ns	
Write command to $\overline{\text{CAS}}$ lead time	$t_{\text{CWL}}$	13	–	15	–	20	–	ns	
Data setup time	$t_{\text{DS}}$	0	–	0	–	0	–	ns	16
Data hold time	$t_{\text{DH}}$	10	–	10	–	15	–	ns	16
Data to $\overline{\text{CAS}}$ low delay	$t_{\text{DZC}}$	0	–	0	–	0	–	ns	13

### Read-Modify-Write Cycle

Read-write cycle time	$t_{\text{RWC}}$	126	–	150	–	180	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	$t_{\text{RWD}}$	68	–	80	–	95	–	ns	15
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	$t_{\text{CWD}}$	31	–	35	–	45	–	ns	15
Column address to $\overline{\text{WE}}$ delay time	$t_{\text{AWD}}$	43	–	50	–	60	–	ns	15
$\overline{\text{OE}}$ command hold time	$t_{\text{OEH}}$	13	–	15	–	20	–	ns	

### Fast Page Mode Cycle

Fast page mode cycle time	$t_{\text{PC}}$	35	–	40	–	45	–	ns	
$\overline{\text{CAS}}$ precharge time	$t_{\text{CP}}$	10	–	10	–	10	–	ns	
Access time from $\overline{\text{CAS}}$ precharge	$t_{\text{CPA}}$	–	30	–	35	–	40	ns	7
$\overline{\text{RAS}}$ pulse width	$t_{\text{RAS}}$	50	200k	60	200k	70	200k	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{RAS}}$ Delay	$t_{\text{RHPC}}$	30	–	35	–	40	–	ns	



### AC Characteristics (cont'd) 5)6)

16F

 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}, V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, t_T = 5 \text{ ns}$ 

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		

#### Fast Page Mode Read-Modify-Write Cycle

Fast page mode read-write cycle time	$t_{PRWC}$	71	–	80	–	95	–	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$	$t_{CPWD}$	48	–	55	–	65	–	ns	

#### $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle

$\overline{\text{CAS}}$ setup time	$t_{CSR}$	10	–	10	–	10	–	ns	
$\overline{\text{CAS}}$ hold time	$t_{CHR}$	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	$t_{RPC}$	5	–	5	–	5	–	ns	
Write to $\overline{\text{RAS}}$ precharge time	$t_{WRP}$	10	–	10	–	10	–	ns	
Write hold time referenced to $\overline{\text{RAS}}$	$t_{WRH}$	10	–	10	–	10	–	ns	

#### $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Counter Test Cycle

$\overline{\text{CAS}}$ precharge time	$t_{CPT}$	35	–	40	–	40	–	ns	
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#### Test Mode

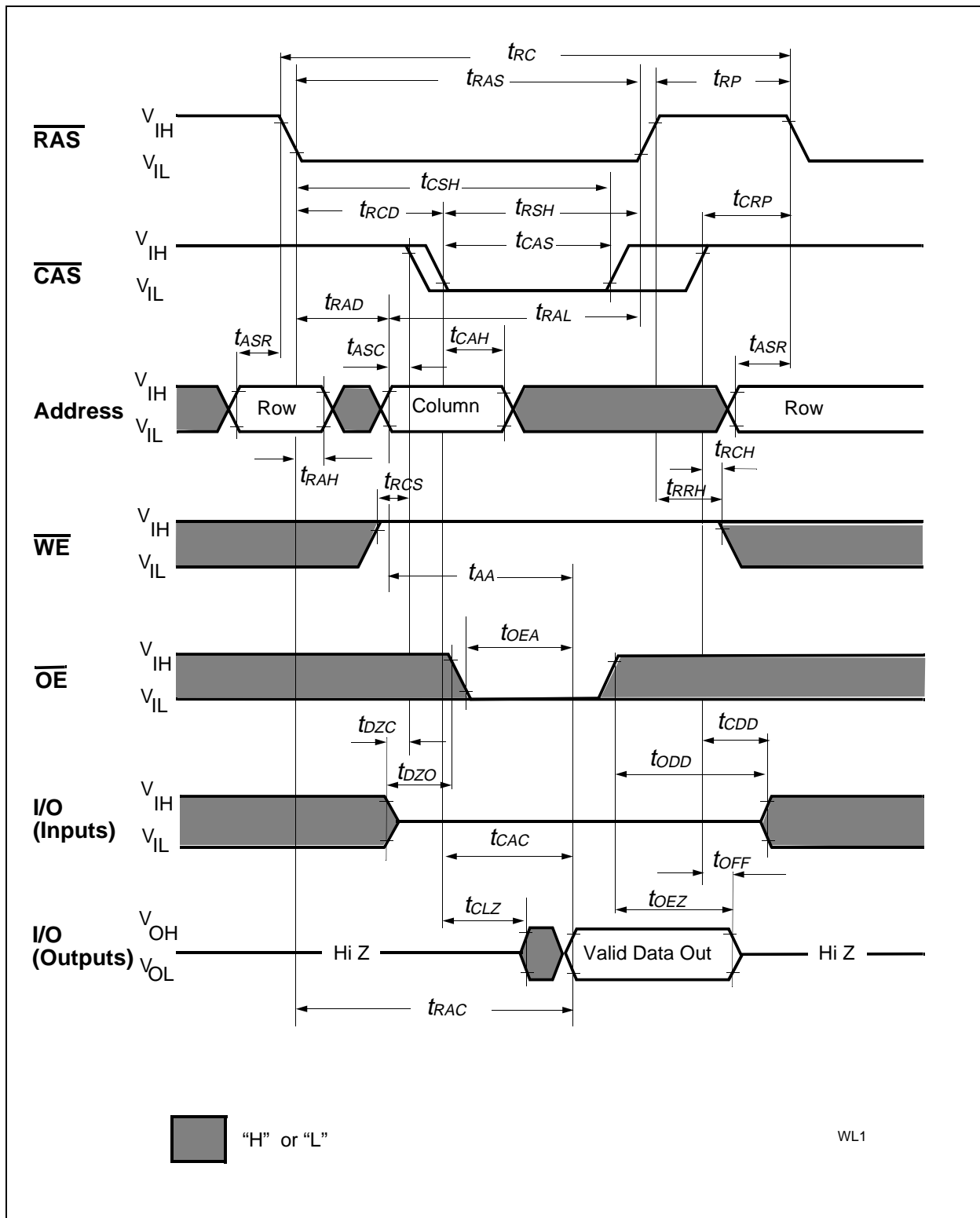
$\overline{\text{CAS}}$ hold time	$t_{CHRT}$	30	–	30	–	30	–	ns	
Write command setup time	$t_{WTS}$	10	–	10	–	10	–	ns	
Write command hold time	$t_{WTH}$	10	–	10	–	10	–	ns	

#### Self Refresh Cycle

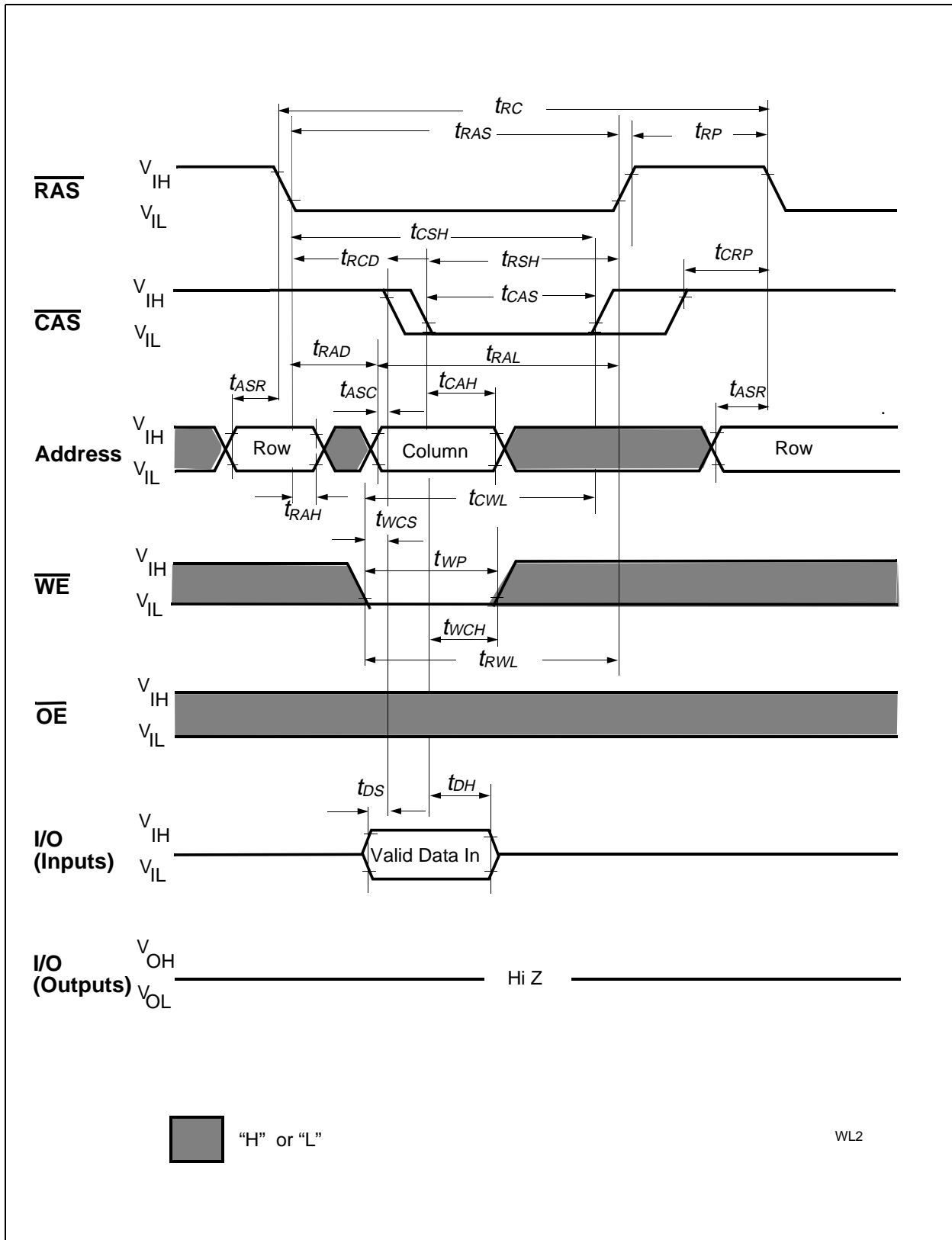
$\overline{\text{RAS}}$ pulse width	$t_{RASS}$	100k	–	100k	–	100k	–	ns	17
$\overline{\text{RAS}}$ precharge time	$t_{RPS}$	95	–	110	–	130	–	ns	17
$\overline{\text{CAS}}$ hold time	$t_{CHS}$	-50	–	-50	–	-50	–	ns	17

**Notes:**

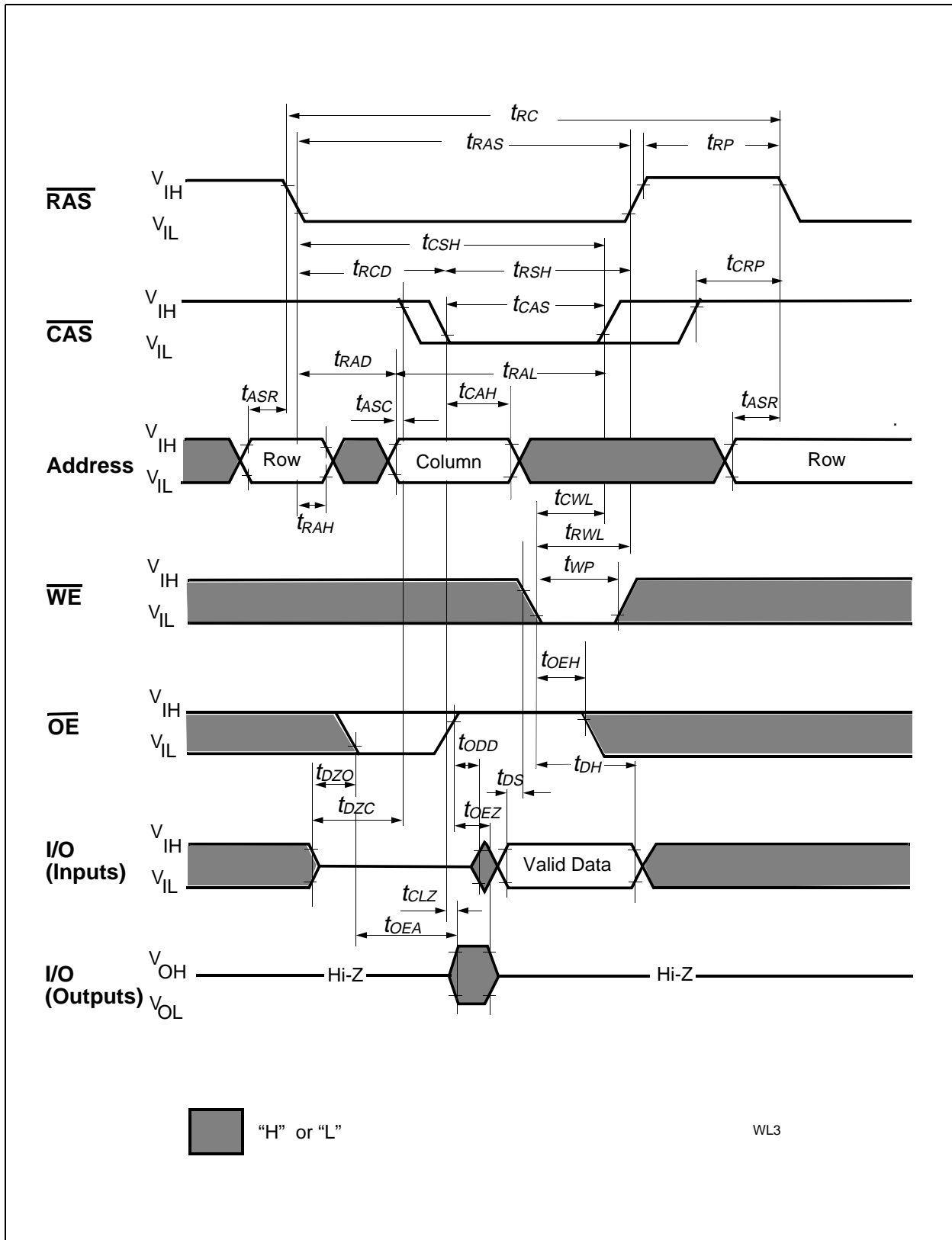
- 1) All voltages are referenced to VSS.
- 2) ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.
- 3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.
- 4) Address can be changed once or less while  $\overline{\text{RAS}} = \text{VIL}$ . In the case of ICC4 it can be changed once or less during a fast page mode cycle (tPC).
- 5) An initial pause of 200  $\mu\text{s}$  is required after power-up followed by 8 RAS cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.
- 6) AC measurements assume  $t_T = 5 \text{ ns}$ .
- 7)  $V_{IH}$  (min.) and  $V_{IL}$  (max.) are reference levels for measuring timing of input signals. Transition times are also measured between  $V_{IH}$  and  $V_{IL}$ .
- 8) Measured with a load equivalent to 100 pF and at  $V_{oh}=2.0 \text{ V}$  ( $I_{oh} = -2\text{mA}$ ),  $V_{ol}=0.8\text{V}$  ( $I_{ol}=2\text{mA}$ ).
- 9) Operation within the tRCD (max.) limit ensures that tRAC (max.) can be met. tRCD (max.) is specified as a reference point only: If tRCD is greater than the specified tRCD (max.) limit, then access time is controlled by tCAC.
- 10) Operation within the tRAD (max.) limit ensures that tRAC (max.) can be met. tRAD (max.) is specified as a reference point only: If tRAD is greater than the specified tRAD (max.) limit, then access time is controlled by tAA.
- 11) Either tRCH or tRRH must be satisfied for a read cycle.
- 12) tOFF (max.) and tOEZ (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
- 13) Either tDZC or tDZO must be satisfied.
- 14) Either tCDD or tODD must be satisfied.
- 15) tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $tWCS > tWCS \text{ (min.)}$ , the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if  $tRWD > tRWD \text{ (min.)}$ ,  $tCWD > tCWD \text{ (min.)}$ ,  $tAWD > tAWD \text{ (min.)}$  and  $tCPWD > tCPWD \text{ (min.)}$ , the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
- 16) These parameters are referenced to the CAS leading edge in early write cycles and to the WE leading edge in read-write cycles.
- 17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:  
  
If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.  
  
If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.



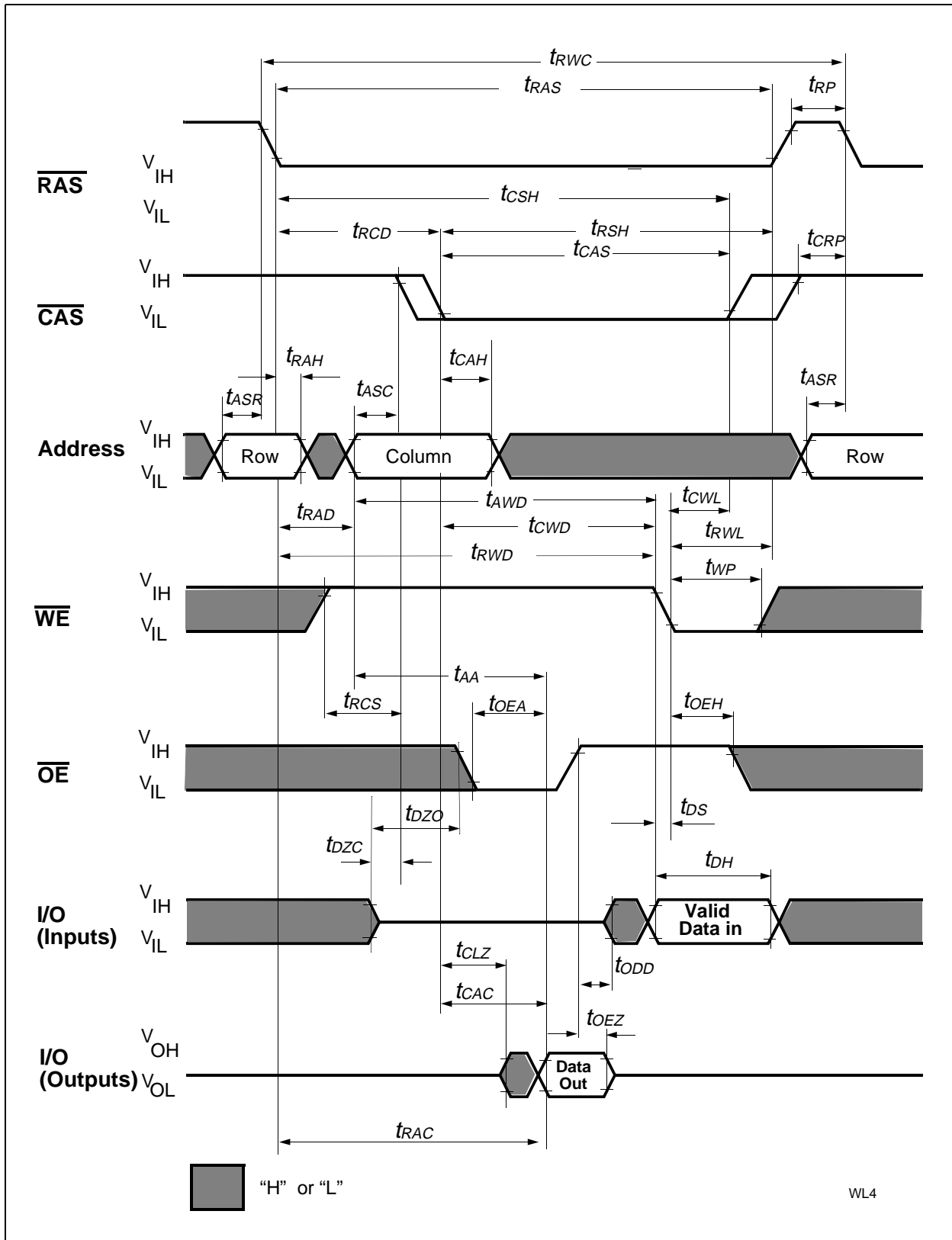
Read Cycle



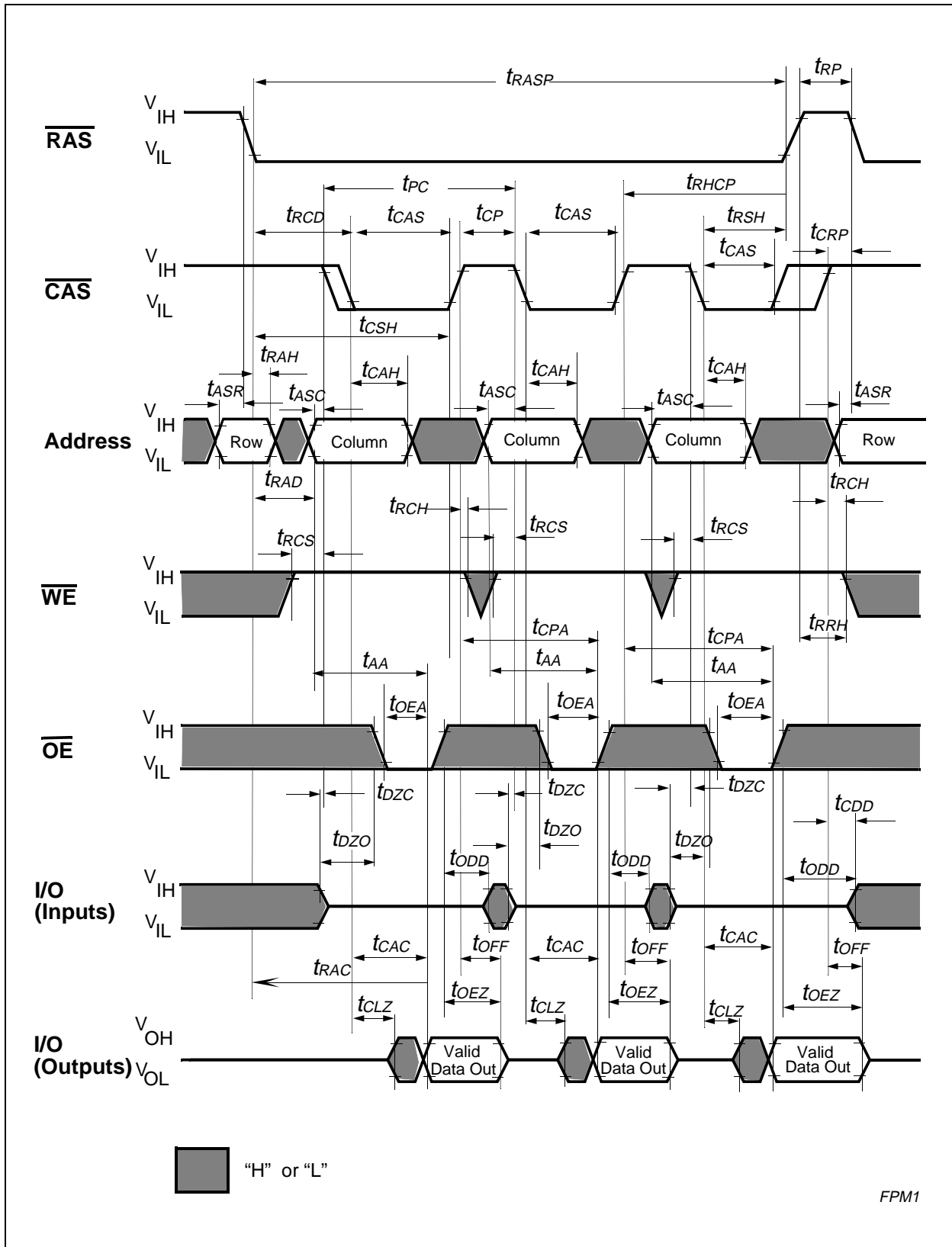
Write Cycle (Early Write)



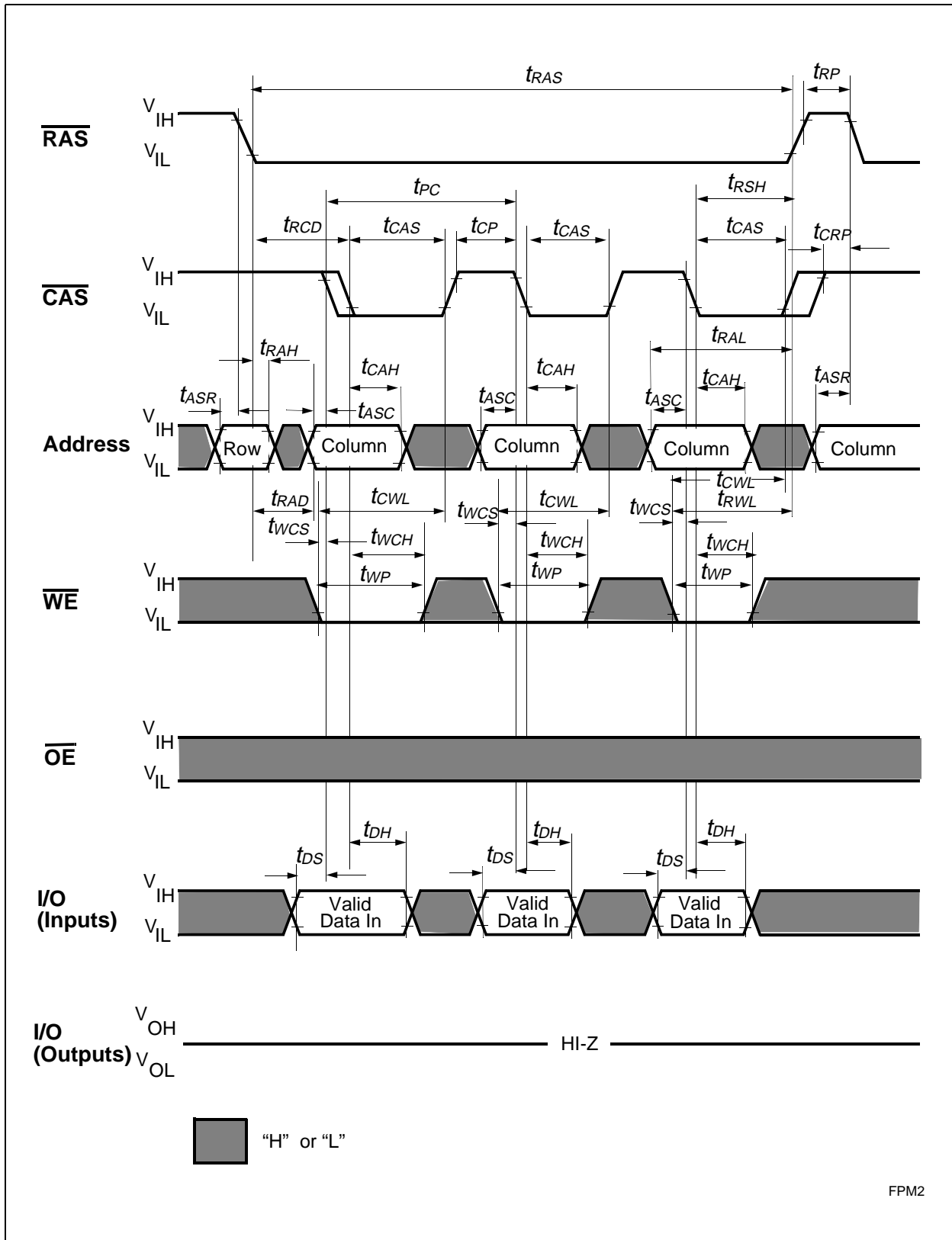
Write Cycle ( $\overline{OE}$  Controlled Write)



Read-Write (Read-Modify-Write) Cycle



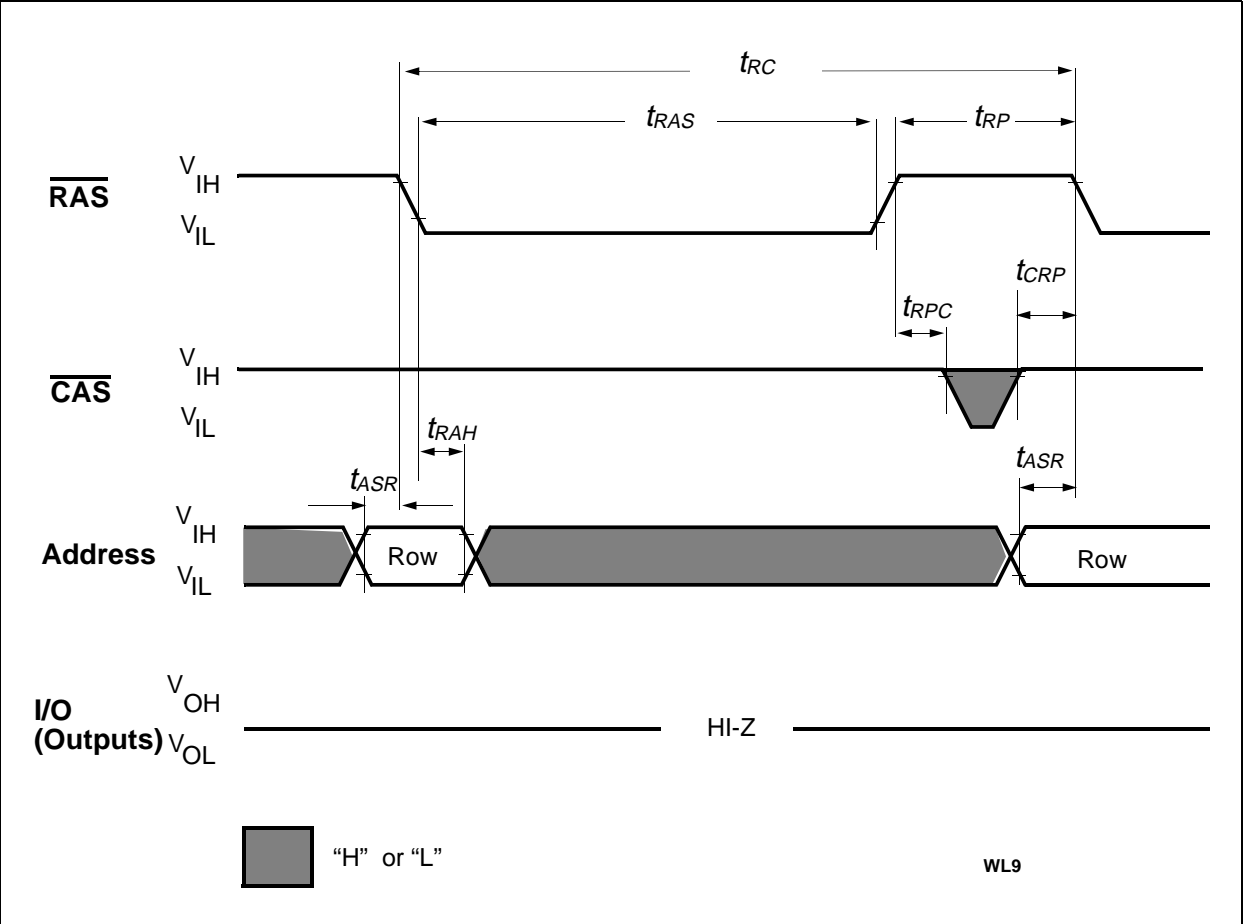
Fast Page Mode Read Cycle



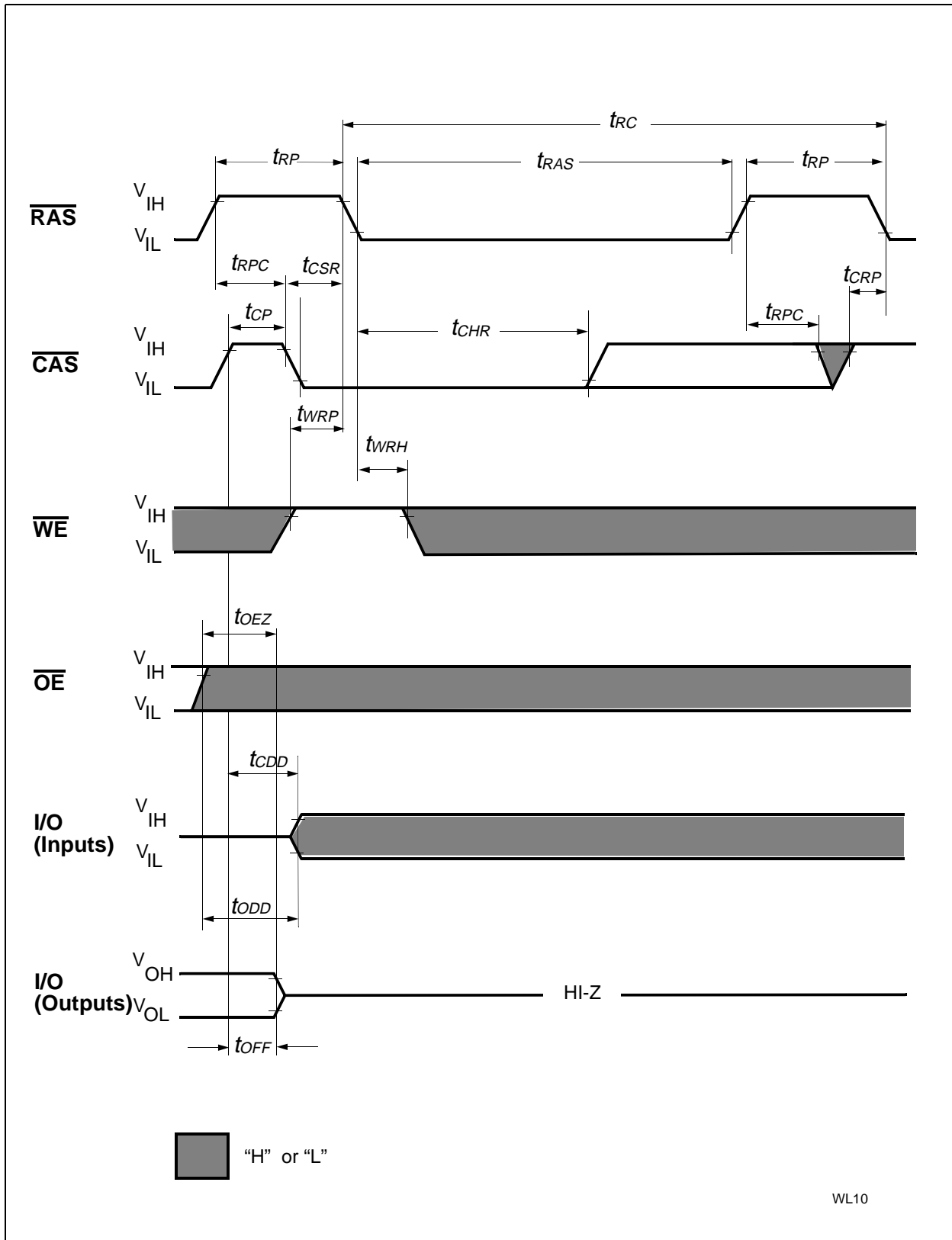
Fast Page Mode Early Write Cycle



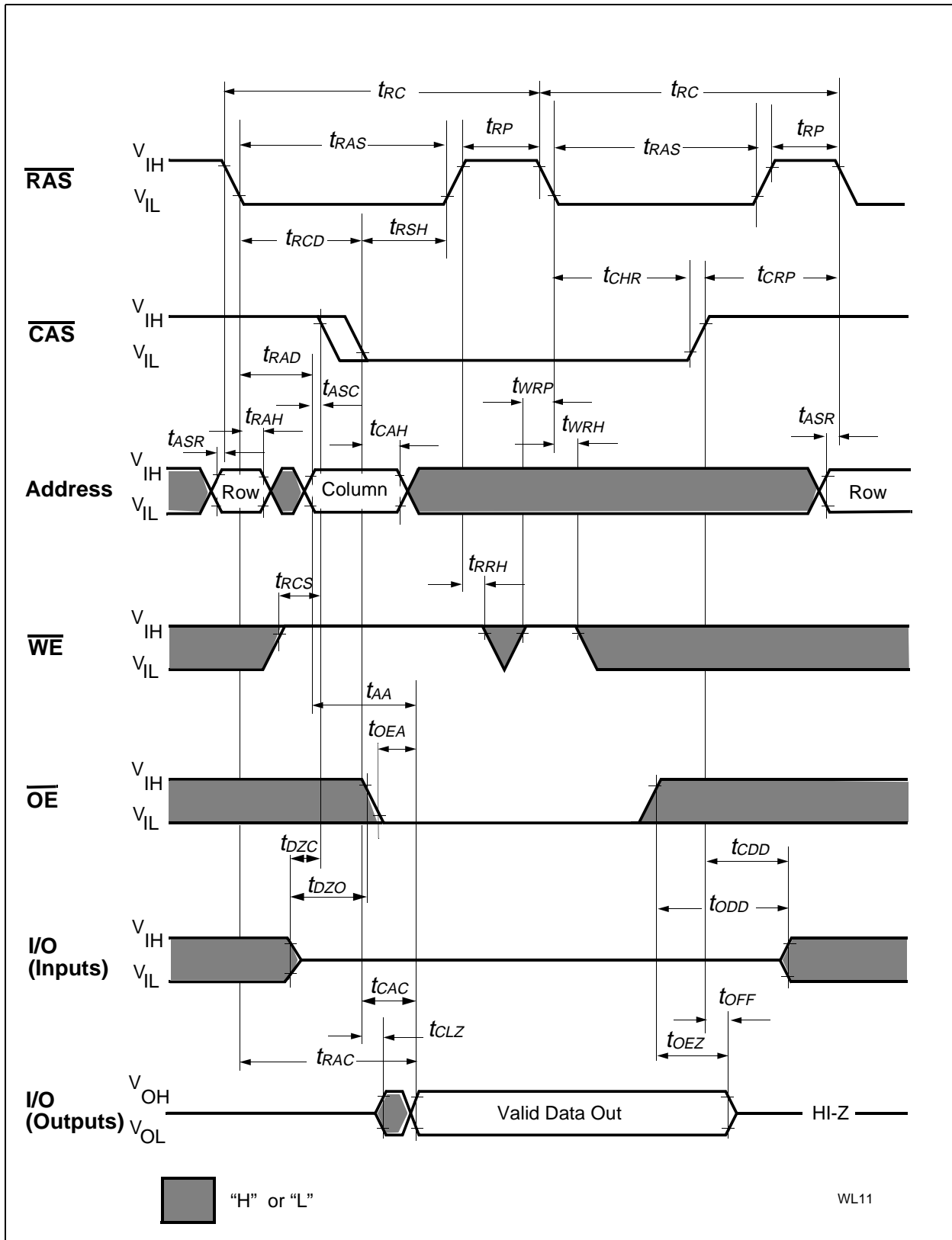




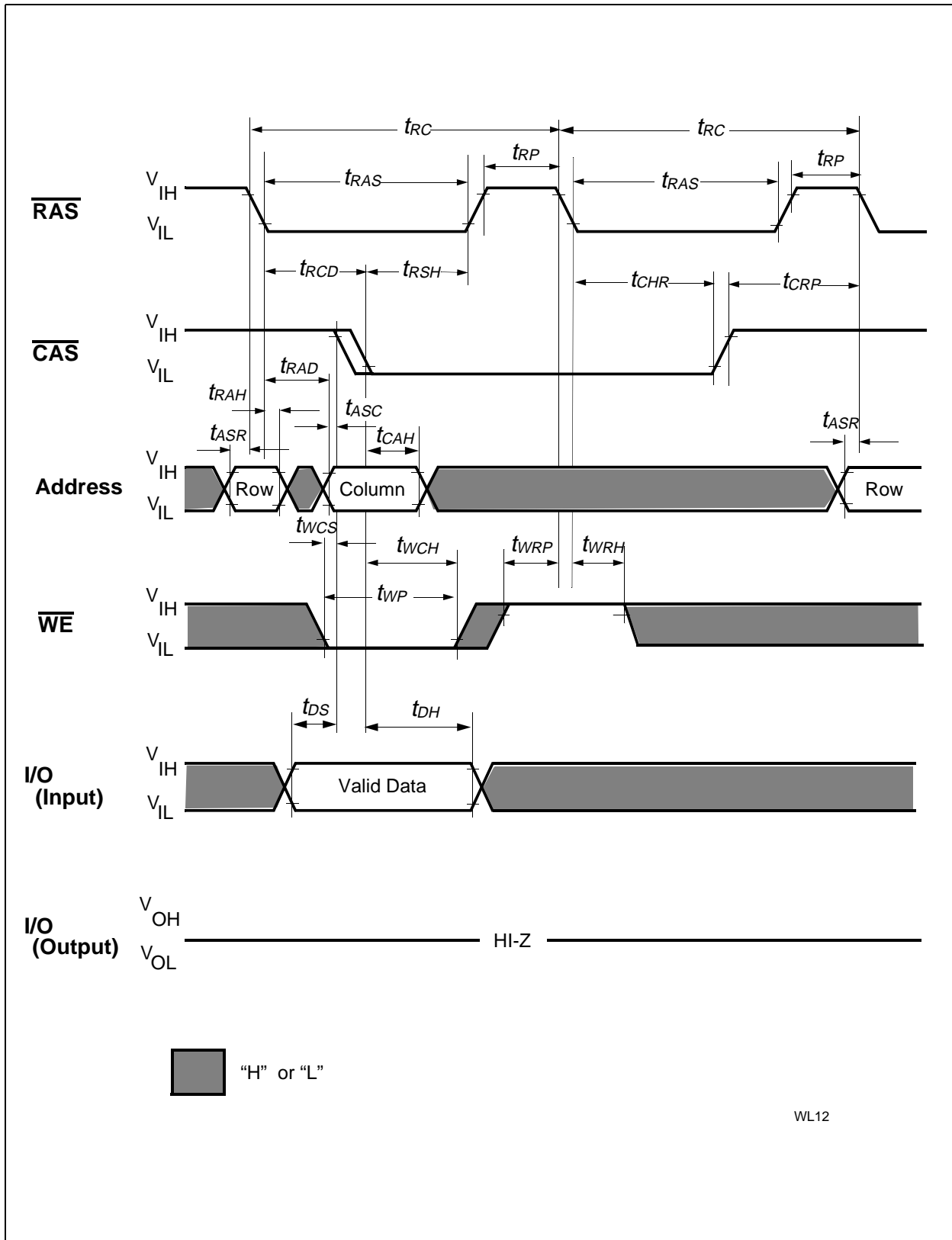
$\overline{\text{RAS}}$ -Only Refresh Cycle



**CAS-Before-RAS Refresh Cycle**

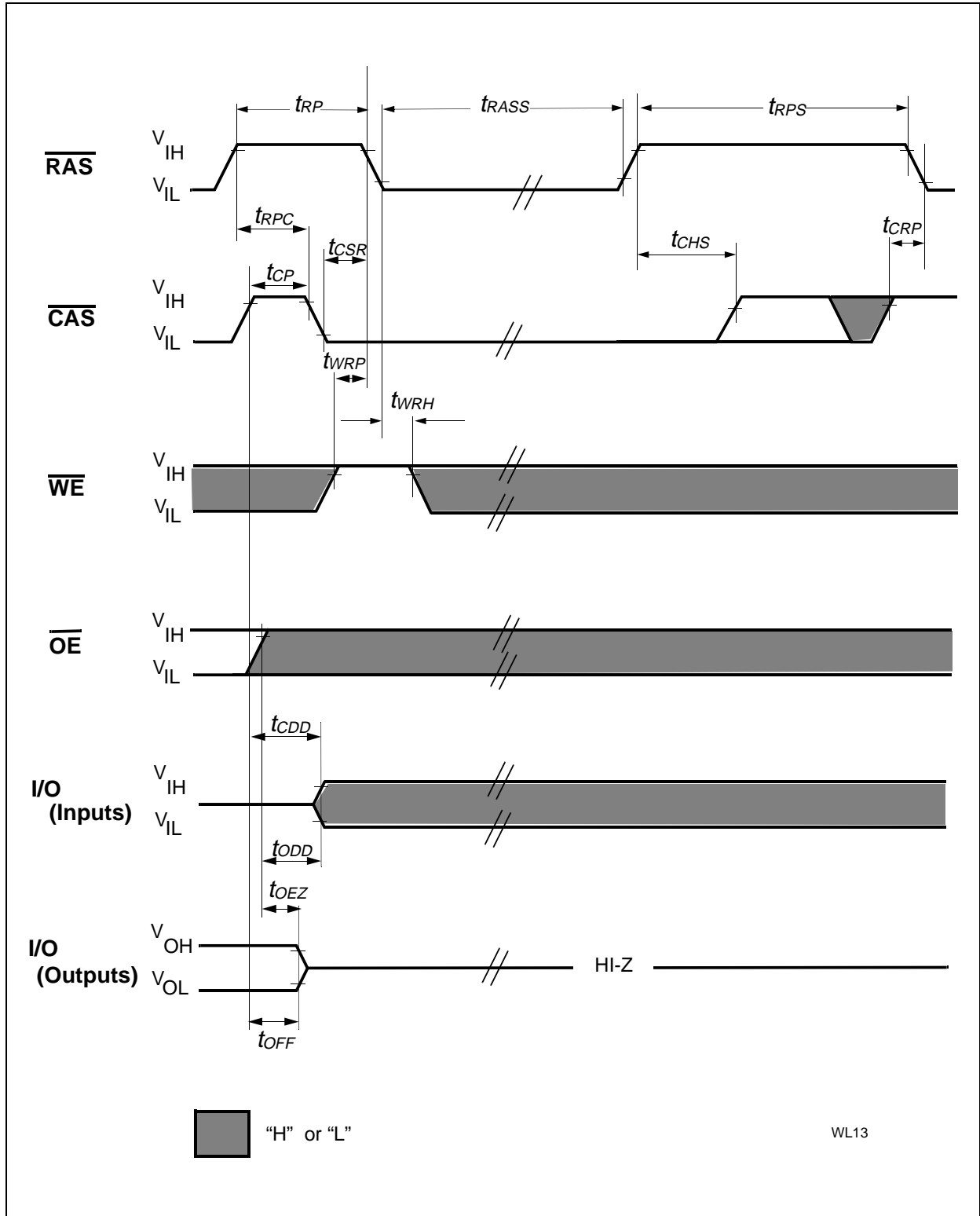


Hidden Refresh Cycle (Read) Cycle

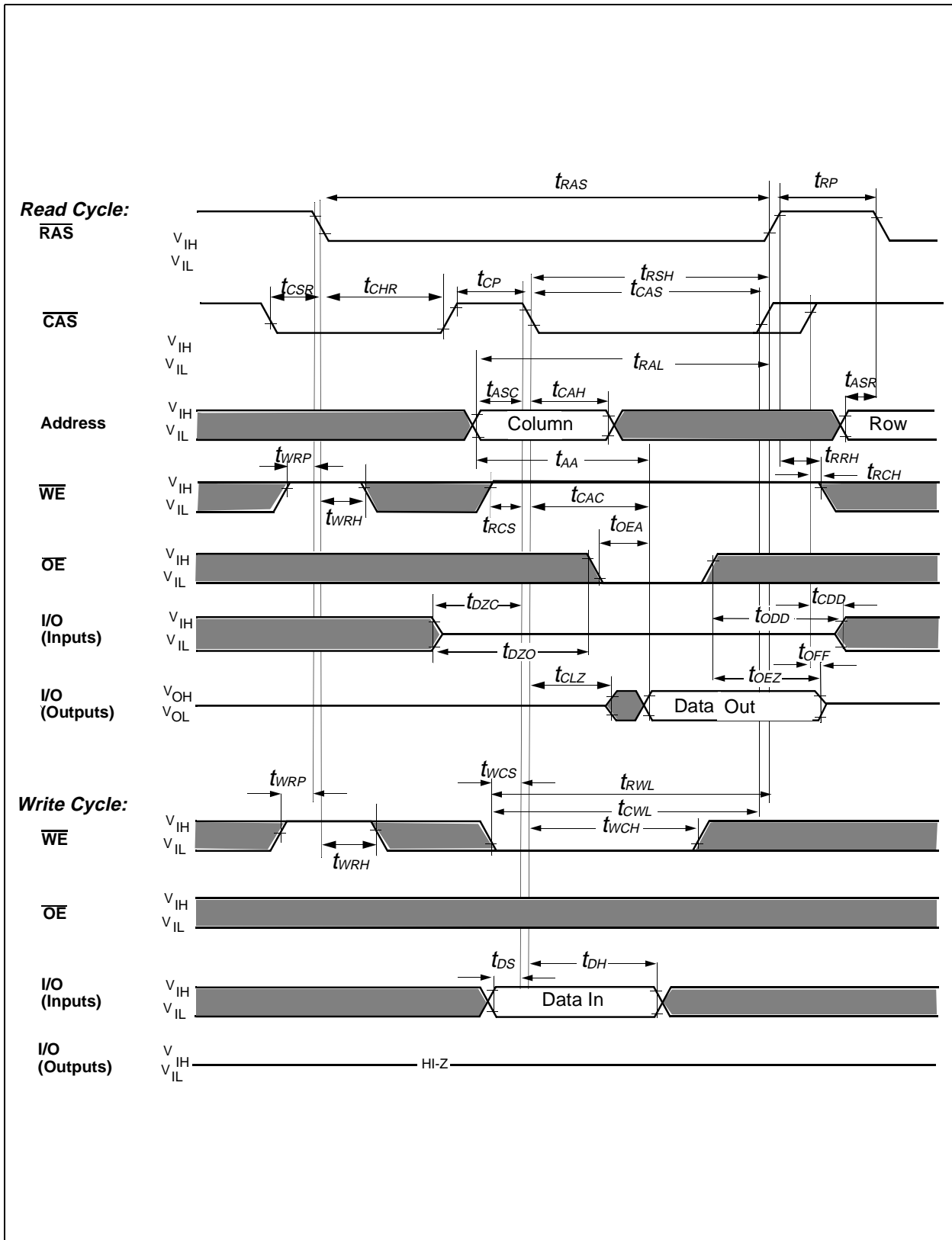


WL12

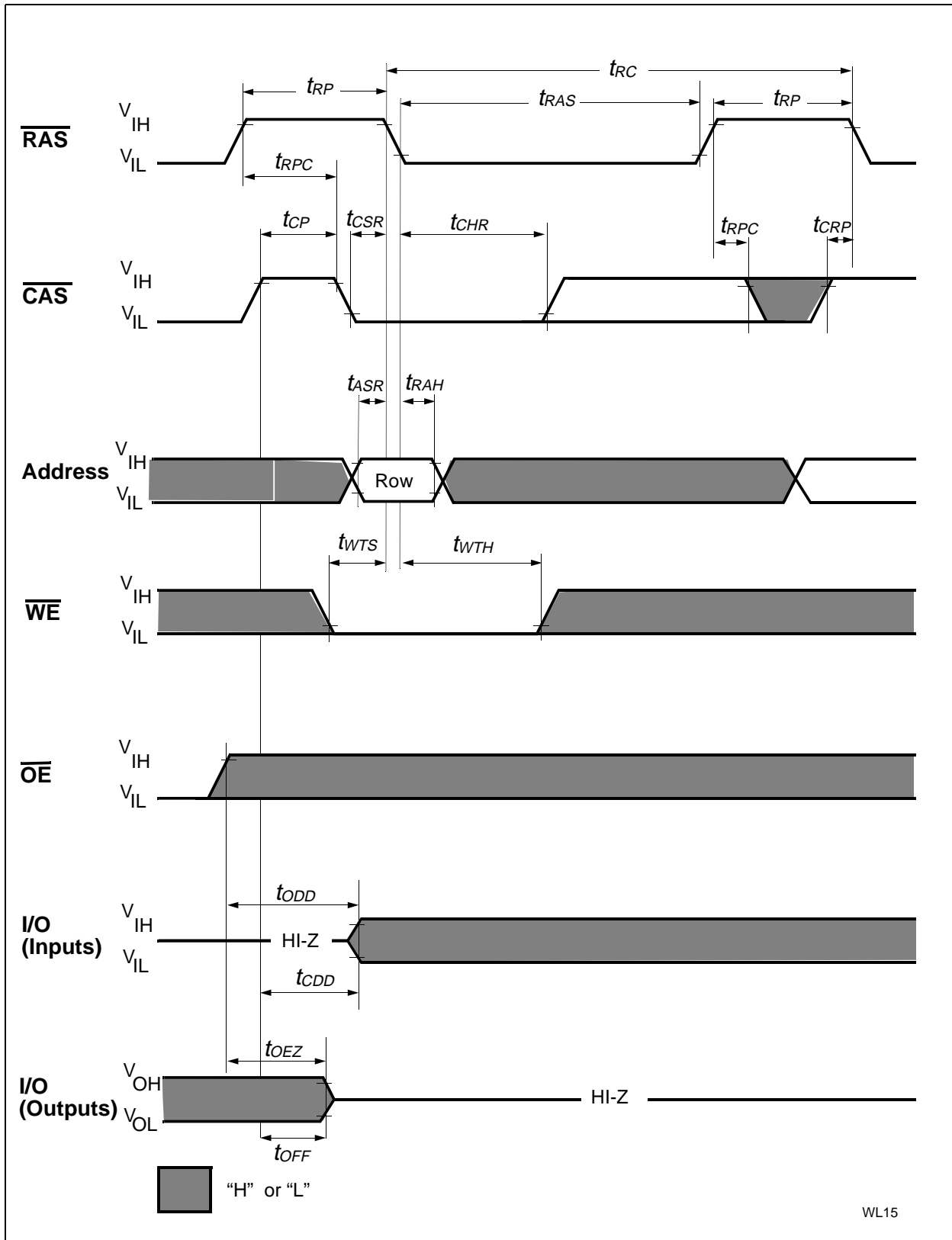
Hidden Refresh Cycle (Early Write)



$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  Self Refresh Cycle



**CAS-Before-RAS Refresh Counter Test Cycle**



WL15

Test Mode Entry



**Test Mode**

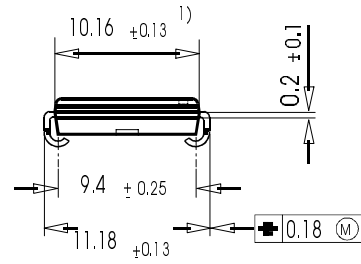
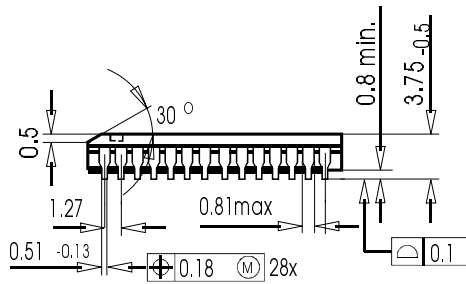
As the HYB 3117800BSJ is organized internally as 1M x 16-bits, a test mode cycle using 2:1 compression can be used to improve test time. Note that in the 2M x 8 version the test time is reduced by 1/2 for a N test pattern.

In a test mode “write” the data from each I/O pin is written into two 1M blocks simultaneously (all “1” s or all “0” s). In test mode “read” each I/O output is used for indicating the test mode result. If the internal two bits are equal, the I/O would indicate a “1”. If they were not equal, the I/O would indicate a “0”. The WCBR cycle ( $\overline{WE}$ ,  $\overline{CAS}$  before  $\overline{RAS}$ ) puts the device into test mode. To exit from test mode, a “ $\overline{CAS}$  before  $\overline{RAS}$  refresh”, “ $\overline{RAS}$  only refresh” or “Hidden refresh” can be used. Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles.

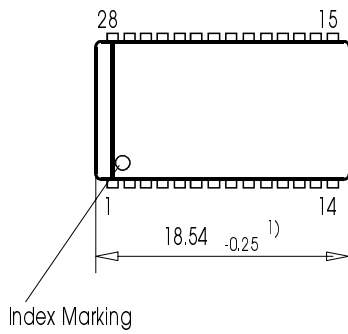
Row addresses A0 through A9 have to be kept high to perform a testmode entry cycle. All other addresses are don't care.

### Package Outlines

#### Plastic Package P-SOJ-28-3 (400 mil) (Small Outline J-lead, SMD)



GPJ05699



1) Does not include plastic or metal protrusion of 0.15 max. per side