

# TRIPLE 2-CHANNEL ANALOGUE MULTIPLEXER/DEMULTIPLEXER



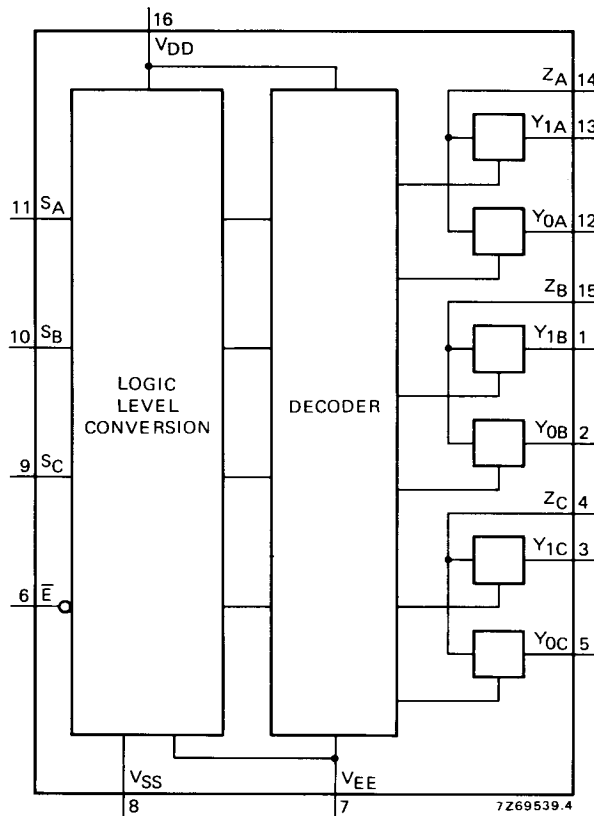
The HEF4053B is a triple 2-channel analogue multiplexer/demultiplexer with a common enable input ( $\bar{E}$ ). Each multiplexer/demultiplexer has two independent inputs/outputs ( $Y_0$  and  $Y_1$ ), a common input/output ( $Z$ ), and select inputs ( $S_n$ ). Each also contains two-bidirectional analogue switches, each with one side connected to an independent input/output ( $Y_0$  and  $Y_1$ ) and the other side connected to a common input/output ( $Z$ ).

With  $\bar{E}$  LOW, one of the two switches is selected (low impedance ON-state) by  $S_n$ . With  $\bar{E}$  HIGH, all switches are in the high impedance OFF-state, independent of  $S_A$  to  $S_C$ .

$V_{DD}$  and  $V_{SS}$  are the supply voltage connections for the digital control inputs ( $S_A$  to  $S_C$  and  $\bar{E}$ ). The  $V_{DD}$  to  $V_{SS}$  range is 3 to 15 V. The analogue inputs/outputs ( $Y_0$ ,  $Y_1$  and  $Z$ ) can swing between  $V_{DD}$  as a positive limit and  $V_{EE}$  as a negative limit.  $V_{DD}-V_{EE}$  may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer,  $V_{EE}$  is connected to  $V_{SS}$  (typically ground).

Fig. 1 Functional diagram.



## FAMILY DATA

$I_{DD}$  LIMITS category MSI  
see Family Specifications

# HEF4053B

MSI



Fig. 2 Pinning diagram.

### PINNING

- Y<sub>0A</sub> to Y<sub>0C</sub> independent inputs/outputs
- Y<sub>1A</sub> to Y<sub>1C</sub> independent inputs/outputs
- S<sub>A</sub> to S<sub>C</sub> select inputs
- $\bar{E}$  enable input (active LOW)
- Z<sub>A</sub> to Z<sub>C</sub> common inputs/outputs

- HEF4053BP : 16-lead DiL; plastic (SOT-38Z).
- HEF4053BD : 16-lead DiL; ceramic (cerdip) (SOT-74).
- HEF4053BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

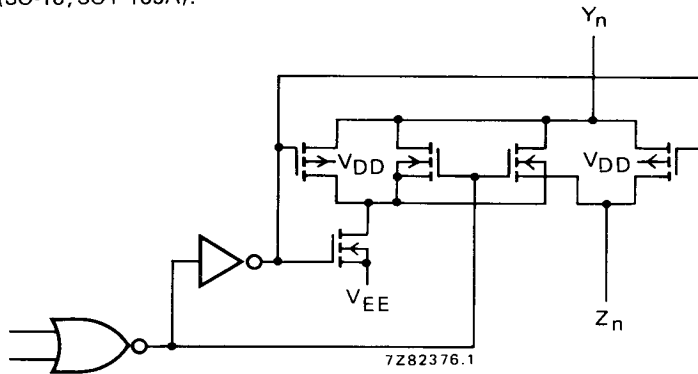


Fig. 3 Schematic diagram (one switch).

### FUNCTION TABLE

inputs		channel ON
$\bar{E}$	S <sub>n</sub>	
L	L	Y <sub>0n</sub> -Z <sub>n</sub>
L	H	Y <sub>1n</sub> -Z <sub>n</sub>
H	X	none

- H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial

### RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (with reference to V<sub>DD</sub>) V<sub>EE</sub> -18 to +0,5 V

### NOTE

To avoid drawing V<sub>DD</sub> current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V<sub>DD</sub> current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V<sub>DD</sub> or V<sub>EE</sub>.

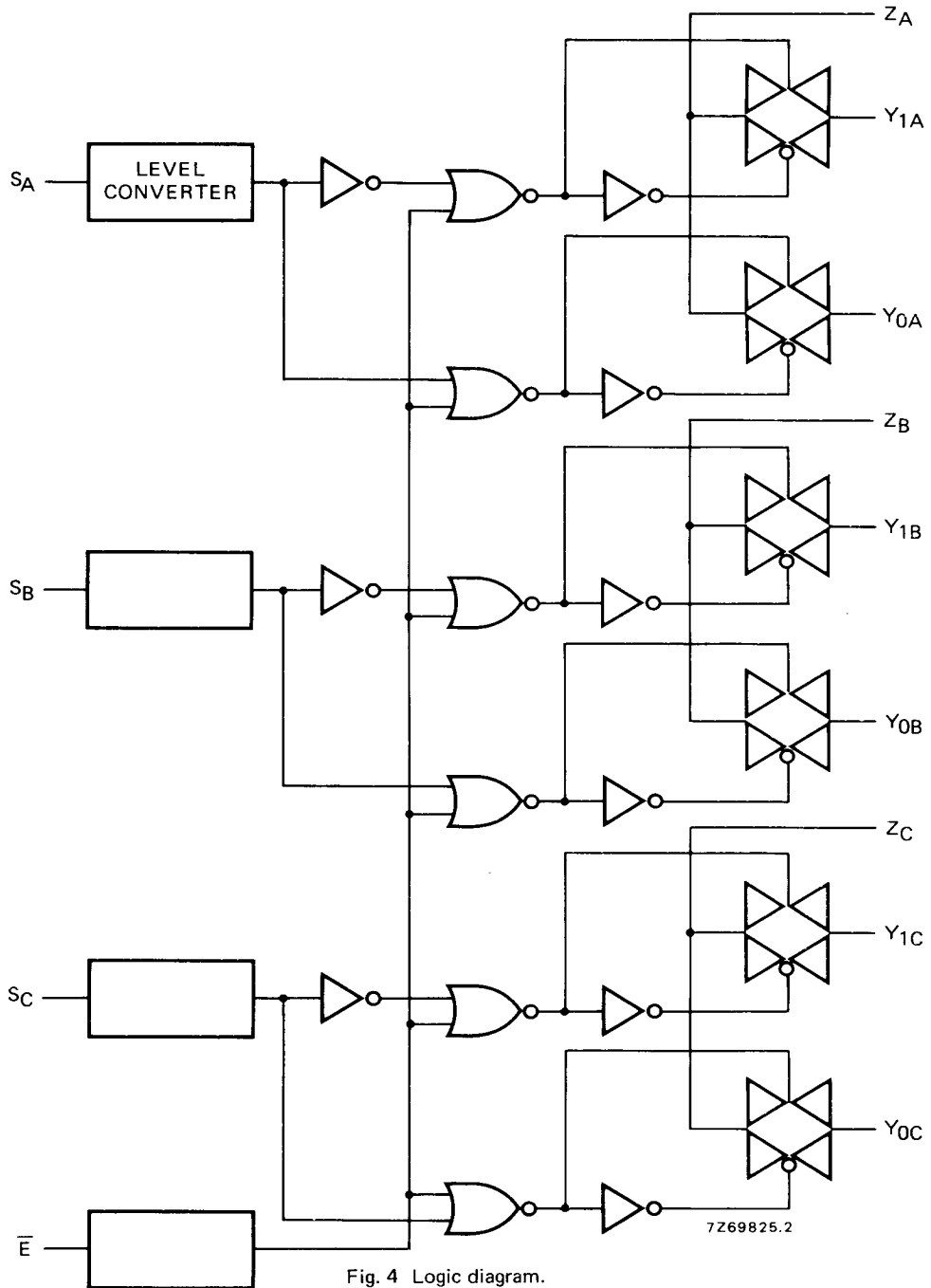


Fig. 4 Logic diagram.

## D.C. CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$ 

	$V_{DD}-V_{EE}$ V	symbol	typ.	max.		conditions
ON resistance	5	$R_{ON}$	350	2500	$\Omega$	} $V_{is} = 0$ to $V_{DD}-V_{EE}$ see Fig. 6
	10		80	245	$\Omega$	
	15		60	175	$\Omega$	
ON resistance	5	$R_{ON}$	115	340	$\Omega$	} $V_{is} = 0$ see Fig. 6
	10		50	160	$\Omega$	
	15		40	115	$\Omega$	
ON resistance	5	$R_{ON}$	120	365	$\Omega$	} $V_{is} = V_{DD}-V_{EE}$ see Fig. 6
	10		65	200	$\Omega$	
	15		50	155	$\Omega$	
' $\Delta$ ' ON resistance between any two channels	5	$\Delta R_{ON}$	25	—	$\Omega$	} $V_{is} = 0$ to $V_{DD}-V_{EE}$ see Fig. 6
	10		10	—	$\Omega$	
	15		5	—	$\Omega$	
OFF-state leakage current, all channels OFF	5	$I_{OZZ}$	—	—	nA	} $\bar{E}$ at $V_{DD}$
	10		—	—	nA	
	15		—	1000	nA	
OFF-state leakage current, any channel	5	$I_{OZY}$	—	—	nA	} $\bar{E}$ at $V_{SS}$
	10		—	—	nA	
	15		—	200	nA	

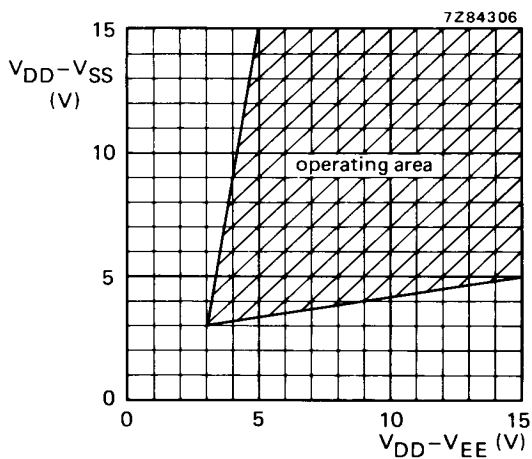


Fig. 5 Operating area as a function of the supply voltages.

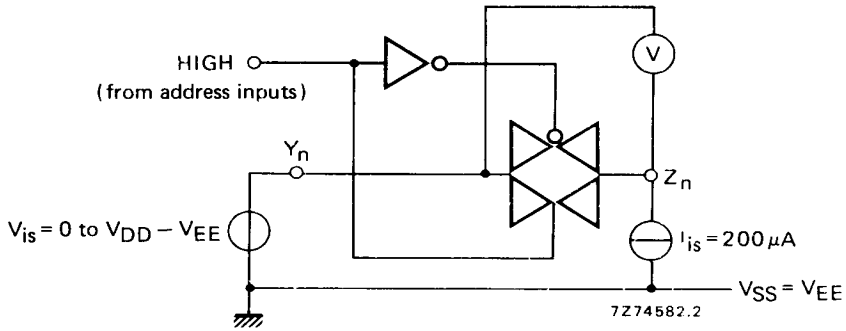


Fig. 6 Test set-up for measuring  $R_{ON}$ .

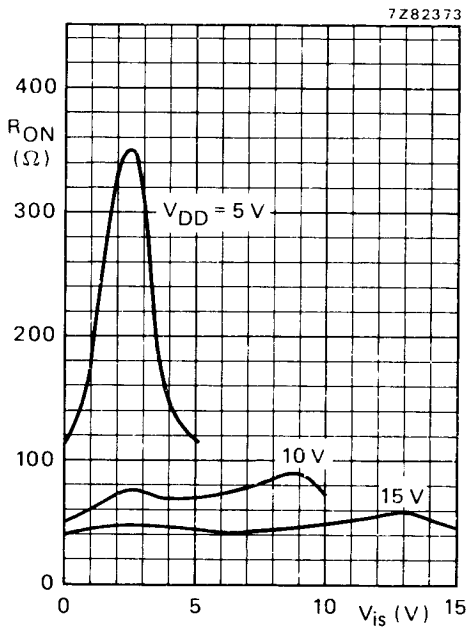


Fig. 7 Typical  $R_{ON}$  as a function of input voltage.

$I_{is} = 200 \mu A$   
 $V_{SS} = V_{EE} = 0 V$

## A.C. CHARACTERISTICS

 $V_{EE} = V_{SS} = 0 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; input transition times  $\leq 20 \text{ ns}$ 

	$V_{DD}$ V	typical formula for P ( $\mu\text{W}$ )	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)
Dynamic power dissipation per package (P)	5	$2\,500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$11\,500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$29\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

## A.C. CHARACTERISTICS

 $V_{EE} = V_{SS} = 0 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; input transition times  $\leq 20 \text{ ns}$ 

	$V_{DD}$ V	symbol	typ.	max.		
Propagation delays $V_{is} \rightarrow V_{os}$ HIGH to LOW	5	tPHL	10	20	ns	} note 1
	10		5	10	ns	
	15		5	10	ns	
LOW to HIGH	5	tPLH	15	30	ns	} note 1
	10		5	10	ns	
	15		5	10	ns	
$S_n \rightarrow V_{os}$ HIGH to LOW	5	tPHL	200	400	ns	} note 2
	10		85	170	ns	
	15		65	130	ns	
LOW to HIGH	5	tPLH	275	555	ns	} note 2
	10		100	200	ns	
	15		65	130	ns	
Output disable times $\bar{E} \rightarrow V_{os}$ HIGH	5	tPHZ	200	400	ns	} note 3
	10		115	230	ns	
	15		110	220	ns	
LOW	5	tPLZ	200	400	ns	} note 3
	10		120	245	ns	
	15		110	215	ns	
Output enable times $\bar{E} \rightarrow V_{os}$ HIGH	5	tPZH	260	525	ns	} note 3
	10		95	190	ns	
	15		65	130	ns	
LOW	5	tPZL	280	565	ns	} note 3
	10		105	205	ns	
	15		70	140	ns	

## A.C. CHARACTERISTICS

 $V_{EE} = V_{SS} = 0 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; input transition times  $\leq 20 \text{ ns}$ 

	$V_{DD}$ V	symbol	typ.	max.	
Distortion, sine-wave response	5		0,25	%	} note 4
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5		—	MHz	} note 5
	10		1	MHz	
	15		—	MHz	
Crosstalk; enable or address input to output	5		—	mV	} note 6
	10		50	mV	
	15		—	mV	
OFF-state feed-through	5		—	MHz	} note 7
	10		1	MHz	
	15		—	MHz	
ON-state frequency response	5		13	MHz	} note 8
	10		40	MHz	
	15		70	MHz	

## NOTES

 $V_{is}$  is the input voltage at a Y or Z terminal, whichever is assigned as input.

 $V_{os}$  is the output voltage at a Y or Z terminal, whichever is assigned as output.

- $R_L = 10 \text{ k}\Omega$  to  $V_{EE}$ ;  $C_L = 50 \text{ pF}$  to  $V_{EE}$ ;  $\bar{E} = V_{SS}$ ;  $V_{is} = V_{DD}$  (square-wave); see Fig. 8.
- $R_L = 10 \text{ k}\Omega$ ;  $C_L = 50 \text{ pF}$  to  $V_{EE}$ ;  $\bar{E} = V_{SS}$ ;  $S_n = V_{DD}$  (square-wave);  $V_{is} = V_{DD}$  and  $R_L$  to  $V_{EE}$  for  $t_{PLH}$ ;  $V_{is} = V_{EE}$  and  $R_L$  to  $V_{DD}$  for  $t_{PHL}$ ; see Fig. 8.
- $R_L = 10 \text{ k}\Omega$ ;  $C_L = 50 \text{ pF}$  to  $V_{EE}$ ;  $\bar{E} = V_{DD}$  (square-wave);  $V_{is} = V_{DD}$  and  $R_L$  to  $V_{EE}$  for  $t_{PHZ}$  and  $t_{PZH}$ ;  $V_{is} = V_{EE}$  and  $R_L$  to  $V_{DD}$  for  $t_{PLZ}$  and  $t_{PZL}$ ; see Fig. 8.
- $R_L = 10 \text{ k}\Omega$ ;  $C_L = 15 \text{ pF}$ ; channel ON;  $V_{is} = \frac{1}{2} V_{DD(p-p)}$  (sine-wave, symmetrical about  $\frac{1}{2} V_{DD}$ );  $f_{is} = 1 \text{ kHz}$ ; see Fig. 9.
- $R_L = 1 \text{ k}\Omega$ ;  $V_{is} = \frac{1}{2} V_{DD(p-p)}$  (sine-wave, symmetrical about  $\frac{1}{2} V_{DD}$ );  $20 \log \frac{V_{os}}{V_{is}} = -50 \text{ dB}$ ; see Fig. 10.
- $R_L = 10 \text{ k}\Omega$  to  $V_{EE}$ ;  $C_L = 15 \text{ pF}$  to  $V_{EE}$ ;  $\bar{E}$  or  $S_n = V_{DD}$  (square-wave); crosstalk is  $|V_{os}|$  (peak value); see Fig. 8.
- $R_L = 1 \text{ k}\Omega$ ;  $C_L = 5 \text{ pF}$ ; channel OFF;  $V_{is} = \frac{1}{2} V_{DD(p-p)}$  (sine-wave, symmetrical about  $\frac{1}{2} V_{DD}$ );  $20 \log \frac{V_{os}}{V_{is}} = -50 \text{ dB}$ ; see Fig. 9.
- $R_L = 1 \text{ k}\Omega$ ;  $C_L = 5 \text{ pF}$ ; channel ON;  $V_{is} = \frac{1}{2} V_{DD(p-p)}$  (sine-wave, symmetrical about  $\frac{1}{2} V_{DD}$ );  $20 \log \frac{V_{os}}{V_{is}} = -3 \text{ dB}$ ; see Fig. 9.

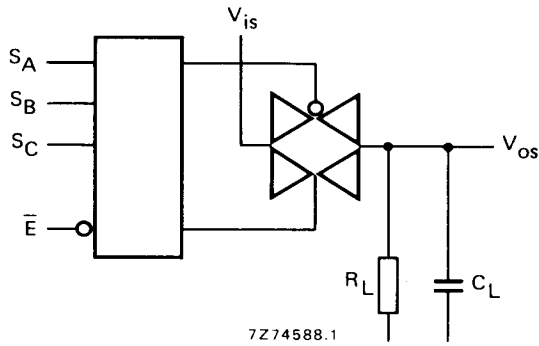


Fig. 8.

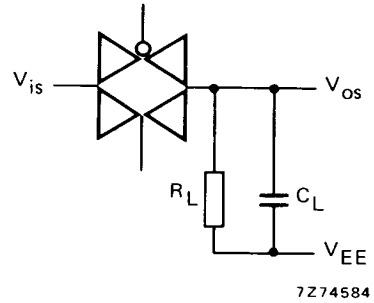


Fig. 9.

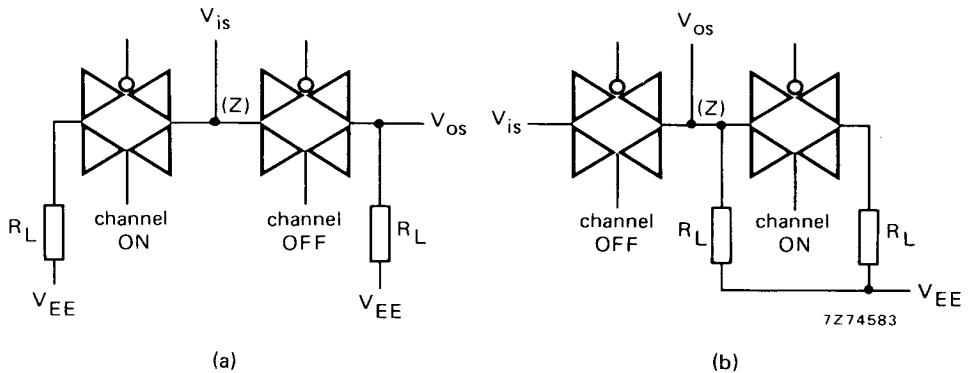


Fig. 10.

**APPLICATION INFORMATION**

Some examples of applications for the HEF4053B are:

- Analogue multiplexing and demultiplexing.
- Digital multiplexing and demultiplexing.
- Signal gating.

**NOTE**

If break before make is needed, then it is necessary to use the enable input.