HD404304 Series

Description

The HD404304 Series is a CMOS 4-bit single-chip microcomputer basically equivalent to the HMCS400 series, providing high programming productivity, high speed operation, and low power dissipation. It incorporates ROM, RAM, I/O, A/D converter, two timer/counters, including high voltage I/O pins to drive fluorescent display tubes directly.

The HD404304 Series includes three chips: the HD404302R with 2 k-word ROM, the HD404304 with 4 k-word ROM and the HD4074308 with 8 k-word PROM. The HD4074308, which includes PROM, is ZTAT™ microcomputer that can dramatically shorten system development periods and smooth the process from debugging to mass production. (The PROM program specifications are the same as for the 27256.)

Features

- 2048-word × 10-bit ROM (mask ROM version, HD404302R)
  4096-word × 10-bit ROM (HD404304)
  8192-word × 10-bit PROM (ZTAT™ version)
- 160-digit × 4-bit RAM
- 33 I/O pins, including 25 high-voltage I/O pins (40 V max.)
- Two timer/counters
  — 11-bit prescaler
  — 8-bit timer (free-running timer/watchdog timer)
  — 8-bit timer (auto-reload timer/event counter)
- Five interrupt sources
  — Two by external sources
  — Two by timer/counters
  — One by A/D converter
- 4-channel × 8-bit A/D converter
- Two tone generator outputs
- Subroutine stack, up to 16 levels including interrupts
- Two low-power dissipation modes
  — Standby mode
  — Stop mode
- On-chip oscillator
  — Crystal or ceramic oscillator
  — External clock
- Package
  — 42-pin plastic DIP (DP-42)
  — 42-pin ceramic DIP with window (DC-42)*
  — 42-pin plastic shrink DIP (DP-42S)
  — 54-pin flat plastic package (FP-54)
- Instruction cycle time: 2 µs (f_{OSC} = 4 MHz)

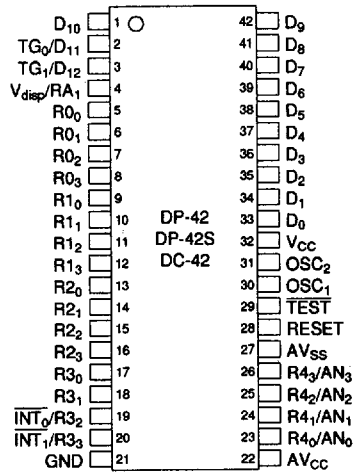
Note: * Available as a sample

Ordering Information

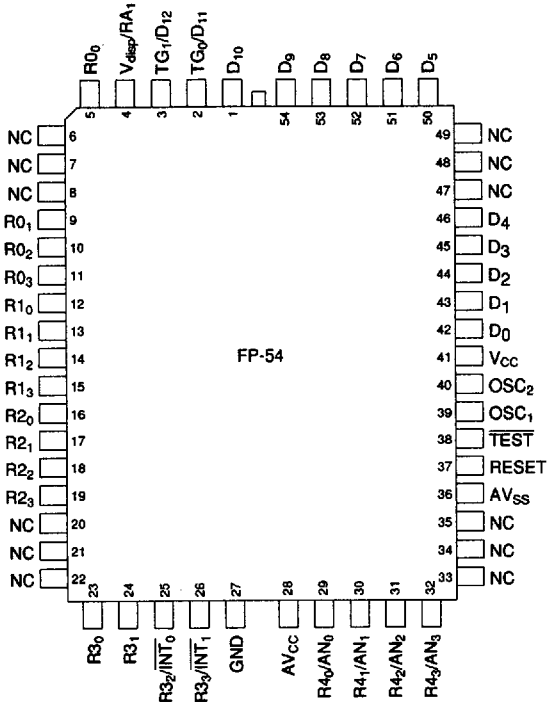
Type	Product Name	Model Name	ROM (Words)	Package
Mask ROM	HD404302R	HD404302RP	2,048	DP-42
		HD404302RS		DP-42S
		HD404302RF		FP-54
	HD404304	HD404304P	4,096	DP-42
		HD404304S		DP-42S
		HD404304F		FP-54
ZTAT™	HD4074308	HD4074308P	8,192	DP-42
		HD4074308S		DP-42S
		HD4074308C*		DC-42*
		HD4074308F		FP-54

Note: * Available as a sample

Pin Arrangement



Top view



Top view

Pin Description

Pin Number			
DP-42, DP-42S, DC-42	FP-54	Pin Name	I/O
1	1	D_{10}	I/O
2	2	D_{11}/TG_0	I/O
3	3	D_{12}/TG_1	I
4	4	RA_1/V_{disp}	I
5	5	$R0_0$	I/O
6	9	$R0_1$	I/O
7	10	$R0_2$	I/O
8	11	$R0_3$	I/O
9	12	$R1_0$	I/O
10	13	$R1_1$	I/O
11	14	$R1_2$	I/O
12	15	$R1_3$	I/O
13	16	$R2_0$	I/O
14	17	$R2_1$	I/O
15	18	$R2_2$	I/O
16	19	$R2_3$	I/O
17	23	$R3_0$	I/O
18	24	$R3_1$	I/O
19	25	$R3_2/\overline{INT_0}$	I/O
20	26	$R3_3/\overline{INT_1}$	I/O
21	27	GND	
22	28	AV_{CC}	
23	29	$R4_0/AN_0$	I/O
24	30	$R4_1/AN_1$	I/O
25	31	$R4_2/AN_2$	I/O
26	32	$R4_3/AN_3$	I/O
27	36	AV_{SS}	

NC: No connection

Pin Number			
DP-42, DP-42S, DC-42	FP-54	Pin Name	I/O
28	37	RESET	I
29	38	$\overline{TEST}$	I
30	39	OSC_1	I
31	40	OSC_2	O
32	41	V_{CC}	
33	42	D_0	I/O
34	43	D_1	I/O
35	44	D_2	I/O
36	45	D_3	I/O
37	46	D_4	I/O
38	50	D_5	I/O
39	51	D_6	I/O
40	52	D_7	I/O
41	53	D_8	I/O
42	54	D_9	I/O
—	6	NC	
—	7	NC	
—	8	NC	
—	20	NC	
—	21	NC	
—	22	NC	
—	33	NC	
—	34	NC	
—	35	NC	
—	47	NC	
—	48	NC	
—	49	NC	

Pin Functions

Power Supply

V_{CC}: Apply power supply voltage to this pin.

GND: Connect to ground.

V_{disp}: This pin, multiplexed with RA_1, is for the power supply of the high-voltage output pins with a maximum voltage of V_{CC}–40 V. For details, see the Input/Output section.

AV_{CC}, AV_{SS}: Power supply pins for the A/D converter.

$\overline{TEST}$: Non-user pin. Connect this pin to V_{CC}.

RESET: MCU reset pin. For details, see the Reset section.

Oscillators

OSC_1, OSC_2: Input/output pins for the internal oscillator circuit. They can be connected to a crystal, ceramic, or external oscillator circuit. For details, see the Internal Oscillator Circuit section.

Ports

D_0 to D_{12} (D Port): Input/output port addressed by its bits. These 13 pins are all high-voltage input/output pins. The circuit type for each pin can be selected using a mask option. For details, see the Input/Output section.

$R0_0$ to $R0_3$, $R1_0$ to $R1_3$, $R2_0$ to $R2_3$, $R3_0$ to $R3_3$, $R4_0$ to $R4_3$, RA_1 (R Ports): R0 to R4 are 4-bit I/O ports. RA is a 1-bit input-only port. The pins of R0 to R2 and RA_1 are high-voltage pins, and the pins of R3 to R4 are standard pins. $R3_2$ and $R3_3$ are multiplexed with $\overline{INT_0}$ and $\overline{INT_1}$, respectively. For details, see the Input/Output section.

Interrupts

$\overline{INT_0}$, $\overline{INT_1}$: External interrupt pins. $\overline{INT_1}$ can be used as an external event input pin for timer B. $\overline{INT_0}$ and $\overline{INT_1}$ are multiplexed with $R3_2$ and $R3_3$, respectively. For details, see the Interrupt section.

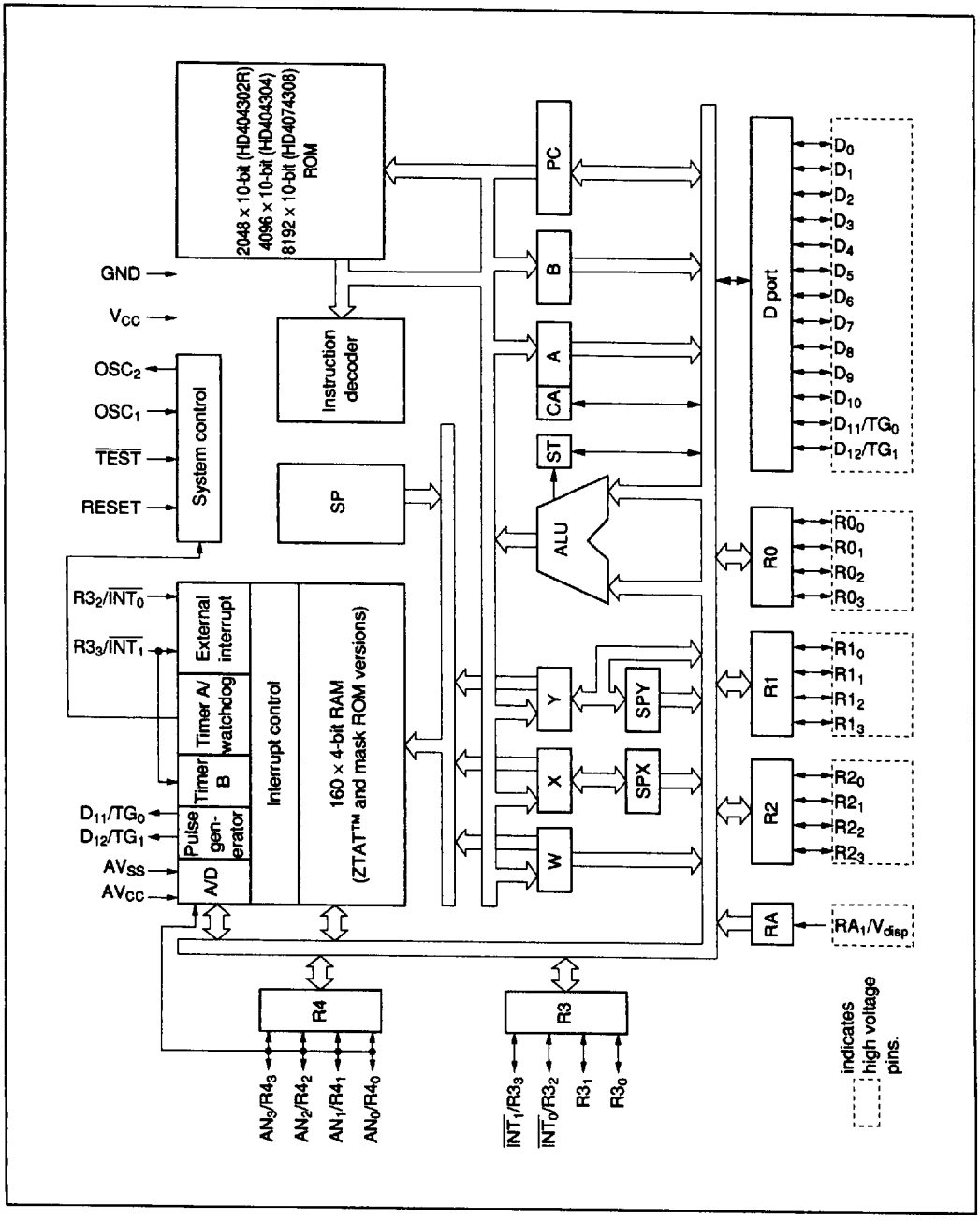
Tone Generator

TG_0, TG_1: Tone generator output pins. These pins are high-voltage pins multiplexed with D_{11} and D_{12}, respectively.

A/D Converter

AN_0 to AN_3 (AN Port): A/D converter input port. AN_0 to AN_3 are multiplexed with $R4_0$ to $R4_3$, respectively. For details, see the A/D Converter section.

Block Diagram



Memory Map

ROM Memory Map

The ROM is described in the following paragraphs with the ROM memory map in figure 1.

Vector Address Area ($0000 to $000F): Locations $0000 through $000F are reserved for JMPL instructions to branch to the starting address of the initialization program and the interrupt programs. After a reset or an interrupt, program execution continues from the vector address.

Zero-Page Subroutine Area ($0000 to $003F): Locations $0000 through $003F are reserved for subroutines. The CAL instruction branches to these subroutines.

Pattern Area ($0000 to $07FF: HD404302R; $0000 to $0FFF: HD404304, HD4074308): Locations $0000 through $07FF or $0FFF are reserved for ROM data. The P instruction allows reference to ROM data as a pattern.

Program Area ($0000 to $07FF: HD404302R; $0000 to $0FFF: HD404304; $0000 to $1FFF: HD4074308): Locations from $0000 to $1FFF can be used for program code.

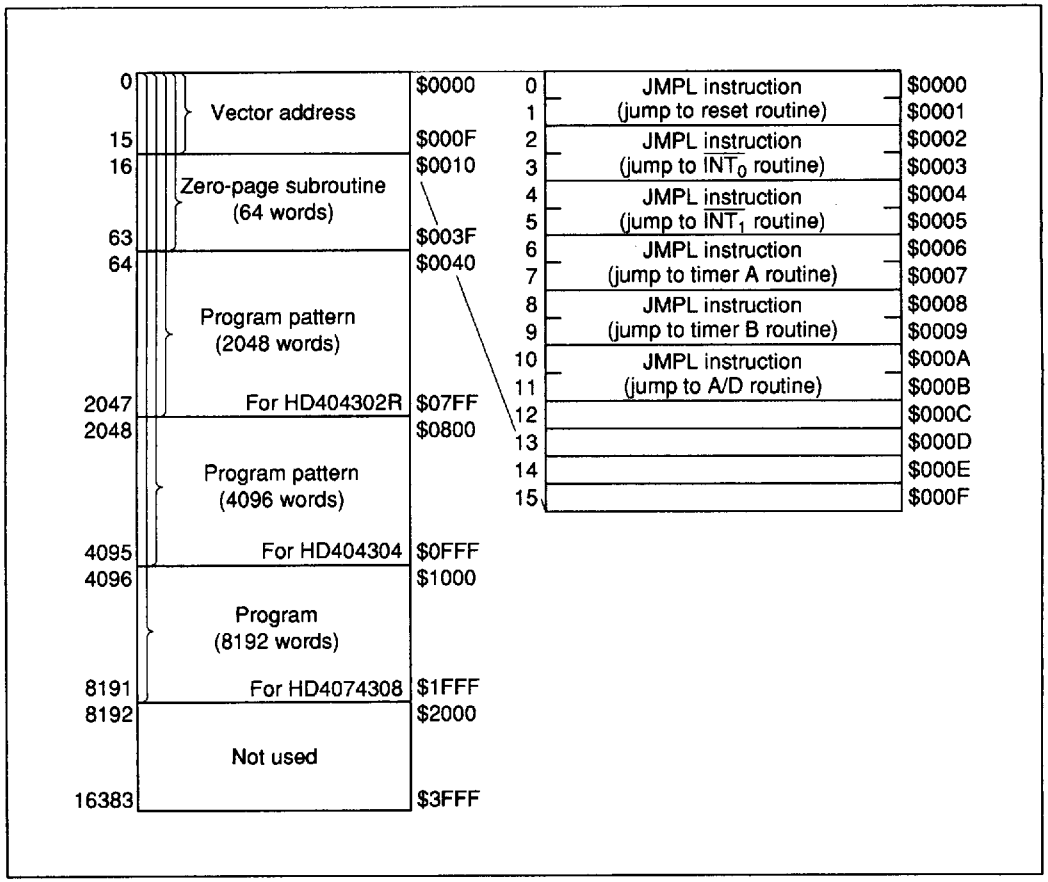


Figure 1 ROM Memory Map

RAM Memory Map

The MCU contains a 160-digit × 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. The RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bits Area ($000 to $003): The interrupt control bits area (figure 3) is used for interrupt control. It is accessible only by RAM bit manipulation instructions. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area ($004 to $034): The special function registers are the mode or data registers for external interrupt, A/D conversion, and the timer/counters, and are the I/O port data control registers. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2. These registers cannot be accessed by RAM bit manipulation instructions. However, WDON ($020) can be accessed only by those bit instructions.

Data Area ($040 to $09F): The 16 digits of $040 through $04F are called memory registers (MR) and are accessible by the LAMR and XMRA instructions (figure 4).

Stack Area ($3C0 to $3FF): Locations $3C0 through $3FF are reserved for the stack area to save the contents of the program counter (PC), status flag (ST), and carry flag (CA) when subroutine calls (CAL and CALL instructions) and interrupts are processed. This area can be used as a 16-level nesting stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by the RTN and RTNI instructions. The status and carry flags are restored only by the RTNI instruction. This area, when not used as a stack, is available as a data area.

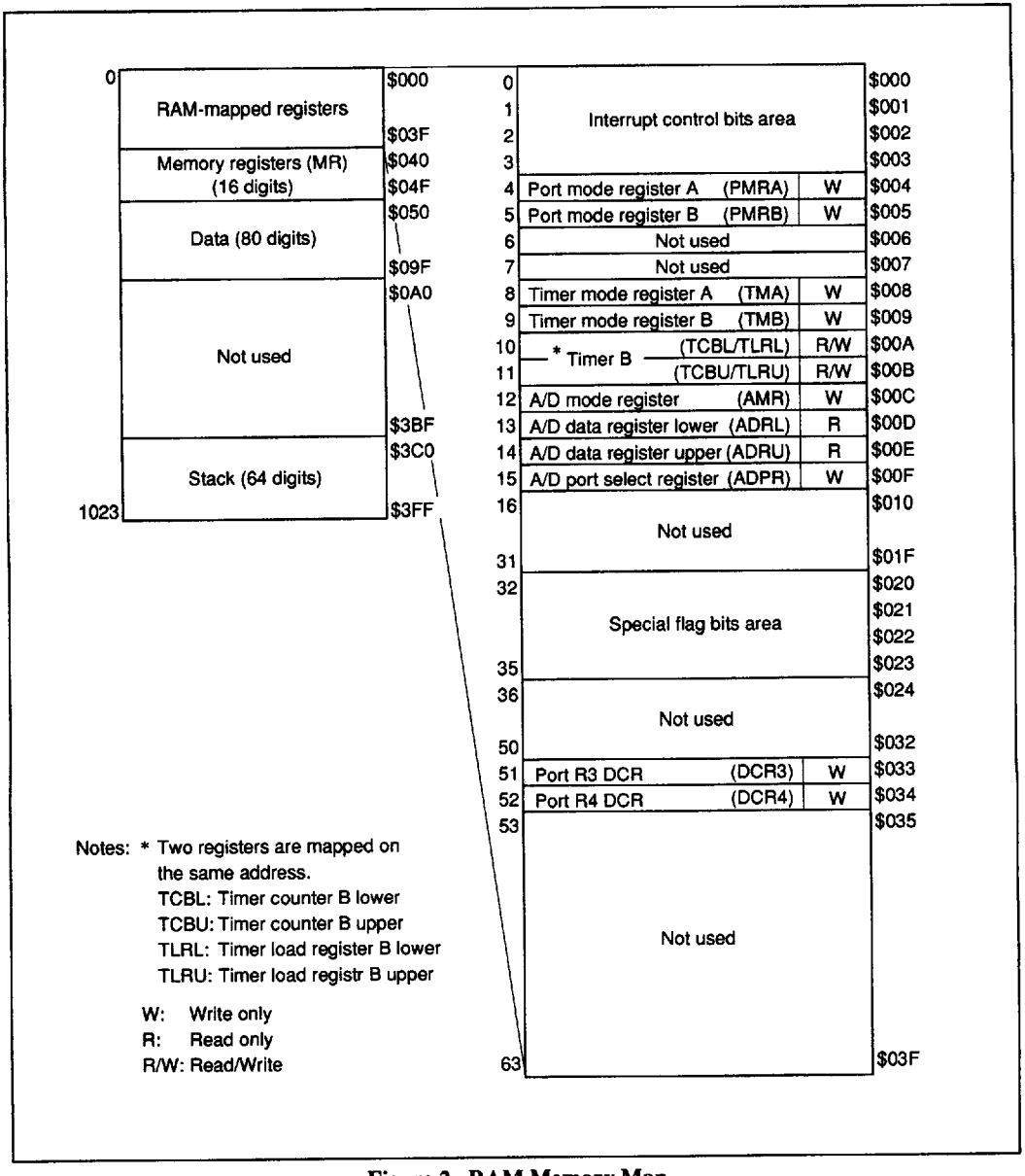


Figure 2 RAM Memory Map

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP bit)	IE (Interrupt enable flag)	$000
1	IMTA (IM of timer A)	IFTA (IF of timer A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	IMAD (IM of A/D)	IFAD (IF of A/D)	IMTB (IM of timer B)	IFTB (IF of timer B)	$002
3	Not used	Not used	Not used	Not used	$003

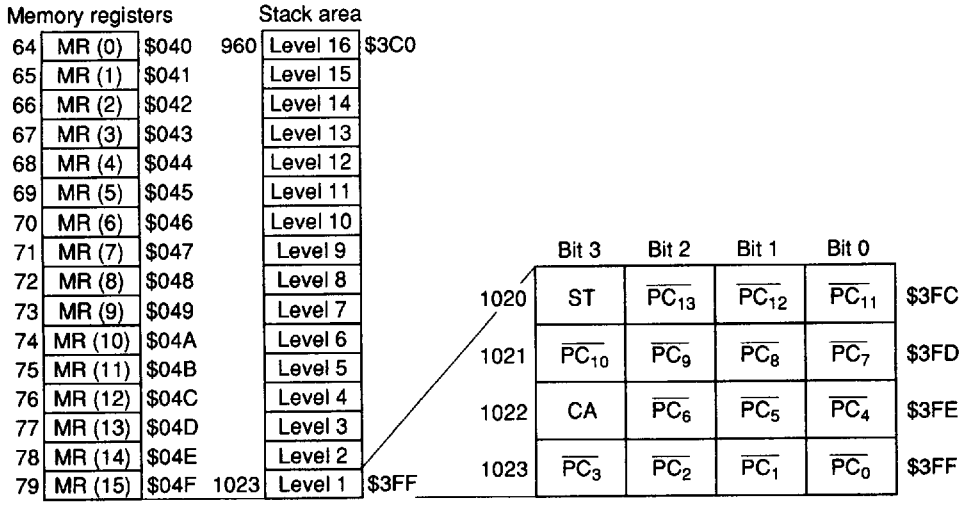
IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer

Note: Each bit in the interrupt control bits area is set by the SEM/SEMD instruction, reset by the REM/REMD instruction, and tested by the TM/TMD instruction. Other instructions have no effect. Furthermore, the interrupt request flag is not affected by the SEM/SEMD instruction. The contents of the status flag become invalid when unusable bits and the RSP bit are tested by the TM or TMD instruction.

	Bit 3	Bit 2	Bit 1	Bit 0	
32	Not used	Not used	WDON (Watchdog on flag)	ADSF (A/D start flag)	$020
	Reserved				$021
					$022
					$023

Note: The WDON flag can be used by the SEM/SEMD instruction, and reset by MCU reset. ADSF stays high during A/D conversion and becomes low after A/D conversion.

Figure 3 Configuration of Interrupt Control Bits Area



PC_{13} to PC_0: Program counter
ST: Status flag
CA: Carry flag

Notes: 1. Since the HD404302R has a 2-kword ROM, $\overline{PC_{11}}$, $\overline{PC_{12}}$, and $\overline{PC_{13}}$ are not used.
2. Since the HD404304 has a 4-kword ROM, $\overline{PC_{12}}$ and $\overline{PC_{13}}$ are not used.
3. Since the HD4074308 has a 8-kword ROM, $\overline{PC_{13}}$ is not used.

Figure 4 Configuration of Memory Registers, Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has nine registers and two flags for CPU operations. The following paragraphs describe the registers and flags shown in figure 5 in detail.

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results from the arithmetic logic unit (ALU) as well as the transfer data between memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The 2-bit W register and the 4-bit X and Y registers indirectly address the RAM. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): The 4-bit SPX and SPY registers are used to assist the X and Y registers, respectively.

Carry Flag (CA): The carry flag (CA) indicates an overflow generated from the ALU during arithmetic operation. It is also affected by the SEC, REC, ROTL, and ROTR instructions. A carry is pushed onto the stack during an interrupt, and popped off the stack by the RTNI instruction. This flag is not affected by the RTN instruction.

Status Flag (ST): The status flag (ST) indicates an ALU overflow and ALU non-zero during arithmetic or compare instructions, and the result of a bit test instruction. Moreover, the status flag controls branching caused by the BR, BRL, CAL, or CALL instruction. Whether these instructions are executed or skipped, the status flag is always set to 1. The state of this flag remains unchanged until the next arithmetic, compare, bit test, or branch instruction is executed. During an interrupt, ST is pushed onto the stack, and popped off the stack by the RTNI instruction. This flag is not affected by the RTN instruction.

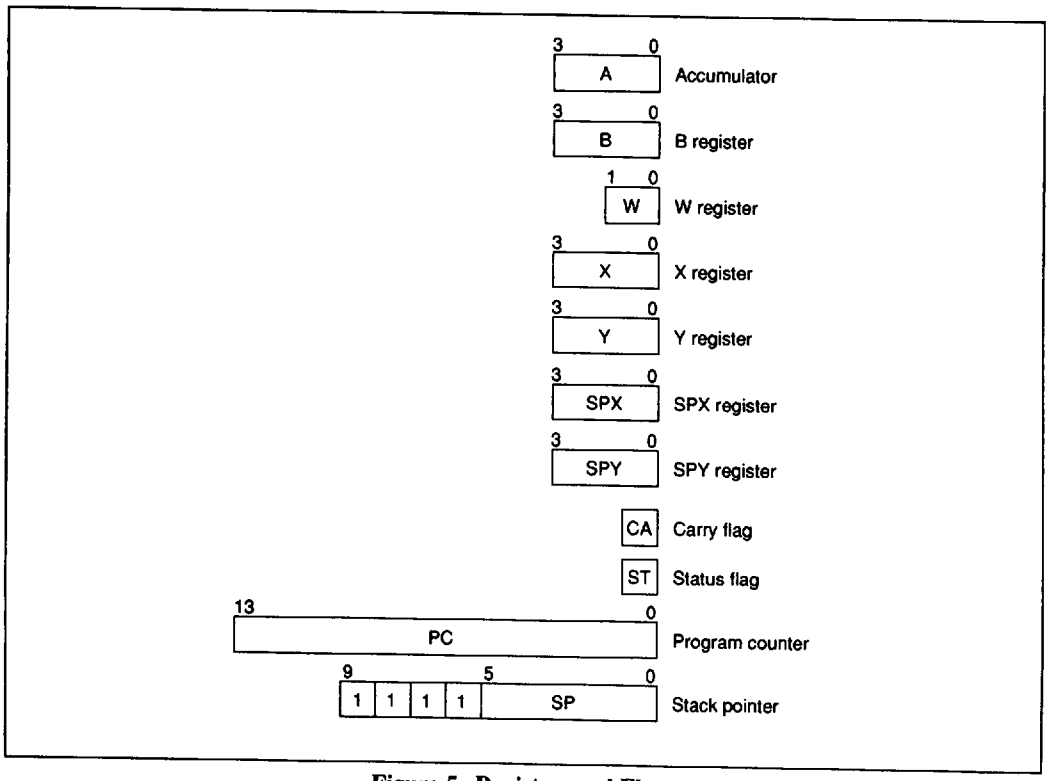


Figure 5 Registers and Flags

Program Counter (PC): The program counter is a 14-bit binary counter which holds the address of the next program instruction to be executed.

Stack Pointer (SP): The stack pointer (SP) is a 10-bit register which indicates the next stack address. This pointer, which is initialized to $3FF, is decremented by 4 when data is pushed onto the stack, and is incremented by 4 when data is popped off the stack. The highest four bits are fixed to 1111, which allows the pointer to indicate up to 16 levels of subroutines. The stack pointer is initialized when the MCU is reset or the RSP bit ($000, bit 1) is reset by the REM or REMD instruction.

Interrupts

Five interrupt sources are available on the MCU: external requests ($\overline{INT_0}$, $\overline{INT_1}$), timer/counters (timer A, timer B), and A/D. For each source, the interrupt request flag (IF), interrupt mask (IM), and interrupt vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (IE) is also used to control interrupt operations.

Interrupt Control Bits and Interrupt Service: The interrupt control bits are mapped on $000 through $003 of the RAM space. They are accessible by RAM bit manipulation instructions. However, the interrupt request flag (IF) cannot be set by software. The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 after MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source. The interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Table 1 Vector Addresses and Interrupt Priority

Reset/Interrupt	Priority	Vector Addresses
RESET	—	$0000
$\overline{INT_0}$	1	$0002
$\overline{INT_1}$	2	$0004
Timer A	3	$0006
Timer B	4	$0008
A/D	5	$000A

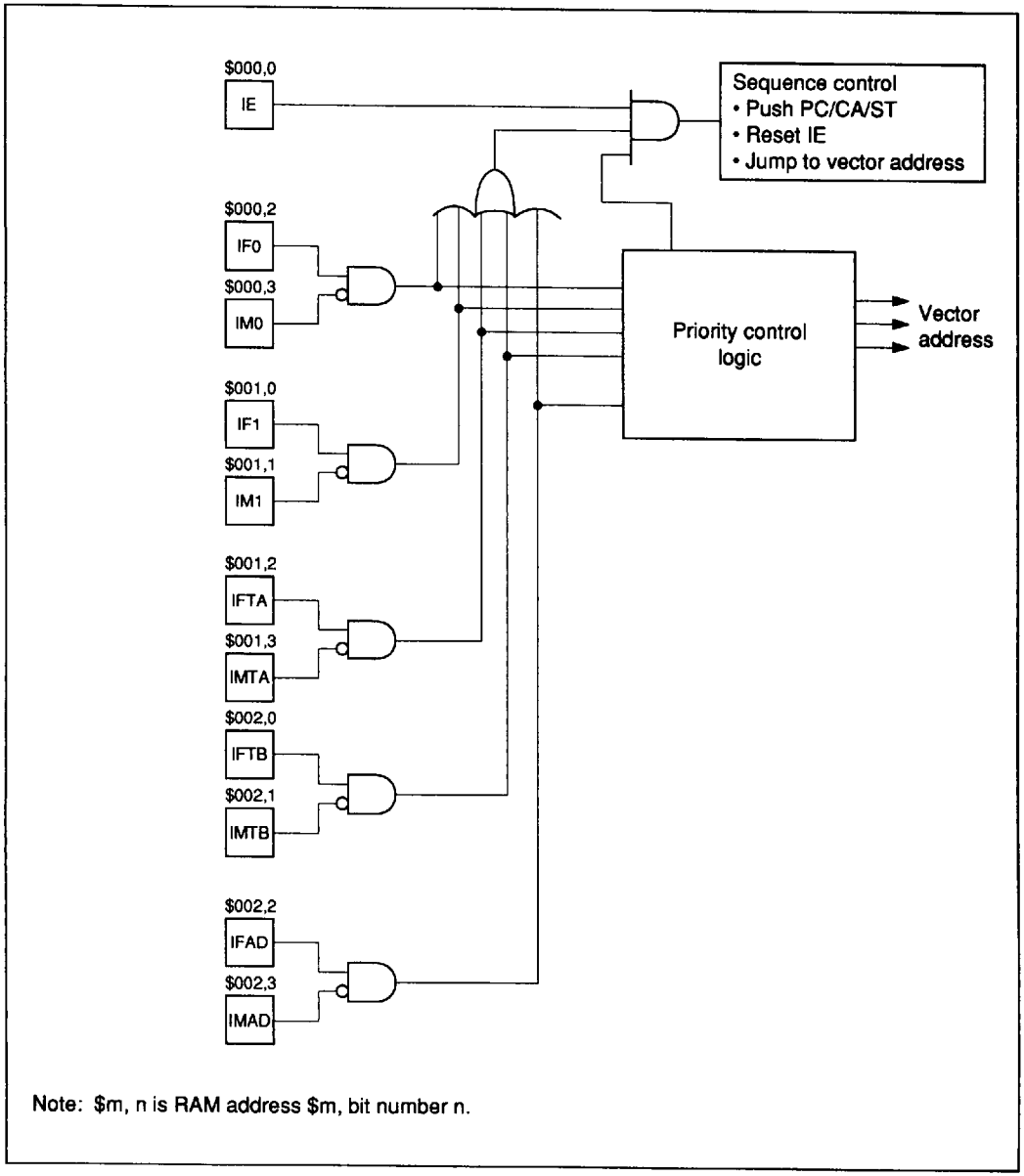
Table 2 Interrupt Conditions

Interrupt Control Bit	$\overline{INT_0}$	$\overline{INT_1}$	Timer A	Timer B	A/D
IE	1	1	1	1	1
IF0 · $\overline{IM0}$	1	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0
IFTA · $\overline{IMTA}$	*	*	1	0	0
IFTB · $\overline{IMTB}$	*	*	*	1	0
IFAD · $\overline{IMAD}$	*	*	*	*	1

Note: * Don't care

Figure 7 shows the interrupt processing sequence, and figure 8 shows the interrupt processing flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry flag, status flag, and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed, after jumping to the vector address.

At each vector address, program the JMPL instruction to branch to the starting address of the interrupt program. The IF which caused the interrupt must be reset by software in the interrupt program.



Note: $m, n is RAM address $m, bit number n.

Figure 6 Interrupt Control Circuit Block Diagram

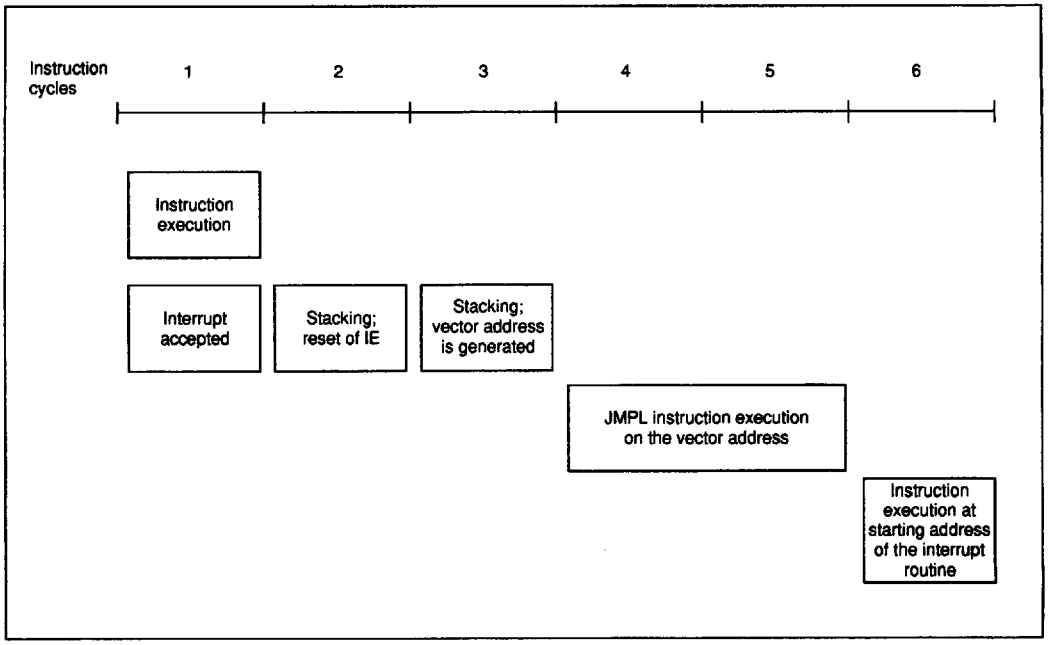


Figure 7 Interrupt Processing Sequence

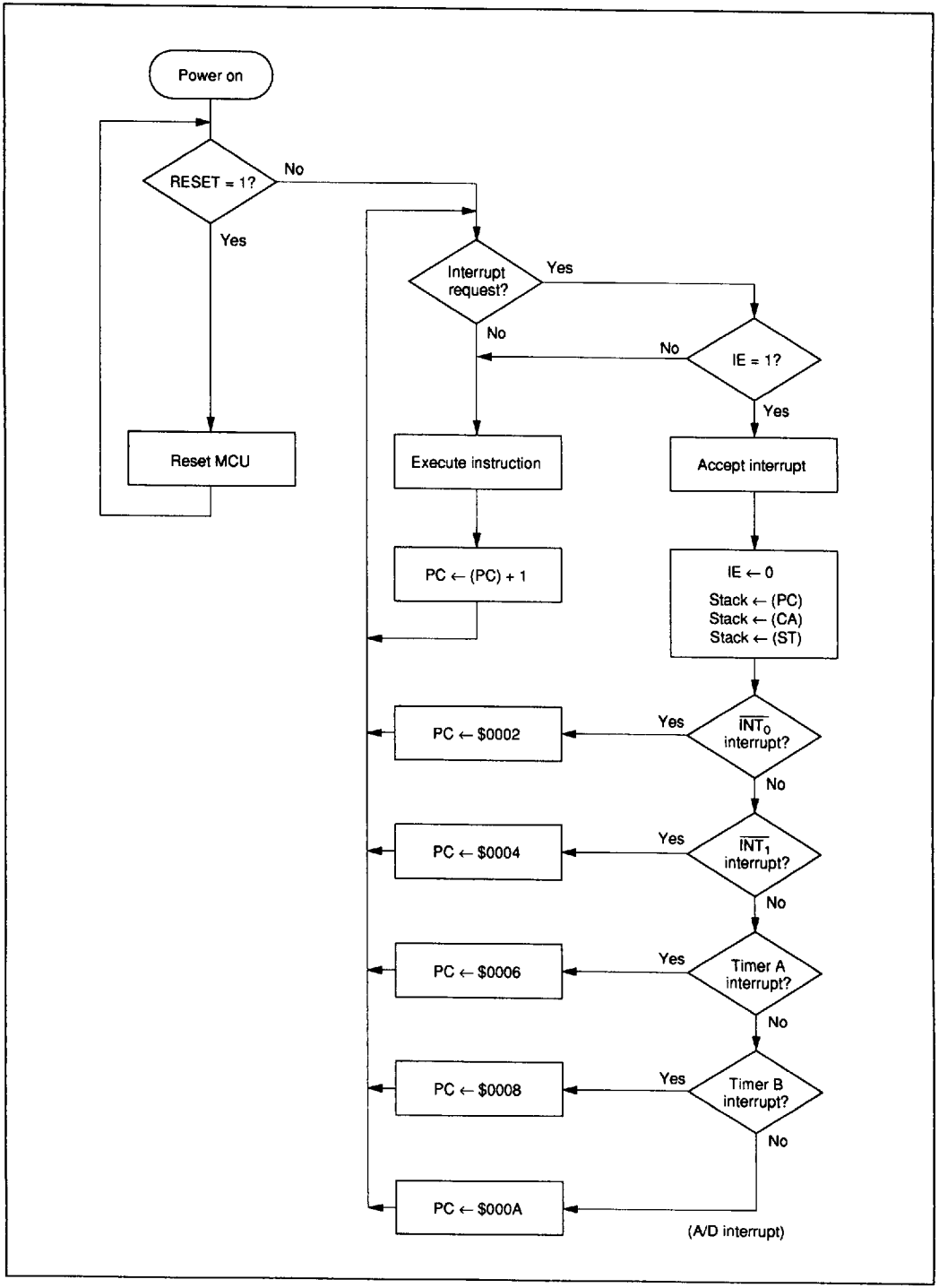


Figure 8 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): The interrupt enable flag enables/disables interrupt requests. It is reset by an interrupt and set by the RTNI instruction.

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$): The external interrupt request inputs ($\overline{INT_0}$, $\overline{INT_1}$) can be selected by port mode register A (PMRA: $004) (figure 10).

The external interrupt request flags (IF0, IF1) are set at the falling edge of $\overline{INT_0}$ and $\overline{INT_1}$ inputs, respectively.

The $\overline{INT_1}$ input can be used as a clock signal input to time B. Timer B is incremented at each falling edge of the $\overline{INT_1}$. When using $\overline{INT_1}$ as the timer B external event input, the external interrupt mask (IM1) must be set so that the interrupt request by $\overline{INT_1}$ will not be accepted. Figure 9 shows the interrupt mode register.

External Interrupt Request Flags (IF0: $000, Bit 2; IF1: $001, Bit 0): The external interrupt request flags (IF0, IF1) (figure 9) are set at the falling edge of the $\overline{INT_0}$ and $\overline{INT_1}$ inputs, respectively.

External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1): The external interrupt mask bits (figure 9) mask an interrupt request caused by the external interrupt request flags.

Port Mode Register A (PMRA: $004): Port mode register A is a 4-bit write-only register which controls the $R3_2/\overline{INT_0}$ pin and $R3_3/\overline{INT_1}$ pin as shown in figure 10. Port mode register A will be initialized to $0 by MCU reset.

Timer A Interrupt Request Flag (IFTA: $001, Bit 2): The timer A interrupt request flag (figure 9) is set when an overflow occurs in timer A.

Timer A Interrupt Mask (IMTA: 001, Bit 3): The timer A interrupt mask bit (figure 9) masks an interrupt request caused by the timer A interrupt request flag.

Timer B Interrupt Request Flag (IFTB: $002, Bit 0): The timer B interrupt request flag (figure 9) is set when an overflow occurs in timer B.

Timer B Interrupt Mask (IMTB: $002, Bit 1): The timer B interrupt mask bit (figure 9) masks an interrupt request caused by the timer B interrupt request flag.

A/D Interrupt Request Flag (IFAD: $002, Bit 2): The A/D interrupt request flag (figure 9) is set when an A/D conversion is completed.

A/D Interrupt Mask (IMAD: $002, Bit 3): The A/D interrupt mask bit (figure 9) masks an interrupt request caused by the A/D interrupt request flag.

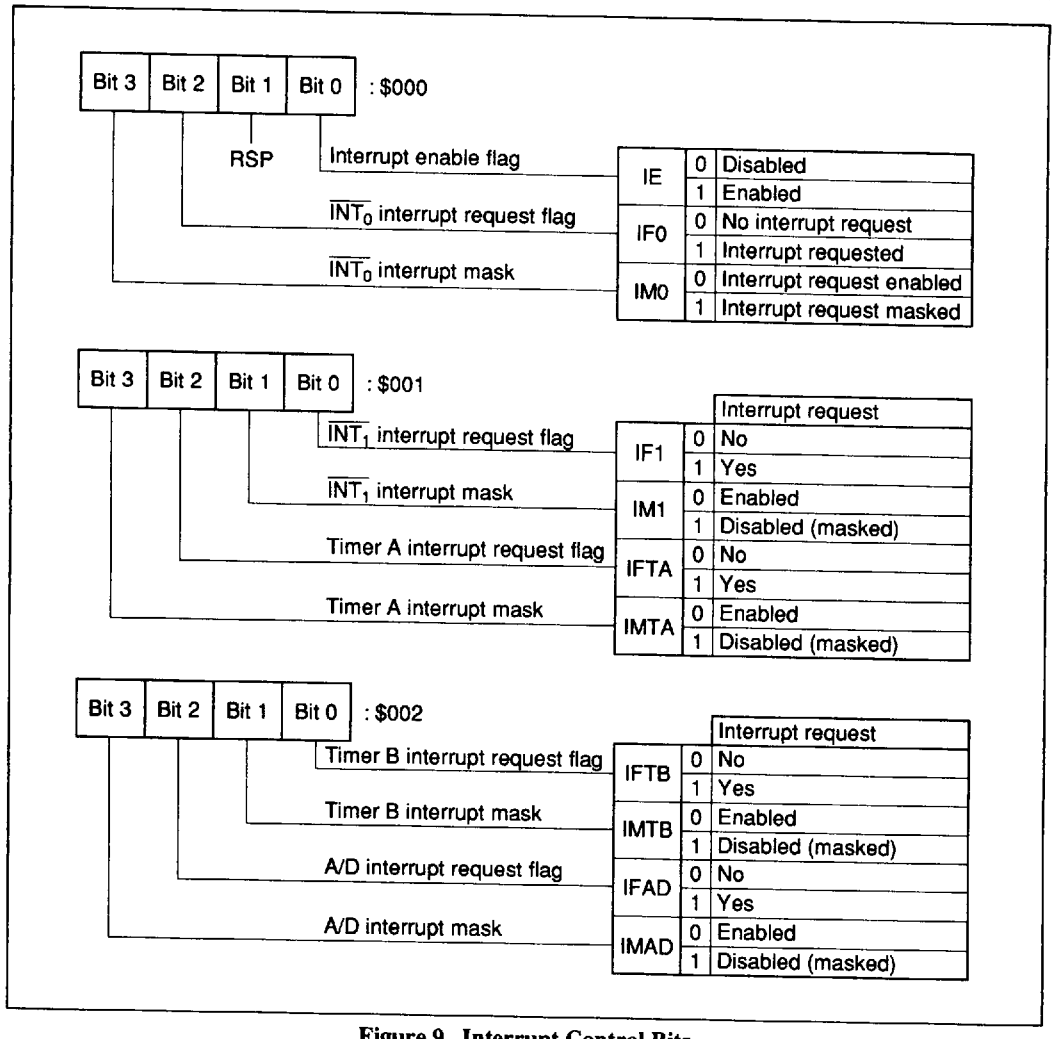


Figure 9 Interrupt Control Bits

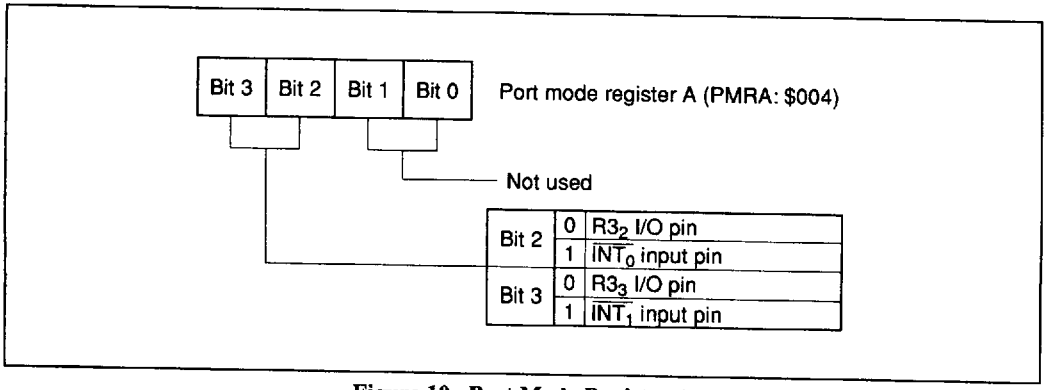


Figure 10 Port Mode Register A

Timers

The MCU contains a prescaler and two timer/counters (timers A and B) as shown by the block diagram in figure 11.

Prescaler: The input to the prescaler is the system clock signal. The prescaler is initialized to $000 by MCU reset or by setting bit 3 of timer mode register A (TMA: $008) when the watchdog timer on flag (WDON: $020, bit 1) is 0, after which the prescaler starts to divide the system clock. It continues operation until MCU reset or stop mode occurs.

The pulse frequency of timer A input clock, timer B input clock, and the tone generator outputs (TG_0, TG_1) are selected among prescaler outputs by timer mode register A (TMA: $008), timer mode register B (TMB: $009), and port mode register B (PMRB: $005), respectively.

After MCU reset, WDON is 0. Thus, when timer A is reset by setting bit 3 of timer mode register A (TMA) when the watchdog timer is off, the prescaler is also reset, which affects the operation of timer B and the tone generator outputs (TG_0, TG_1). Consequently, the program should control these conditions.

Timer A Operation: Timer A is an 8-bit interval timer which can be used also as a watchdog timer. The prescaler divide ratio of timer A is selected by timer mode register A (TMA: $008).

After timer A is initialized to $00 by MCU reset or setting bit 3 of timer mode register A (TMA: $008), it is incremented at every clock input signal. Eight different clock signals, divided by the prescaler, can be used as an input clock. The clock input signals to timer A are selected by timer mode register A. When the next clock signal is applied after timer A becomes $FF, an overflow is generated and timer A is reset to $00. This overflow causes the timer A interrupt request flag (IFTA $001, bit 2) to go to 1.

This timer can function as a watchdog timer to detect a runaway program. The MCU is reset when an overflow output is generated from a timer counter that cannot be controlled due to a runaway program while the watchdog timer on flag (WDON) is 1.

Timer B Operation: Timer mode register B (TMB: $009) selects the auto-reload function input clock source, and the prescaler divide ratio for timer B. When an external event input is used as an input clock signal to timer B, select $R3_3/\overline{INT_1}$ as $\overline{INT_1}$ by setting port mode register A (PMRA: $004), and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

Timer B is initialized according to data written into timer load register B by software. Timer B is incremented at every clock input signal. When the next clock signal is applied to timer B after it is set to $FF, it will generate an overflow output. In this case, if the auto-reload function is selected, timer B is initialized according to the value of timer load register B. If it is not selected, timer B is reset to $00. The timer B interrupt request flag (IFTB: $002, bit 0) will be set at this overflow output.

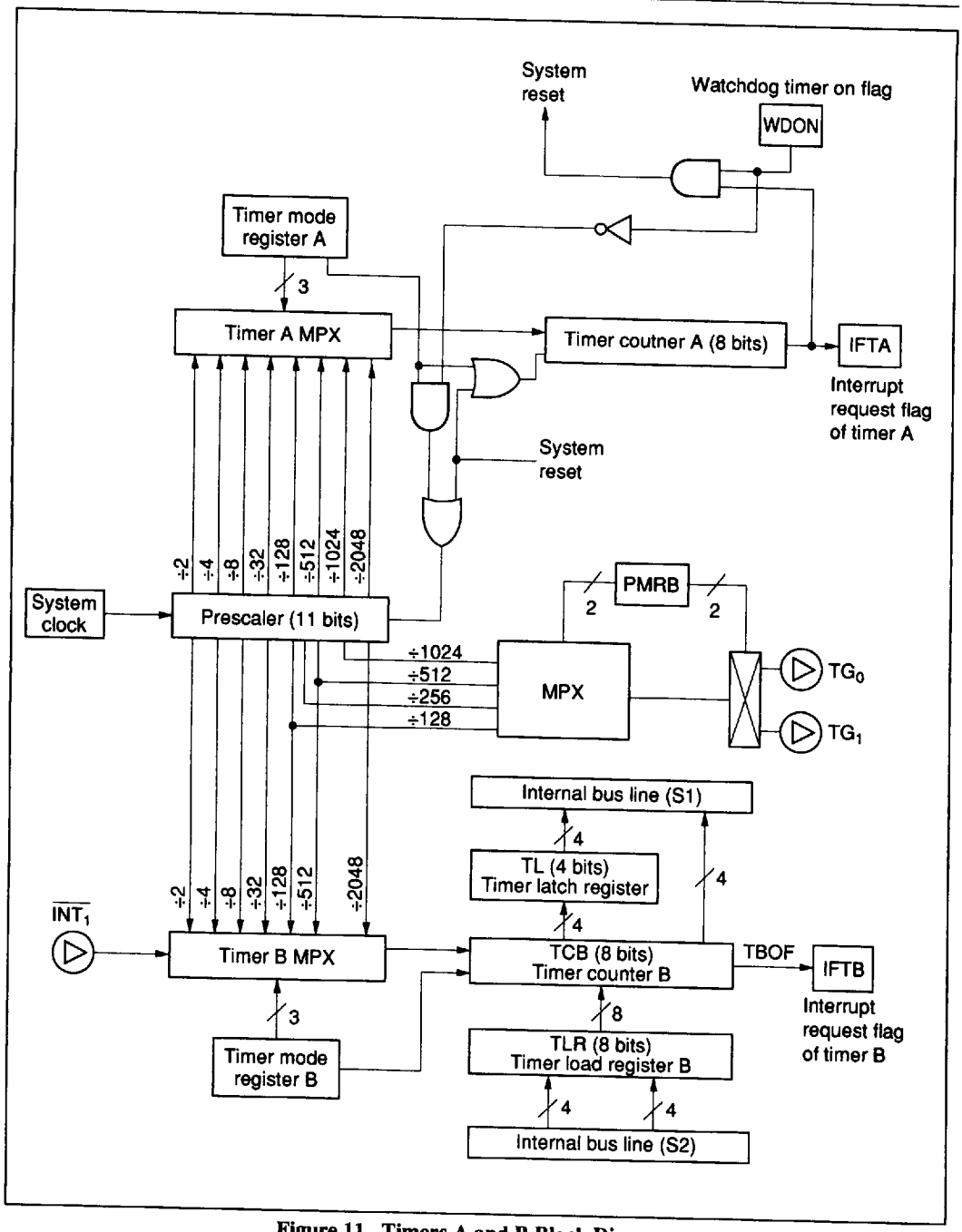


Figure 11 Timers A and B Block Diagram

Timer Mode Register A (TMA: $008): Timer mode register A is a 4-bit write-only register. Bits 0 to 2 of TMA control the prescaler divide ratio of the timer counter A clock input, as shown in figure 12. Bit 3 resets timer A when set to 1; if WDON = 0, the prescaler is also reset. Bit 3 retains a 1 for only one instruction cycle.

Timer mode register A can be modified from the second instruction cycle of the write instruction.

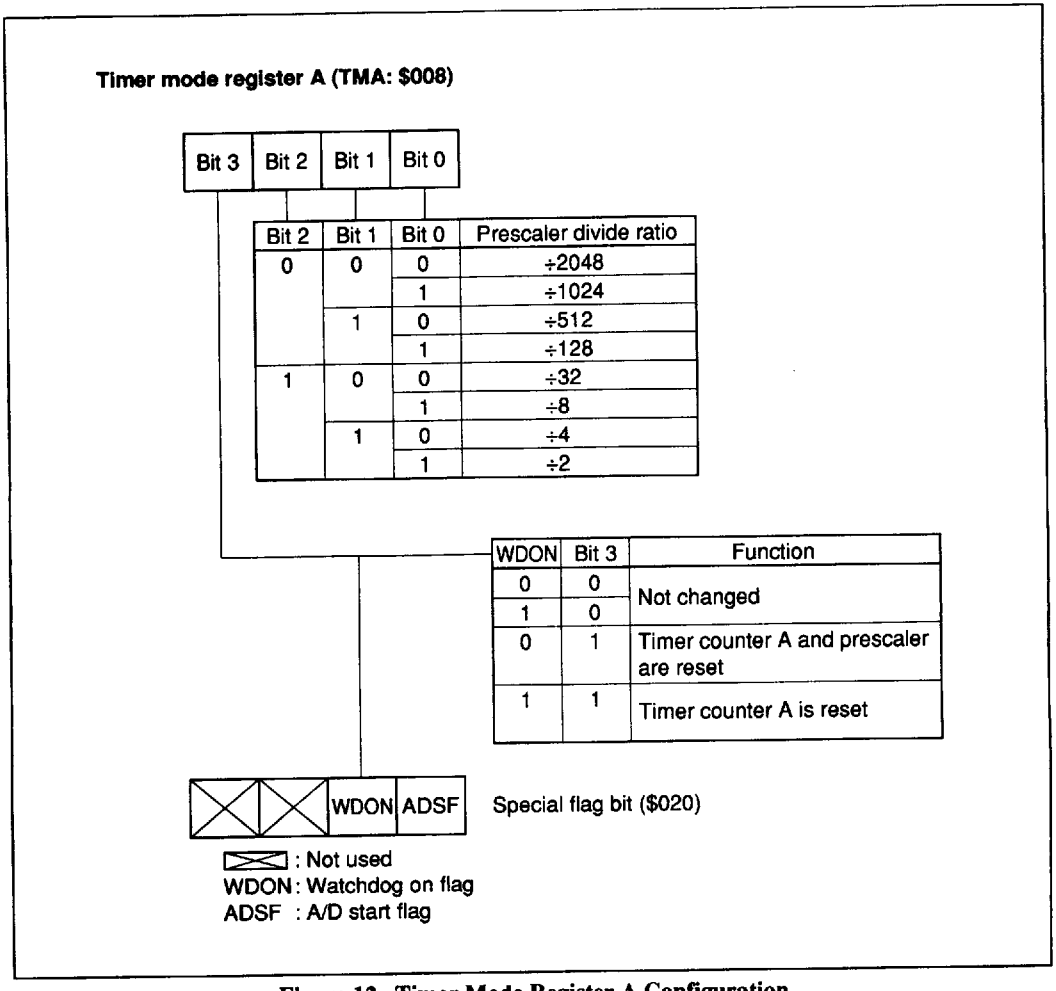


Figure 12 Timer Mode Register A Configuration

Timer Mode Register B (TMB: $009): Timer mode register B is a 4-bit write-only register which selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in figure 13. Timer mode register B is initialized to $0 by MCU reset.

The operation mode of timer B can be modified from the second instruction cycle after timer mode register B is written to. The initialization of timer B by a write to the timer load register should be performed after the contents of timer mode register B have been appropriately changed.

Timer B (TCBL: $00A, TCBU: $00B, TLRL: $00A, TLRU: $00B): Timer B consists of an 8-bit write-only timer load register, and an 8-bit read-only timer counter. Each of them has a low-order digit (TCBL: $00A, TLRL: $00A) and a high-order digit (TCBU: $00B, TLRU: $00B).

Timer counter B can be initialized by writing data into timer load register B. In this case, write the low-order digit first, and then the high-order digit. The timer counter is initialized when the high-order digit is written. The timer load register is initialized to $00 by MCU reset.

The counter value of timer B can be obtained by reading time counter B. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched when the high-order digit is read.

Timer mode register B (TMB: $009)

Bit 3	Bit 2	Bit 1	Bit 0

Bit 2	Bit 1	Bit 0	Prescaler divide ratio input clock source
0	0	0	÷2048
		1	÷512
	1	0	÷128
		1	÷32
1	0	0	÷8
		1	÷4
	1	0	÷2
		1	$\overline{INT_1}$ (external event input)

Bit 3		
	0	No auto-reload function
	1	Auto-reload function provided

Figure 13 Timer Mode Register B Configuration

Timer A Interrupt Request Flag (IFTA: $001, Bit 2): The timer A interrupt request flag (figure 14) is set by the overflow output of timer A. When the watchdog timer function is selected, the timer interrupt request flag is not set since the MCU is reset by an overflow output.

Timer A Interrupt Mask (IMTA: $001, Bit 3): The timer A interrupt mask (figure 14) prevents an interrupt request from being generated by the timer A interrupt request flag.

Timer B Interrupt Request Flag (IFTB: $002, Bit 0): The timer B interrupt request flag (figure 14) is set by the overflow output of timer B.

Timer B Interrupt Mask (IMTB: $002, Bit 1): The timer B interrupt mask (figure 14) prevents an interrupt request from being generated by the timer B interrupt request flag.

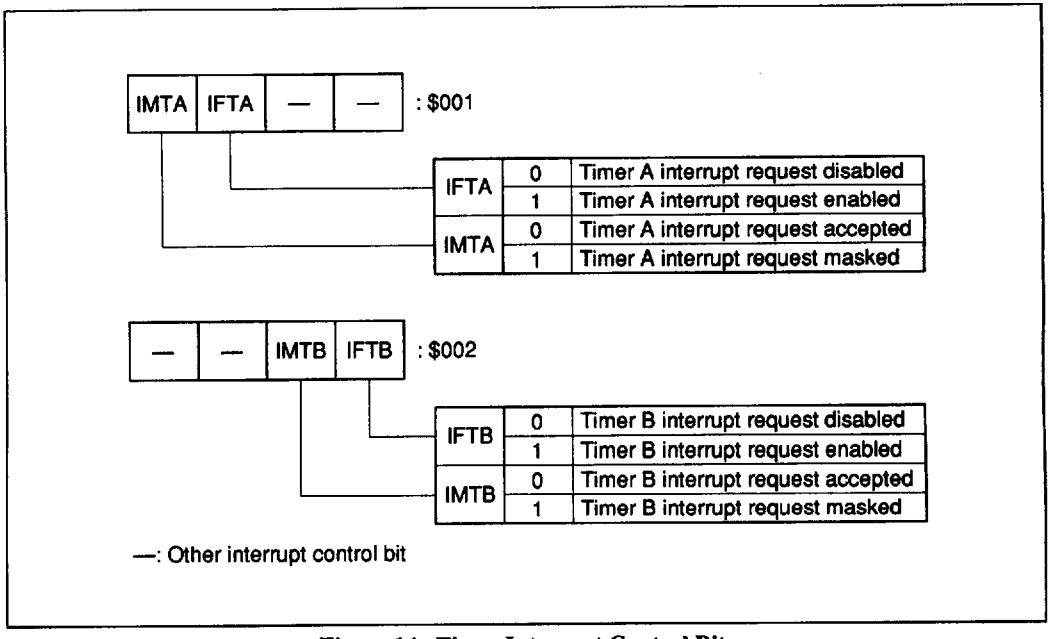


Figure 14 Timer Interrupt Control Bits

A/D Converter

The HD404302R, HD404304, and HD4074308 incorporate a sequential comparison system A/D converter consisting of a resistor ladder. It can measure four analog inputs with 8-bit resolution. Figure 15 shows the A/D converter block diagram. The A/D converter consists of the following registers:

- A/D mode register (4 bits)
- A/D start flag (1 bit)
- A/D port select register (4 bits)
- A/D data register (4 bits + 4 bits)

A/D Mode Register (AMR: $00C): The A/D mode register (figure 16) is a 4-bit write-only register which selects the A/D conversion speed (bit 0, bit 1) and analog input channel (bit 2, bit 3).

A/D Start Flag (ADSF: $020, Bit 0): A/D conversion is started when a 1 is written to the A/D start flag (figure 16). After a conversion is completed, the conversion data is set in the A/D data register and the A/D start flag is cleared simultaneously. Note that the bit manipulation instruction SEM or SEMD should be used to write data to ADSF. During A/D conversion, ADSF must not be written to.

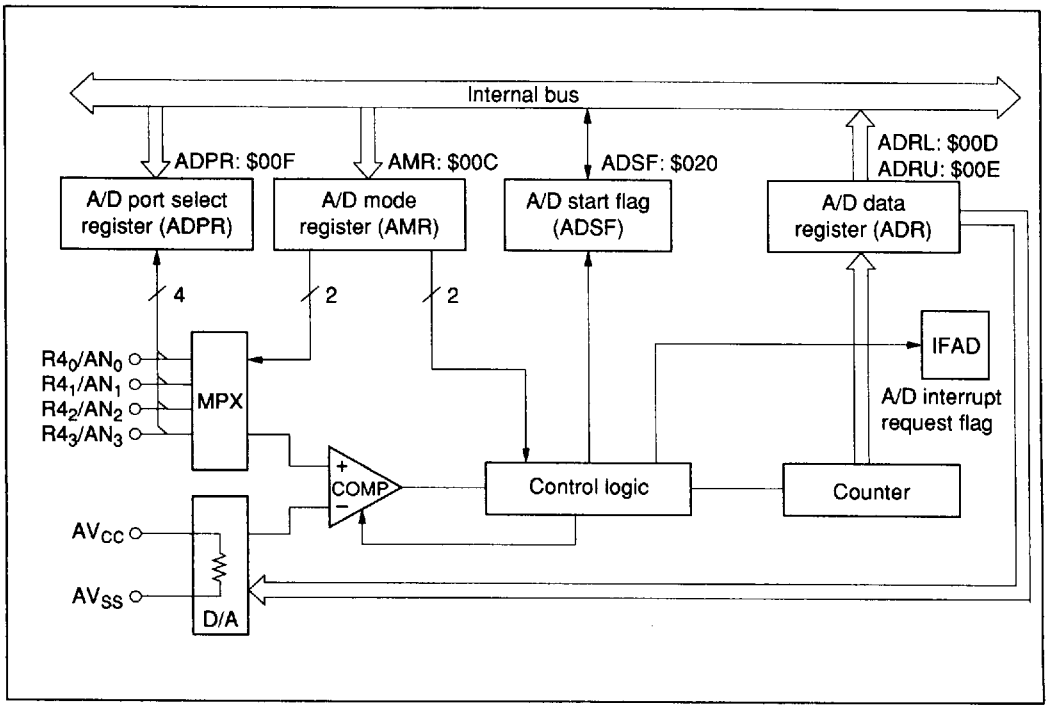


Figure 15 A/D Converter Block Diagram

A/D Port Select Register (ADPR: $00F): The A/D port select register (figure 16) is a write-only register which selects the digital port and analog port.

A/D mode register (AMR: $00C)

Bit 3	Bit 2	Bit 1	Bit 0

Bit 1	Bit 0	Conversion cycle
0	0	34
	1	67

Bit 3	Bit 2	Analog input
0	0	AN_0
	1	AN_1
1	0	AN_2
	1	AN_3

Special flag bit ($020)

Bit 3	Bit 2	Bit 1	Bit 0

A/D start flag (ADSF)		
ADSF	Start bit (write)	Status information (test)
0	Not affect	A/D idle
1	Start	A/D converting

WDON (see Timer section)

Not used

A/D port select register (ADPR: $00F)

Bit 3	Bit 2	Bit 1	Bit 0

Port select				
1	AN_3	AN_2	AN_1	AN_0
0	$R4_3$	$R4_2$	$R4_1$	$R4_0$

Figure 16 A/D Register Configuration

A/D Data Register (ADRL: $00D, ADRU: $00E): The A/D data register (figure 17) is a 4-bit/4-bit read-only register in which the 8-bit conversion result is set after completing A/D conversion. The data is preserved until the next conversion begins. Data read is not guaranteed during A/D conversion. The A/D data register is initialized to $80 by the MCU reset.

Precautions on Using the A/D Converter:

- If a digital signal is input to the $R4_0$ to $R4_3$ or adjacent pins during A/D conversion, conversion accuracy may be affected.
- Data in the A/D data register is not guaranteed during A/D conversion.
- Port output instructions should not be executed during A/D conversion to allow for a stable A/D converter operation.

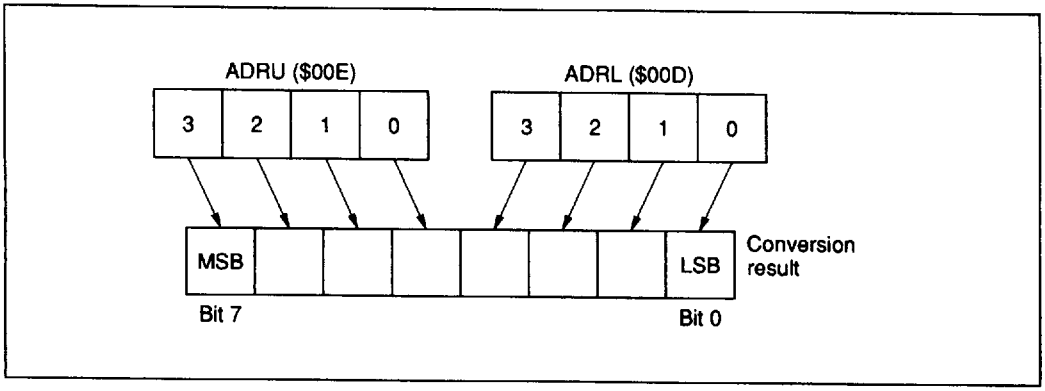


Figure 17 A/D Data Register Configuration

Input/Output

The MCU has 33 I/O pins, 25 being high-voltage pins. The on/off status of the output buffers of the standard pins (figure 19) is controlled by the combinations of the value of the port register (PDR) and data control register (DCR).

D Port: The D port is an I/O port which has 13 discrete I/O pins, each of which can be addressed independently. It can be set/reset through the SED/RED and SEDD/REDD instructions, and can be tested through the TD and TDD instructions. Furthermore, the contents of the status flag become invalid when the unused ports are tested. D_{11} and D_{12} ports are multiplexed with tone generator pins TG_0 and TG_1, respectively. The circuit type of the D port is shown in table 3.

R Ports: The R ports are composed of 20 I/O pins and one input-only pin. Data is input through the LAR and LBR instructions and output through the LRA and LRB instructions. The MCU will not be affected by writing into the input-only and nonexisting ports. The on/off status of the output buffers of the R3 and R4 ports are controlled by the R port data control register (DCR3, DCR4). $R3_2$ and $R3_3$ are multiplexed with $\overline{INT_0}$ and $\overline{INT_1}$, respectively. $R4_0$, $R4_1$, $R4_2$, and $R4_3$ pins are multiplexed with AN_0, AN_1, AN_2, and AN_3, respectively. The circuit type of the R port is shown in table 3.

Port Mode Register B (PMRB: $005): Port mode register B is a 4-bit write-only register which controls the D_{11}/TG_0 pin and D_{12}/TG_1 pin as shown in figure 18. The port mode register is initialized to $0 by MCU reset. These pins are therefore initially used a ports.

Unused I/O Pins: If any unused I/O pins are left floating, the LSI may malfunction due to noise. The I/O pins should be fixed as follows to prevent malfunction.

- If without pull-down MOS (PMOS open drain) is selected for high-voltage pins connect to V_{CC} on the printed circuit board.
- If without pull-up MOS is selected for standard pins, connect to GND on the printed circuit board.

The contents of PDR and DCR of the corresponding pin should be programmed to remain the same as in the reset state. The corresponding pin should not be used as a peripheral function I/O pin.

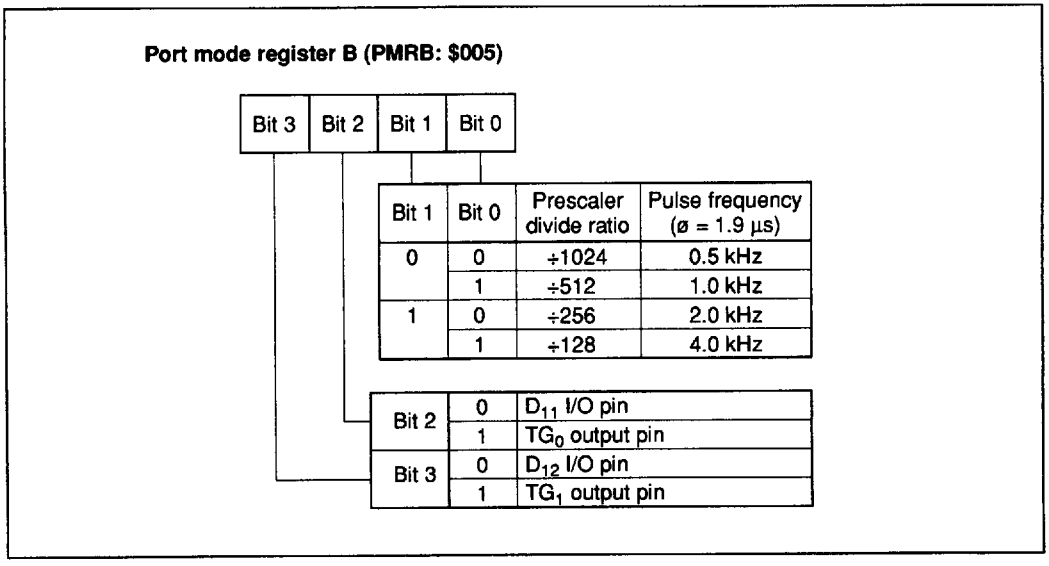
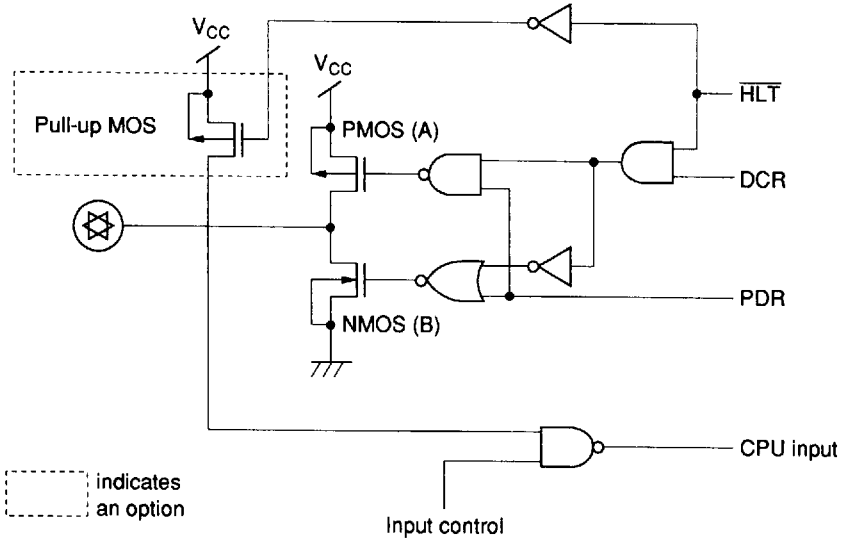


Figure 18 Port Mode Register B Functions



Mask Option		With Pull-Up MOS (B)				With Pull-Up MOS (C)			
DCR (data control register)		0		1		0		1	
PDR (port data register)		0	1	0	1	0	1	0	1
CMOS buffer	PMOS (A)	—	—	—	On	—	—	—	On
	NMOS (B)	—	—	On	—	—	—	On	—
Pull-up MOS (C)		On	On	On	On	—	—	—	—

Notes: 1: On
0: Off
—: Off

Figure 19 I/O Buffer Configuration (Standard Pins)

Table 3 I/O Pin Circuit Types

Standard Pins

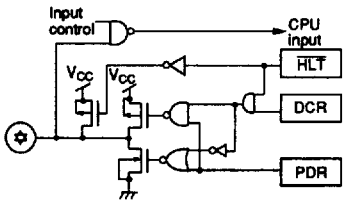
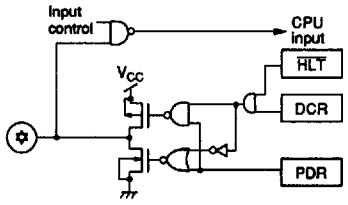
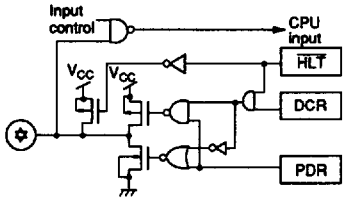
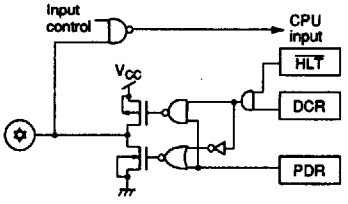
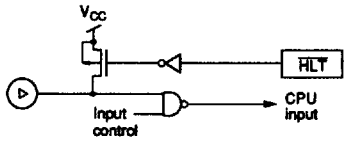
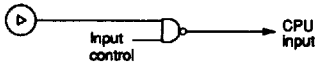
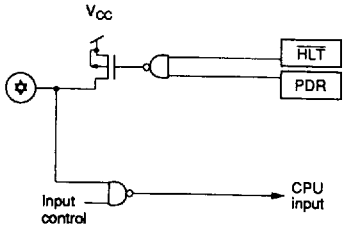
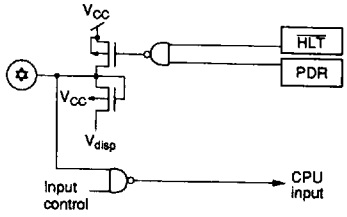
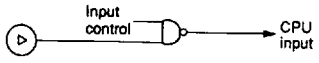
Pin Type	With Pull-Up MOS (B)	Without Pull-Up MOS (C)	Pin Name
I/O common pins			$R3_0$ to $R3_3$
	 Note: Cannot be used as an analog input pin (AN_0 to AN_3).		$R4_0$ to $R4_3$
Input pins			$\overline{INT_0}$, $\overline{INT_1}$

Table 3 I/O Pin Circuit Types (cont)

High-Voltage Pins

Pin Type	Without Pull-Down MOS (D)	With Pull-Down MOS (E)	Pin Name
I/O common pins			D_0 to D_{12}, $R0_0$ to $R0_3$, $R1_0$ to $R1_3$, $R2_0$ to $R2_3$
Input pins			RA_1

Note: In the stop mode, the MCU is reset, peripheral functions cannot be selected, HLT becomes 1, and I/O pins are in high impedance.

Product type \ Circuit type	B	C	D	E
Mask ROM (HD404302R, HD404304)	Option			
ZTAT™ (HD4074308)		Fixed		

Reset

Setting the RESET pin high resets the MCU. At power-on or when cancelling stop mode, the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two instruction cycles are required for the MCU to be reset.
Table 4 shows the components initialized by MCU reset and the status of each after the reset has been carried out.

Note: After reset, the standard pin port data register (PDR) is not stable. Therefore, write the data to the standard pin port data register (PDR) and set data control register (DCR) to output the data.

Table 4 Initial Values after MCU Reset

Item		Initial Value	Contents
Program counter (PC)		$0000	Execute program from the top of ROM address
Status flag (ST)		1	Enable branching with conditional instructions
Stack pointer (SP)		$3FF	Stack level is 0
I/O	High-voltage pin port data register (PDR)	All bits are 0	Enable to output 0
	Standard pin port data register (PDR)	—	Enable to output 1 (with pull-up MOS)
	Data control register (DCR)	All bits are 0	Output buffer is off (high impedance)
	Port mode register A (PMRA)	0000	See Port Mode Register A section
	Port mode register B (PMRB)	0000	See Port Mode Register B section
Interrupt flags/mask	Interrupt enable flag (IE)	0	Inhibit all interrupts
	Interrupt request flag (IF)	0	No interrupt request
	Interrupt mask (IM)	1	Mask interrupt request
Mode registers	Timer mode register A (TMA)	0000	See Timer Mode Register A section
	Timer mode register B (TMB)	0000	See Timer Mode Register B section
Timer/ counter	Timer counter	$00	—
	Timer counter B (TCB)	$00	—
	Timer load register (TLR)	$00	—
	Prescaler	$000	See Prescaler section
A/D	A/D port select register (ADPR)	0000	See A/D Port Select Register section
	A/D mode register (AMR)	0000	See A/D Mode Register section
	A/D data register (ADR)	$80	See A/D Data Register section
	A/D start flag (ADSF)	0	See A/D Start Flag section
Bit register	Watchdog timer on flag (WDON)	0	See Timer A section

Note: Registers and flags except above become as follows after MCU reset.

Table 4 Initial Values after MCU Reset (cont)

Item	Abbr.	After MCU Reset to Recover from Stop Mode	After MCU Reset to Recover from Other Modes
Carry flag	(CA)	The contents of these items following MCU reset are not retained; they must be reinitialized by software	The contents of these items following MCU reset are not retained; they must be reinitialized by software
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX register	(X/SPX)		
Y/SPY register	(Y/SPY)		
RAM		The contents of RAM just before MCU reset (just before a STOP instruction) are retained	

Internal Oscillator Circuit

Figure 20 is a block diagram of the internal oscillator circuit. Refer to table 5 for the selection type. In addition, see figure 21 for the layout of the crystal or ceramic oscillator. In all cases, an external clock operation is available.

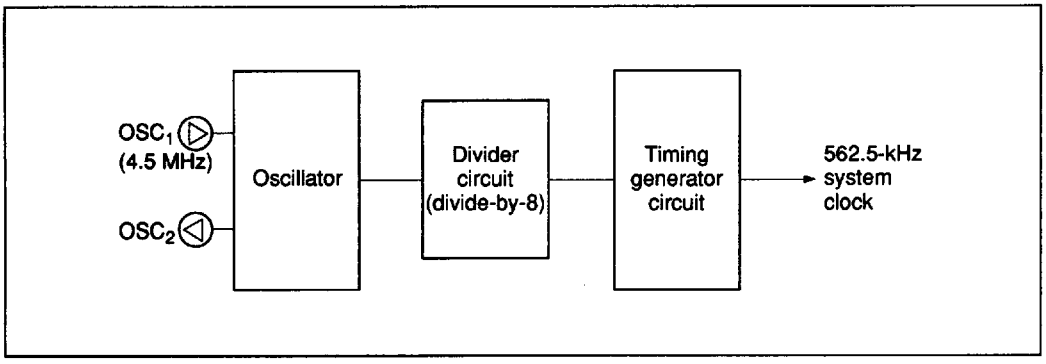


Figure 20 Internal Oscillator Circuit

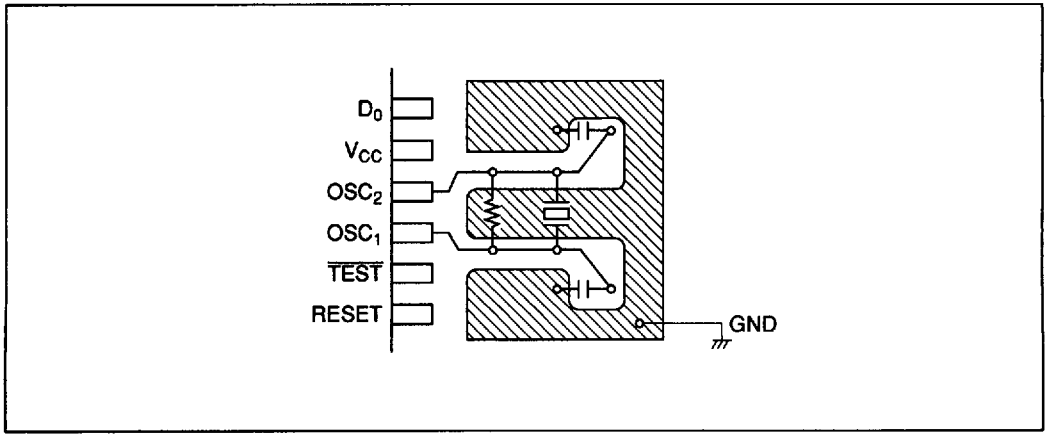
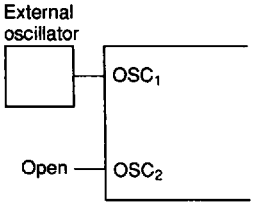
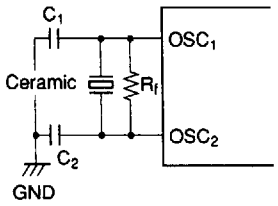
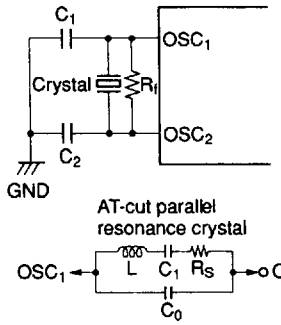


Figure 21 Layout of Crystal and Ceramic Oscillator

Table 5 Example of Oscillator Circuits

	Circuit Configuration	Circuit Constant
External clock operation		
Ceramic oscillator		Ceramic oscillator: CSA 4.00 MG (Murata) R_f = 1 MΩ ±20% C_1 = C2 = 30 pF ±20%
Crystal oscillator		R_f = 1 MΩ ±20% C_1 = 10 pF to 22 pF ±20% C_2 = 10 pF to 22 pF ±20% Crystal: Equivalent to the circuit shown at bottom left C_0 = 7 pF max. R_S = 100 Ω max. f = 1.0 MHz to 4.5 MHz

Notes: 1. The circuit parameters written above are recommended by the crystal or ceramic oscillator manufacturer. The circuit parameters are affected by the crystal, ceramic oscillator, and the floating capacitance when designing the board. When using the resonator, consult with the crystal or ceramic oscillator manufacturer to determine the circuit parameters.

2. Wiring among OSC_1, OSC_2, and other elements should be as short as possible, and avoid crossing other wires. Refer to the recommended layout of the crystal and ceramic oscillator (figure 21).

Low-Power Dissipation Modes

The MCU has two low-power dissipation modes, standby mode and stop mode (table 6). Figure 22 is a mode transition diagram of these modes.

Table 6 Low-Power Dissipation Modes

Condition	Standby Mode	Stop Mode
Instruction	SBY instruction	STOP instruction
Oscillator circuit	Active	Stopped
Instruction execution	Stopped	Stopped
Registers, flags	Retained	Reset*1
Interrupt function	Active	Stopped
RAM	Retained	Retained
Input/output pins	Retained*2	High impedance
Timer/counters	Active	Stopped
A/D	Active	Stopped
Cancellation method	RESET input, interrupt request	RESET input

Notes: 1. The MCU recovers from stop mode by RESET input. Refer to table 4 for the contents of flags and registers.
2. When I/O circuits are active, an I/O current may flow in standby mode, depending on the state of the I/O pins. This is an additional current added to the standby mode current dissipation.

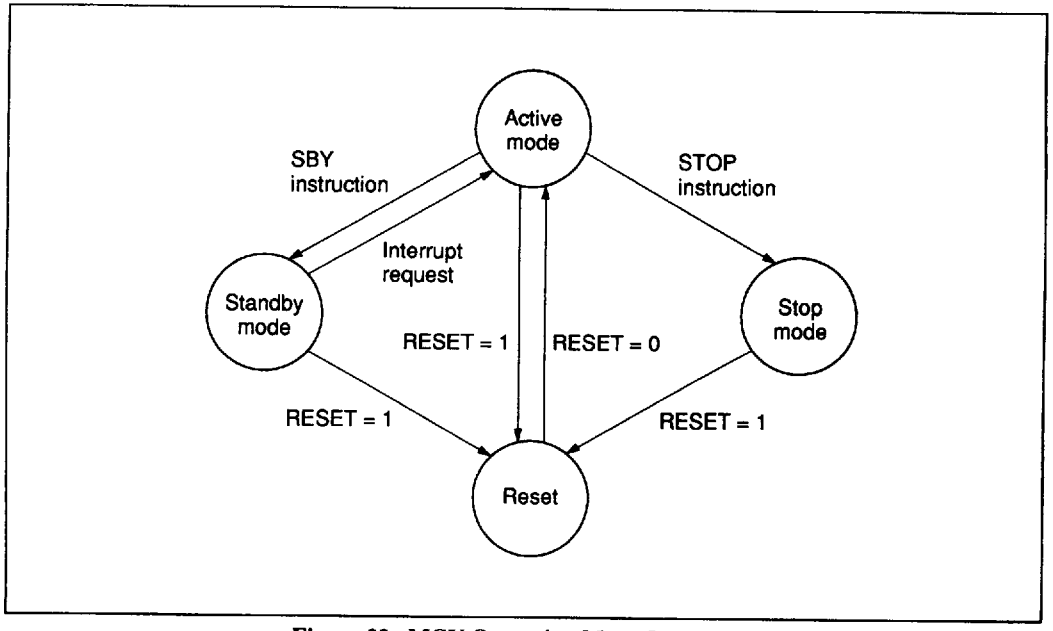


Figure 22 MCU Operation Mode Transition

Standby Mode: Executing the SBY instruction places the MCU into standby mode. In standby mode, the oscillator circuit continues working, and the timer/counter, A/D, and interrupts remain active. On the other hard, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the state they were in just before the MCU went into standby mode.

Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. In the later case, the MCU becomes active and executes the next instruction following the SBY instruction. If the interrupt enable flag is 1 when an interrupt request asserted, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues.

Figure 23 shows the flowchart of the standby mode.

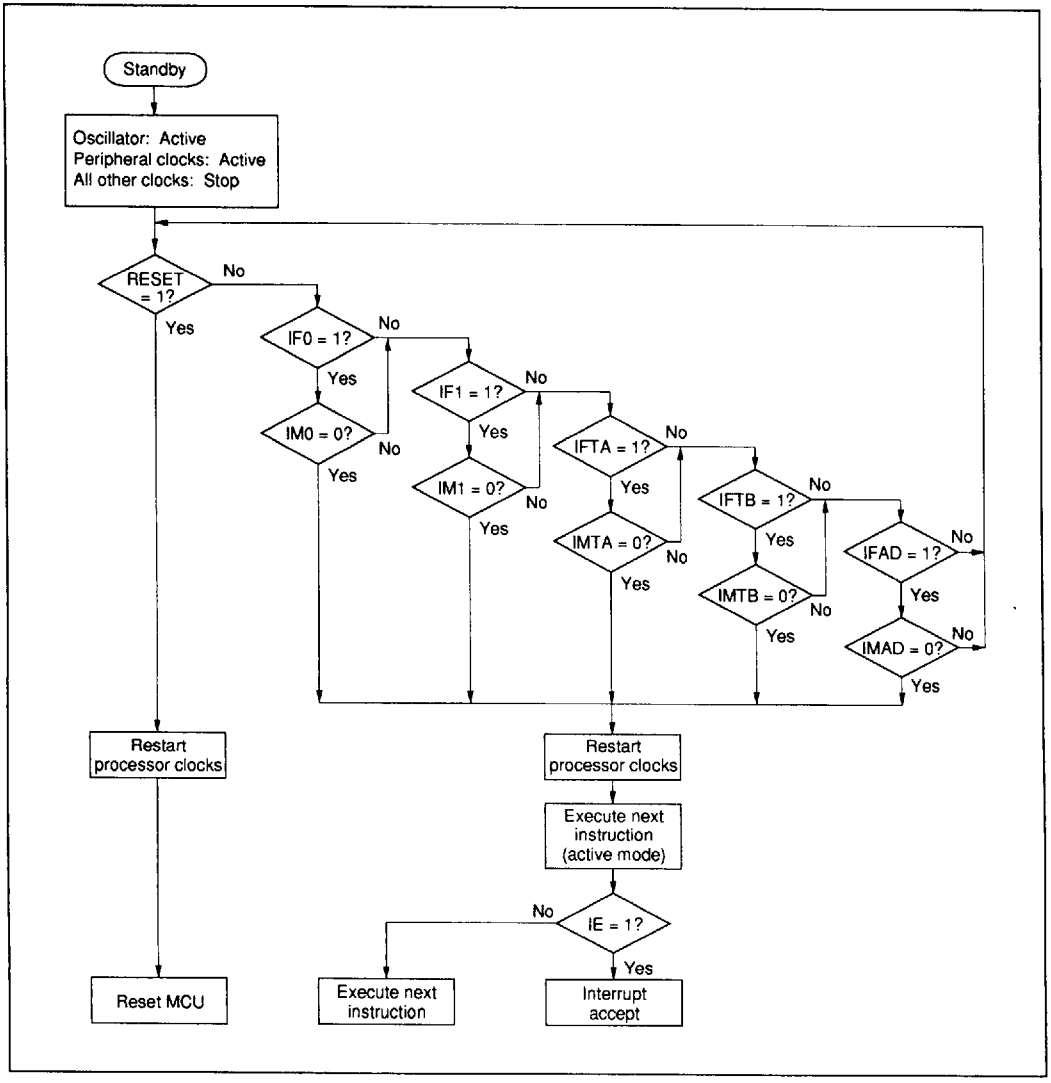


Figure 23 MCU Operating Flowchart in Standby Mode

Stop Mode: Executing the STOP instruction brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

The stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 24, reset input must be applied for at least t_{RC} for oscillation to stabilize. (Refer to AC Characteristics table.) After the stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register, X/SPX registers, Y/SPY registers, carry flag, and A/D data register will not retain their contents.

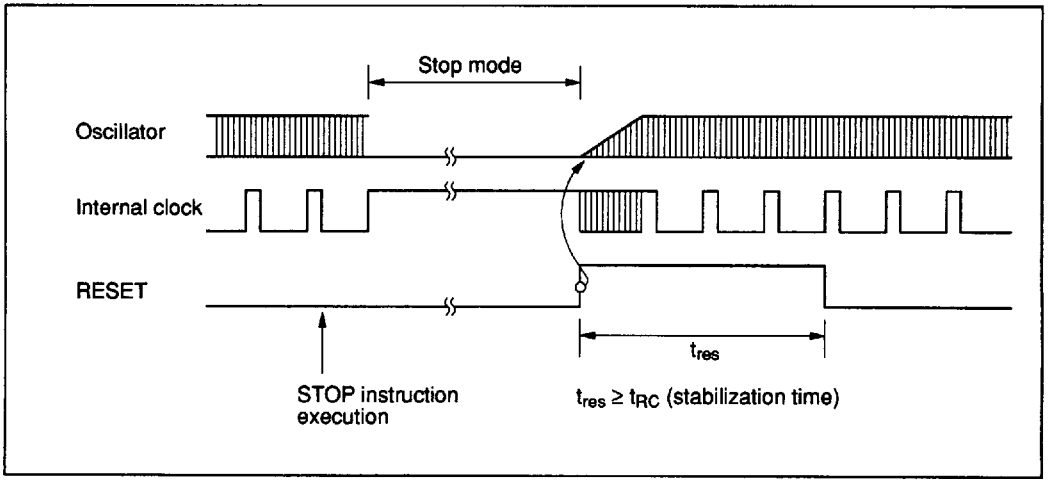


Figure 24 Timing of Stop Mode Cancellation

PROM Mode Pin Description (DP-42, DP-42S, DC-42)

	MCU Mode		PROM Mode	
Pin No.	Pin Name	I/O	Pin Name	I/O
1	D_{10}	I/O	M_2	I
2	D_{11}/TG_0	I/O	V_{CC}	
3	D_{12}/TG_1	I/O	V_{CC}	
4	RA_1/V_{disp}	I		
5	$R0_0$	I/O	A_1	I
6	$R0_1$	I/O	A_2	I
7	$R0_2$	I/O	A_3	I
8	$R0_3$	I/O	A_4	I
9	$R1_0$	I/O	A_5	I
10	$R1_1$	I/O	A_6	I
11	$R1_2$	I/O	A_7	I
12	$R1_3$	I/O	A_8	I
13	$R2_0$	I/O	A_0	I
14	$R2_1$	I/O	A_{10}	I
15	$R2_2$	I/O	A_{11}	I
16	$R2_3$	I/O	A_{12}	I
17	$R3_0$	I/O	O_0	I/O
18	$R3_1$	I/O	O_1	I/O
19	$R3_2/\overline{INT_0}$	I/O	O_2	I/O
20	$R3_3/\overline{INT_1}$	I/O	O_3	I/O
21	GND		GND	
22	AV_{CC}		V_{CC}	
23	$R4_0/AN_0$	I/O	O_4	I/O
24	$R4_1/AN_1$	I/O	O_5	I/O
25	$R4_2/AN_2$	I/O	O_6	I/O
26	$R4_3/AN_3$	I/O	O_7	I/O
27	AV_{SS}		GND	
28	RESET	I	V_{PP}/RESET	
29	$\overline{TEST}$	I	$\overline{TEST}$	I
30	OSC_1	I		
31	OSC_2	O		
32	V_{CC}		V_{CC}	
33	D_0	I/O	M_0	I
34	D_1	I/O	M_1	I
35	D_2	I/O	A_9	I
36	D_3	I/O		
37	D_4	I/O	A_{13}	I
38	D_5	I/O	A_{14}	I
39	D_6	I/O	$\overline{CE}$	I
40	D_7	I/O	$\overline{OE}$	I
41	D_8	I/O		
42	D_9	I/O		

Notes: I/O: Input/output pin
I: Input pin
O: Output pin

PROM Mode Pin Description (FP-54)

	MCU Mode		PROM Mode	
Pin No.	Pin Name	I/O	Pin Name	I/O
1	D_{10}	I/O	M_2	I
2	D_{11}/TG_0	I/O	V_{CC}	
3	D_{12}/TG_1	I/O	V_{CC}	
4	RA_1/V_{disp}	I		
5	$R0_0$	I/O	A_1	I
6	NC			
7	NC			
8	NC			
9	$R0_1$	I/O	A_2	I
10	$R0_2$	I/O	A_3	I
11	$R0_3$	I/O	A_4	I
12	$R1_0$	I/O	A_5	I
13	$R1_1$	I/O	A_6	I
14	$R1_2$	I/O	A_7	I
15	$R1_3$	I/O	A_8	I
16	$R2_0$	I/O	A_0	I
17	$R2_1$	I/O	A_{10}	I
18	$R2_2$	I/O	A_{11}	I
19	$R2_3$	I/O	A_{12}	I
20	NC			
21	NC			
22	NC			
23	$R3_0$	I/O	O_0	I/O
24	$R3_1$	I/O	O_1	I/O
25	$R3_2/\overline{INT_0}$	I/O	O_2	I/O
26	$R3_3/\overline{INT_1}$	I/O	O_3	I/O
27	GND		GND	
28	AV_{CC}		V_{CC}	
29	$R4_0/AN_0$	I/O	O_4	I/O
30	$R4_1/AN_1$	I/O	O_5	I/O
31	$R4_2/AN_2$	I/O	O_6	I/O
32	$R4_3/AN_3$	I/O	O_7	I/O
33	NC			
34	NC			
35	NC			
36	AV_{SS}		GND	
37	RESET	I	V_{PP}/RESET	
38	$\overline{TEST}$	I	$\overline{TEST}$	I
39	OSC_1	I		
40	OSC_2	O		
41	V_{CC}		V_{CC}	
42	D_0	I/O	M_0	I
43	D_1	I/O	M_1	I
44	D_2	I/O	A_9	I
45	D_3	I/O		
46	D_4	I/O	A_{13}	I
47	NC			
48	NC			
49	NC			
50	D_5	I/O	A_{14}	I
51	D_6	I/O	$\overline{CE}$	I
52	D_7	I/O	$\overline{OE}$	I
53	D_8	I/O		
54	D_9	I/O		

Notes: I/O: Input/output pin
I: Input pin
O: Output pin
NC: No connection

Programmable ROM (HD4074308)

The MCU on-chip PROM is programmed in PROM mode. PROM mode is set by pulling $\overline{TEST}$ low, and RESET, M_0, M_1, and M_2 high, as shown in figure 25. In PROM mode, the MCU does not operate. Table 7 shows the PROM mode selection. It can be programmed like a standard 27256 EPROM using a standard PROM programmer and a 42-to-28-pin socket adapter. Table 8 lists recommended PROM programmers and socket adapters.

Since an instruction of the HMCS400 series consists of 10 bits, the HMCS400 series MCU incorporates a conversion circuit to enable the use of a general-purpose PROM programmer. By this circuit, an instruction is read or programmed using 2 addresses, generated as the lower 5 bits and upper 5 bits. For example, if 8 kwords of on-chip PROM are programmed by a general-purpose PROM programmer, 16 kbytes of addresses ($0000-$3FFF) should be specified.

Programming and Verification

The MCU can be high-speed programmed without causing voltage stress or affecting data reliability.

Table 7 shows how programming and verification modes are selected.

Erasing

PROMs with ceramic window packages can be erased by ultraviolet light. All erased bits are set to 1.

Erasing conditions are: ultraviolet (UV) light with a wavelength of 2537 Å with a minimum irradiation of 15 W·sec/cm^2. These conditions are satisfied by exposing the LSI to a 12,000-μW/cm^2 UV source for 15 to 20 minutes at a distance of 1 inch.

Precautions

1. Addresses $0000 to $3FFF must be specified if the PROM is programmed by a PROM programmer. If addresses of $4000 or higher are accessed, the PROM may not be programmed or verified. Note that the plastic type packages cannot be erased and reprogrammed. (Ceramic window packages can be erased and re-programmed by ultraviolet light.) Data in unused addresses must be set to $FF.

2. Be sure that the PROM programmer, socket adapter, and LSI are inserted correctly (pin 1 positions match). Using the wrong programmer or socket adapter may cause an overvoltage and damage the LSI (table 8). Make sure that the LSI is firmly fixed in the socket adapter, and that the socket adapter is firmly fixed onto the programmer.

3. The PROM should be programmed with V_{PP} = 12.5 V. Other PROMs use 21 V. If 21 V is applied to the MCU, the LSI may be permanently damaged. 12.5 V is Intel's 27256 V_{PP}.

Table 7 PROM Modes Selection

	Pin			
Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	O_0 to O_7
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Table 8 PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Manufacturer	**Type Name**	**Manufacturer**	**Package**	**Type Name**
DATA I/O	22B	Hitachi	DP-42	HS430ESD01H
	29B		DP-42S	HS430ESS01H
			FP-54	HS430ESF01H
AVAL Corp.	PKW-1100	Hitachi	DP-42	HS430ESD01H
	PKW-1000		DP-42S	HS430ESS01H
			FP-54	HS430ESF01H

Note: An automatic programming mode of the PROM programmer is not available, therefore if a silicon signature check is performed, the A9 port will be permanently damaged. The A9 port is a high-voltage I/O port of the MCU. It will be damaged if an overvoltage (12.5 V) exceeding the voltage resistance of the MCU buffer is applied.
When a connection check is made using a protection diode between the MCU and its socket, an open error occurs on an address port. Since the direction of the protection diode of the MCU high-voltage pin is reversed, the address port is regarded as open.

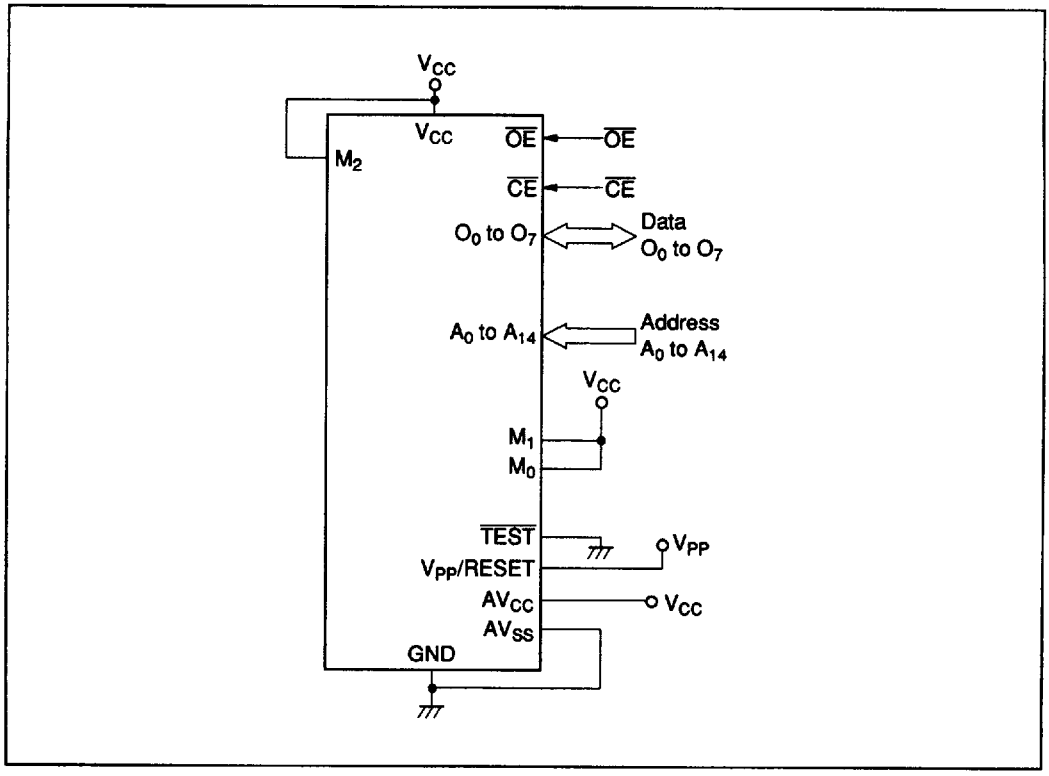


Figure 25 Connections for PROM Mode

Addressing Modes

RAM Addressing Modes

As shown in figure 26, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing Mode: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing Mode: The memory registers (16 digits from $040 to $04F) are accessed by executing the LAMR and XMRA instructions.

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes as shown in figure 27.

Direct Addressing Mode: The program can branch to any address in ROM memory space by executing the JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC_{13} to PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 8 pages of ROM with 256 words per page. By executing the BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order 8 bits of the program counter (PC_7 to PC_0) with 8-bit immediate data.

When the BR instruction is on a page boundary (256n + 255) (figure 28), executing it transfers the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when the BR instruction is used on a page boundary. The HMCS400-series cross macroassembler has an automatic paging facility for ROM pages.

Zero-Page Addressing Mode: By executing the CAL instruction, the program can branch to the zero-page subroutine area, which is located at $0000–$003F. When the CAL instruction is executed, 6 bits of immediate data are placed in the low-order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order eight bits (PC_{13} to PC_6).

Table Data Addressing Mode: By executing the TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referenced by the P instruction (figure 29). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output registers. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

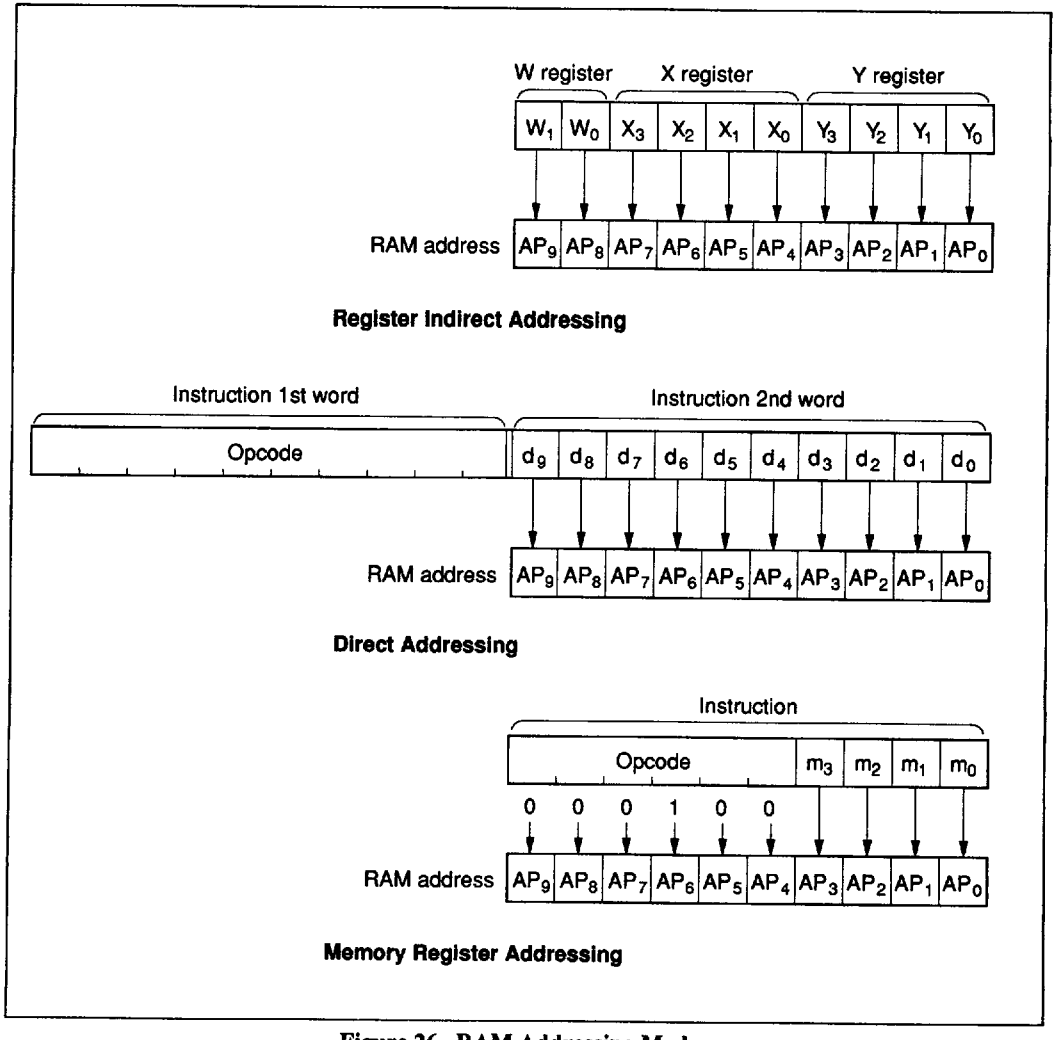


Figure 26 RAM Addressing Modes

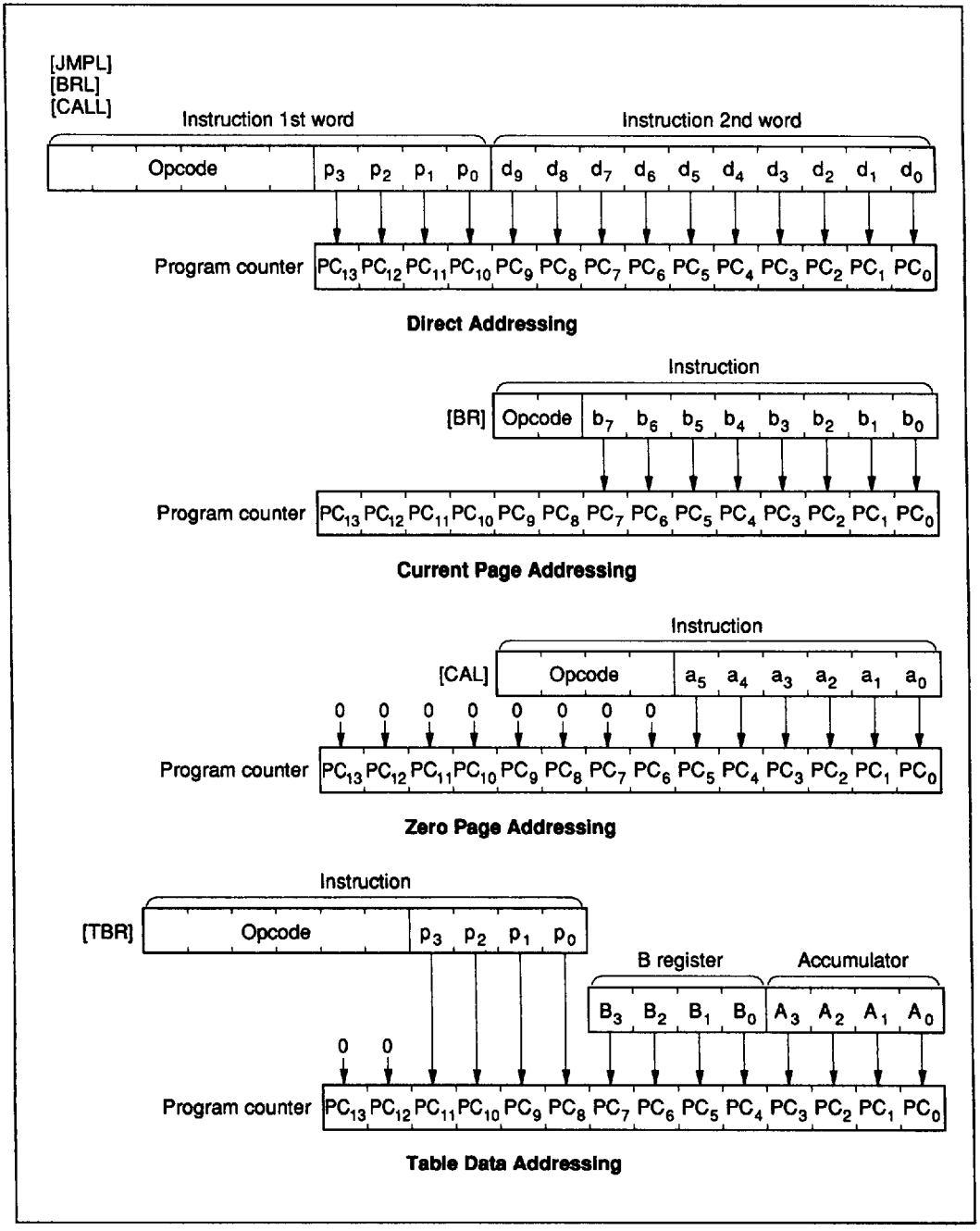


Figure 27 ROM Addressing Modes

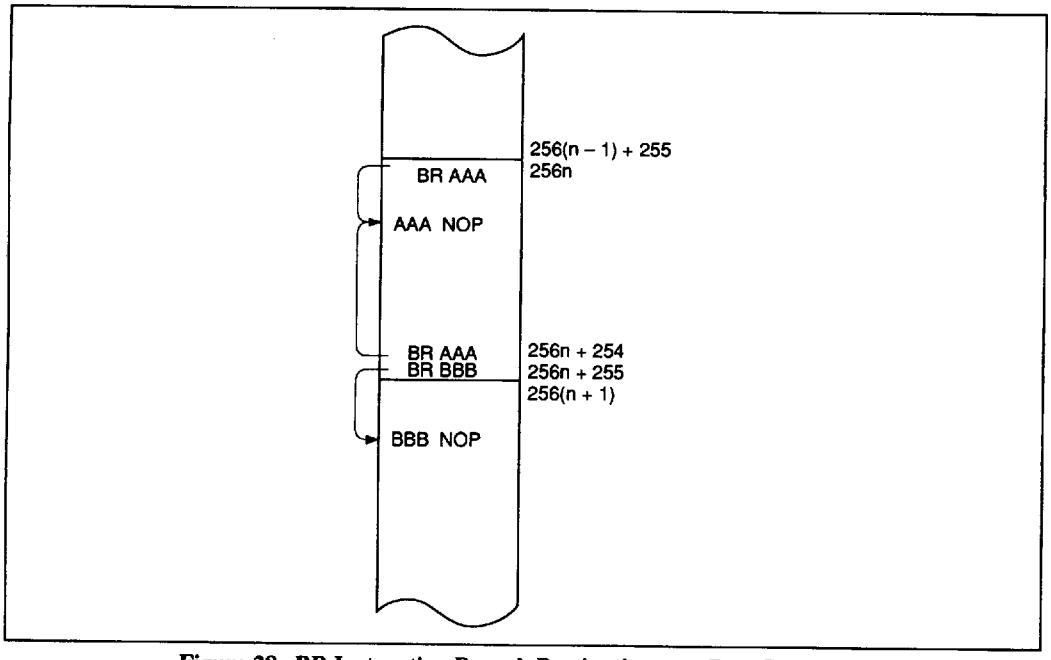


Figure 28 BR Instruction Branch Destination on a Page Boundary

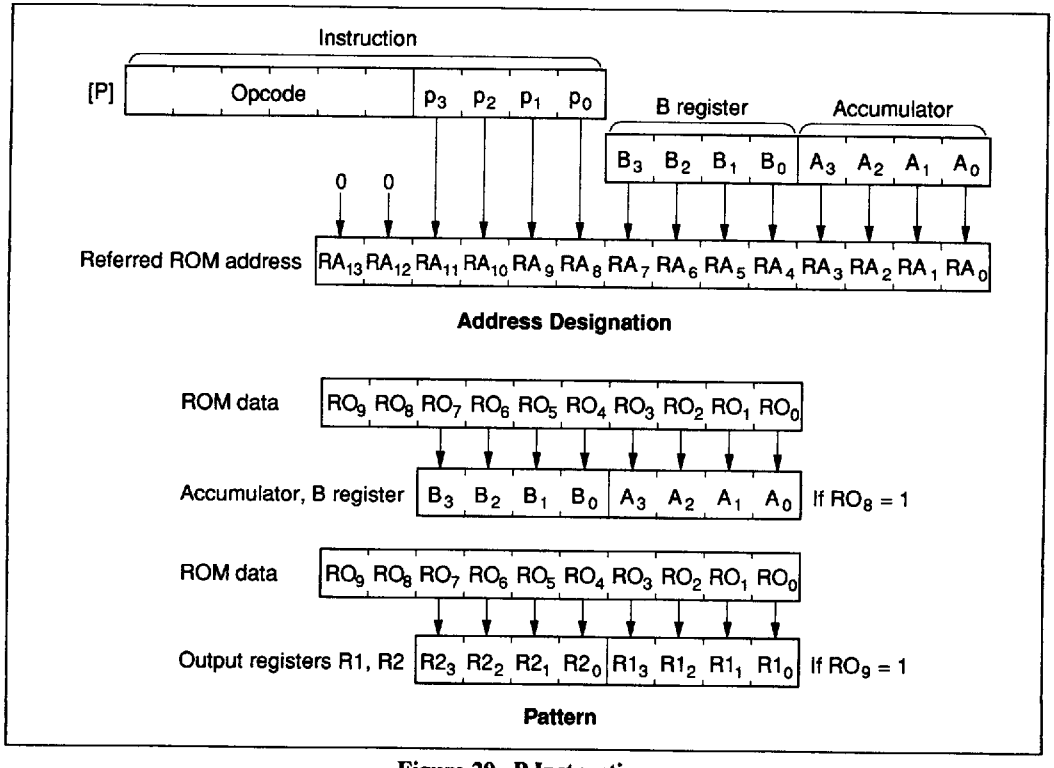


Figure 29 P Instruction

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	−0.3 to +7.0	V	1, 12
Program voltage	V_{PP}	−0.3 to +14.0	V	2
Pin voltage	V_T	−0.3 to V_{CC} + 0.3	V	3
		V_{CC} − 45 to V_{CC} + 0.3	V	4
Total permissible input current	ΣI_0	50	mA	5
Maximum input current	I_0	15	mA	7, 8
Maximum output current	$-I_0$	4	mA	8, 9
		6	mA	9, 10
		30	mA	9, 11
Total permissible output current	$-\Sigma I_0$	150	mA	6
Operation temperature	T_{opr}	−20 to +75	°C	
Storage temperature	T_{stg}	−55 to +125	°C	

Notes:
1. Normal operation should be performed under the conditions specified by the electrical characteristics. Exceeding these conditions can result in malfunction, degraded performance, and permanent damage to the LSI.
2. Applies to the RESET pin (V_{PP}). (HD4074308)
3. Applies to pins other than high-voltage pins.
4. Applies to high-voltage pins.
5. Total permissible input current is the sum of input currents which flow in from all I/O pins to GND simultaneously.
6. Total permissible output current is the sum of output currents which flow from V_{CC} to all I/O pins simultaneously.
7. Maximum input current is the amount of input current allowed from each I/O pin to GND.
8. Applies to R3 and R4.
9. Maximum output current is the amount of output current allowed from V_{CC} to each I/O pin.
10. Applies to R0 to R2.
11. Applies to D_0 to D_{12}.
12. Voltage is based on GND.

Electrical Characteristics

DC Characteristics (V_{CC} = 5 V ±10%, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	RESET, $\overline{INT_0}$, $\overline{INT_1}$	0.8V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	RESET, $\overline{INT_0}$, $\overline{INT_1}$	–0.3	—	0.2V_{CC}	V		
		OSC_1	–0.3	—	0.5	V		
Input/output leakage current	$\lvert I_{IL} \rvert$	RESET, $\overline{INT_0}$, $\overline{INT_1}$, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	3.0	mA	V_{CC} = 5 V; f_{OSC} = 4 MHz	2, 5
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	1.5	mA	V_{CC} = 5 V; f_{OSC} = 4 MHz	3, 5
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	$V_{in(\overline{TEST})}$ = V_{CC} $V_{in(RESET)}$ = GND	4
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes: 1. Excluding pull-up MOS current and output buffer current.
2. The MCU is in the reset state. Input/output current does not flow.
   - MCU in reset state, operation mode
   - RESET, $\overline{TEST}$: V_{CC}
   - R3, R4: V_{CC}
   - D_0 to D_{12}, R0 to R2, RA_1: V_{disp}
3. The timer/counter operates with the fastest clock. Input/output current does not flow.
   - MCU in standby mode
   - Input/output in reset state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - R3, R4: V_{CC}
   - D_0 to D_{12}, R0 to R2, RA_1: V_{disp}
4. Excluding pull-down MOS current.
5. When f_{OSC} = x MHz estimate the current dissipation as follows:
   Max. value f_{OSC} = x MHz = x/4 × (max. value f_{OSC} = 4 MHz)

Input/Output Characteristics for Standard Pins (V_{CC} = 5 V ±10%, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	R3, R4	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	R3, R4	–0.3	—	$0.2V_{CC}$	V		
Output high voltage	V_{OH}	R3, R4	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA	1
			V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.5 mA	1
Output low voltage	V_{OL}	R3, R4	—	—	0.4	V	I_{OL} = 1.6 mA	
Input/output leakage current	$\lvert I_{IL} \rvert$	R3, R4	—	—	1	µA	V_{in} = 0 V to V_{CC}	2
Pull-up MOS current	$-I_{PU}$	R3, R4	30	70	150	µA	V_{CC} = 5 V, V_{in} = 0 V	3

Notes: 1. Applied to I/O pins selected as CMOS output by mask option.
2. Pull-up MOS current and output buffer current are excluded.
3. Applied to I/O pins selected as with pull-up MOS by mask option.

Input/Output Characteristics for High Voltage Pins (V_{CC} = 5 V ±10%, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C unless otherwise specified)

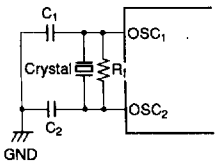
Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0 to D_{12}, R1, R2, RA_1, R0	0.7V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0 to D_{12}, R1, R2, RA_1, R0	V_{CC} – 40	—	0.2V_{CC}	V		
Output high voltage	V_{OH}	D_0 to D_{12}, TG_0, TG_1	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 10 mA	
			V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 4 mA	
		R0 to R2	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 3 mA	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 2 mA	
			V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 0.8 mA	
Output low voltage	V_{OL}	D_0 to D_{12}, R0 to R2	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	1
		D_0 to D_{12}, R0 to R2	—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V	2
Input/output leakage current	$\lvert I_{IL} \rvert$	D_0 to D_{12}, R0 to R2, RA_1	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down MOS current	I_{PD}	D_0 to D_{12}, R0 to R2	200	400	800	µA	HD404302R, HD404304: V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

Notes: 1. Applied to I/O pins selected as with pull-up MOS by mask option.
2. Applied to I/O pins selected as without pull-up MOS (PMOS open drain) by mask option.
3. Pull-up MOS current and output buffer current are excluded.

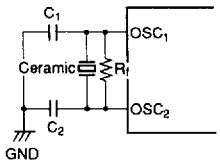
AC Characteristics (V_{CC} = 5 V ±10%, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Oscillation frequency (divide-by-8)	f_{OSC}	OSC_1, OSC_2	0.4	4	4.5	MHz		
Instruction cycle time	t_{cyc}		1.78	2	20	µs		
Oscillation stabilization time	t_{RC}	OSC_1, OSC_2	—	—	20	ms	(Ceramic oscillator)	1
					40	ms	(Crystal)	
External clock frequency	t_{CP}	OSC_1	0.4	—	4.5	MHz		
External clock high and low widths	t_{CPH}, t_{CPL}	OSC_1	92	—	—	ns	Divide-by-8	2
External clock rising and falling times	t_{CPr}, t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT_0}$ high and low widths	t_{IH}, t_{IL}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ high and low widths	t_{IH}, t_{IL}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}		4
Input capacitance	HD404302R/ HD404304 C_{in}	All pins (except RESET)	—	—	30	pF	—	
		RESET	—	—	30	pF	—	
	HD4074308 C_{in}	All pins (except RESET)	—	—	20	pF	f = 1 MHz, V_{in} = 0 V	
		RESET	—	—	250	pF	f = 1 MHz, V_{in} = 0 V	
RESET falling time	t_{RSTf}	RESET	—	—	20	ms		4

Notes: 1. The oscillation stabilization time is the period from when V_{CC} reaches 4.5 V at power-on until when the oscillator stabilizes, or after RESET goes to high to quit the stop mode. At power-on or when cancelling the stop mode, RESET must remain high for at least t_{RC}. Since t_{RC} depends on the crystal or ceramic oscillator's circuit constant and stray capacitance, it is recommended that the user follow the crystal or ceramic oscillator manufacturer's recommendations when designing the reset circuit. Applies to the HD404302R, HD4074308, and HD404304.



Crystal: HC-491U
(4.19304 MHz: Kinseki)
R_f = 1 MΩ ±20%
C_1 = C_2 = 20 pF ±20%



Ceramic oscillator: CSA 4.00 MG
(Murata)
R_f = 1 MΩ ±20%
C_1 = C_2 = 30 pF ±20%

2. See figure 30.
3. See figure 31.
4. See figure 32.

A/D Converter Characteristics (V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = GND, T_a = 0°C to +70°C)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Analog power supply voltage	AV_{CC}	AV_{CC}	V_{CC} – 0.3	V_{CC}	V_{CC} + 0.3	V		
Analog input voltage	AV_{in}	AN_0 to AN_3	AV_{SS}	—	AV_{CC}	V		
Current between AV_{CC} and AV_{SS}	I_{AD}		—	0.08	—	mA		
Analog input capacity	CA_{in}	AN_0 to AN_3	—	15	—	pF		
Resolution	—	—	—	8	—	Bit		
Conversion time	—	—	61	—	536	µs		1
Number of inputs	—	—	0	—	4	Channel		
Absolute accuracy	—	—	—	—	±2	LSB	T_a = 25°C, V_{CC} = 5.0 V, f_{osc} = 1 MHz to 4.5 MHz	1, 2
Input impedance	—	AN_0 to AN_3	1 M	—	—	Ω		

Notes: 1. The operating frequency f_{OSC} of the A/D conversion is from 1 MHz to 4.5 MHz.
2. When using the R4/AN port as an analog input, the I/O option of the R4 port must be set as without pull-up MOS.

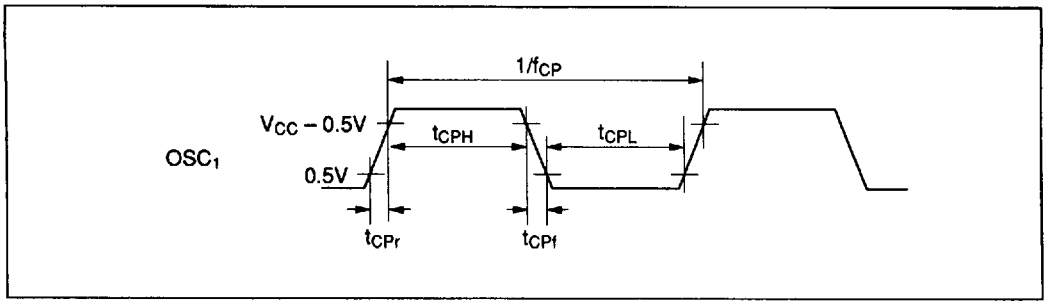


Figure 30 Oscillator Timing

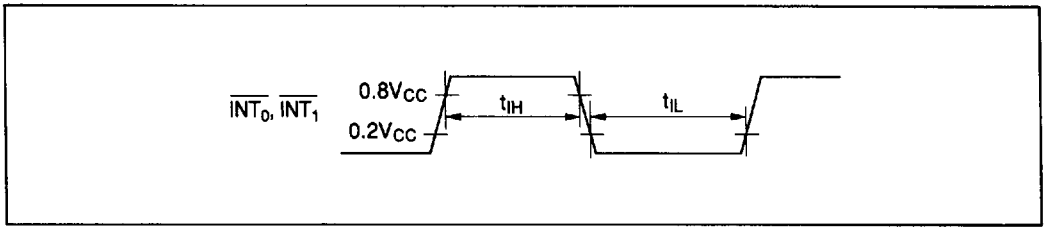


Figure 31 Interrupt Timing

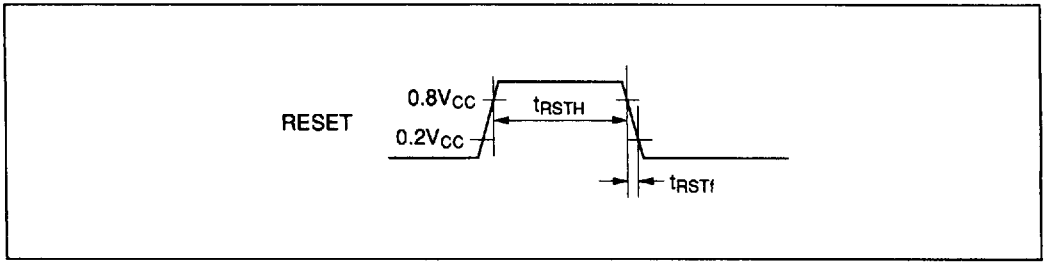


Figure 32 Reset Timing

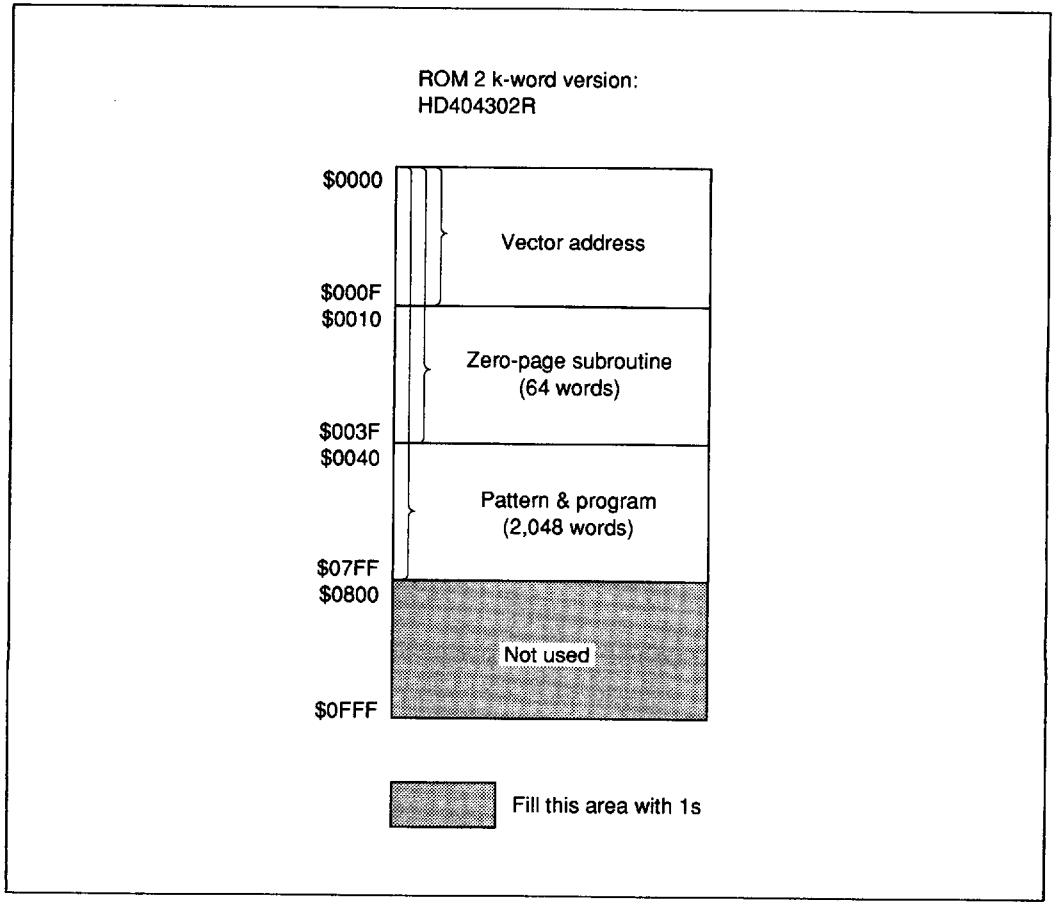
Notes on ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size for the HD404302R as an 4 k-word version (HD404304).

The 4 k-word data size is required to change ROM data to mask manufacturing data since the program used is for a 4 k-word version.

This limitation applies when using an EPROM or a data base.



HD404302R and HD404304 Option List

Please check off the appropriate applications and enter the necessary information.

Order data	
Company name	
Department	
Name	
ROM code	
LSI type:	

1. ROM size

☐ HD404302R	2-kword
☐ HD404304	4-kword

2. I/O option

Note: I/O options masked by ▒ are not available

Pin name		I/O		I/O option				
				A	B	C	D	E
D0		High-voltage pins	I/O	▒	▒	▒		
D1			I/O	▒	▒	▒		
D2			I/O	▒	▒	▒		
D3			I/O	▒	▒	▒		
D4			I/O	▒	▒	▒		
D5			I/O	▒	▒	▒		
D6			I/O	▒	▒	▒		
D7			I/O	▒	▒	▒		
D8			I/O	▒	▒	▒		
D9			I/O	▒	▒	▒		
D10			I/O	▒	▒	▒		
D11			I/O	▒	▒	▒		
D12			I/O	▒	▒	▒		
RA	RA1		I	Selected in option 3				
R0	R00		I/O	▒	▒	▒		
	R01		I/O	▒	▒	▒		
	R02		I/O	▒	▒	▒		
	R03		I/O	▒	▒	▒		

Pin name		I/O		I/O option				
				A	B	C	D	E
R1	R10	High-voltage pins	I/O	▒	▒	▒		
	R11		I/O	▒	▒	▒		
	R12		I/O	▒	▒	▒		
	R13		I/O	▒	▒	▒		
R2	R20		I/O	▒	▒	▒		
	R21		I/O	▒	▒	▒		
	R22		I/O	▒	▒	▒		
	R23		I/O	▒	▒	▒		
R3	R30	Standard pins	I/O	▒			▒	▒
	R31		I/O	▒			▒	▒
	R32		I/O	▒			▒	▒
	R33		I/O	▒			▒	▒
R4*	R40		I/O	▒			▒	▒
	R41		I/O	▒			▒	▒
	R42		I/O	▒			▒	▒
	R43		I/O	▒			▒	▒

B: CMOS output with pull-up MOS
C: CMOS
D: Without pull-down MOS (PMOS open drain)
E: With pull-down MOS

Note: * If pin R4/AN is used for analog input, select it with CMOS output (I/O option C).

3. RA1/Vdisp

☐ RA1: Without pull-down MOS (D)
☐ Vdisp

Note: If even one high-voltage pin is selected with I/O option E, pin RA1/Vdisp must be selected to function as Vdisp.

4. ROM code media
Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

5. System oscillator for OSC1 and OSC2

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

6. Stop mode

☐ Used
☐ Not used

7. Package

☐ DP-42
☐ DP-42S
☐ FP-54