DALLAS SEMICONDUCTOR

DS3150
3.3V
T3 / E3 / STS-1
Line Interface

Preliminary Data Sheet
Version 1
August 20, 1999

REVISION HISTORY

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Original release.

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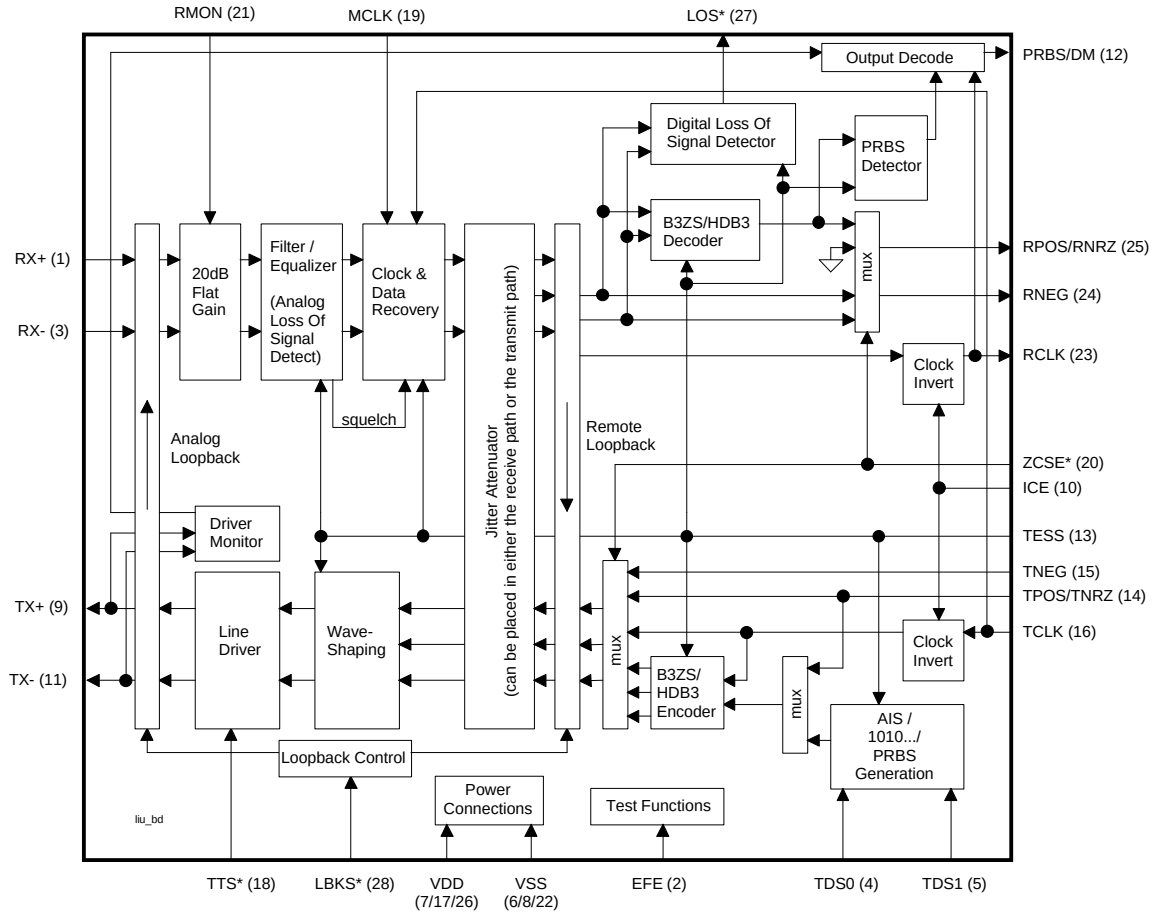
SECTION 1: FUNCTIONAL DESCRIPTION

The DS3150 performs all of the functions necessary for interfacing at the physical layer to T3, E3, and STS-1 lines. The device has independent receive and transmit paths. See Figure 1A. The receiver performs clock and data recovery and monitors for the loss of the incoming signal. The recovered data can be B3ZS/HDB3 decoded and output in a NRZ format. The transmitter accepts either NRZ or bipolar data and will create the waveforms that will be driven onto the T3, E3, or STS-1 COAXial (COAX) cable. Each of these sections will be discussed separately below. Table 1A lists the primary features in the DS3150. Table 1B lists the telecommunications standards that the DS3150 was designed to meet.

DS3150 Block Diagram Figure 1A



Feature List Table 1A

- Integrated transmit & receive T3 (44.736Mbps) / E3 (34.368Mbps) / STS-1 (51.84Mbps) line interface
- Performs clock/data recovery & wave shaping
- Requires no special external components others than 1:2 transformers
- Interfaces to 75 ohm coaxial cable at lengths up to 380 meters (T3), 440 meters (E3), or 360 meters (STS-1)
- Adaptive receive equalizer handles from 0db to 15dB of cable loss
- Jitter attenuator that can be placed either in the receive path or the transmit path or disabled
- Low power 3.3V operation with 5V tolerant I/O
- Pin compatible to the TDK 78P7200 & 78P2241 footprint
- Transmit & Receive interfaces use the same transformer (1:2)
- Onboard B3ZS and HDB3 coder/decoder
- Bipolar and NRZ interfaces
- Analog and digital loopbacks
- Onboard $2^{15} - 1$ and $2^{23} - 1$ Pseudo Random Bit Sequence (PRBS) generator & detector
- Transmit line driver monitor that checks for a faulty transmitter or a shorted output
- Complete T3 AIS generator according to ANSI T1.107
- Unframed all ones generator (E3 AIS)
- Digital clock edge control (clock inversion capability)
- Tri-state capable line driver which places the device into a low power mode
- Able to interface directly to a DSX monitor signal (20dB flat loss)
- Loss of signal detector per ANSI T1.231-1999 and ITU G.775
- Industrial temperature operating range (-40°C to +85°C)
- Small 28-pin PLCC package

Applicable Standards Table 1B

1) American National Standard for Telecommunications - **ANSI T1.107 – 1995** "Digital Hierarchy - Formats Specification"
2) American National Standard for Telecommunications - **ANSI T1.231 - 199X** – Draft "Digital Hierarchy - Layer 1 In-Service Digital Transmission Performance Monitoring"
3) American National Standard for Telecommunications - **ANSI T1.231 – 1993** "Digital Hierarchy - Layer 1 In-Service Digital Transmission Performance Monitoring"
4) American National Standard for Telecommunications - **ANSI T1.404 – 1994** "Network-to-Customer Installation - DS3 Metallic Interface Specification"
5) American National Standard for Telecommunications - **ANSI T1.102 – 1993** "Digital Hierarchy – Electrical Interfaces"
6) Bellcore - **GR-499-CORE**, Issue 1, December 1995 "Transport Systems Generic Requirements (TSGR): Common Requirements"
7) Bellcore - **GR-253-CORE**, Issue 2, December 1995 "SONET Transport Systems: Common Generic Criteria"
8) International Telecommunication Union (ITU) **G.703**, 1991 "Physical/Electrical Characteristics of Hierarchical Digital Interfaces
9) International Telecommunication Union (ITU) **G.823**, March 1993 "The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy"
10) International Telecommunication Union (ITU) **G.775**, November 1994 "Loss Of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria"
11) International Telecommunication Union (ITU) **O.151**, October 1992 "Error Performance Measuring Equipment Operating at the Primary Rate and Above"
12) European Telecommunications Standards Institute (ETSI) **TBR 24**, July 1997 "Business TeleCommunications; 34Mbit/s digital unstructured and structured lease lines; attachment requirements for terminal equipment interface
13) European Telecommunications Standards Institute (ETSI) **ETS 300 687**, March 1996 "Business TeleCommunications; 34Mbit/s digital leased lines (D34U and D34S); Connection characteristics
14) European Telecommunications Standards Institute (ETSI) **ETS 300 686**, March 1996 "Business TeleCommunications; 34Mbit/s and 140Mbits/s digital leased lines (D34U, D34S, D140U and D140S); Network interface presentation

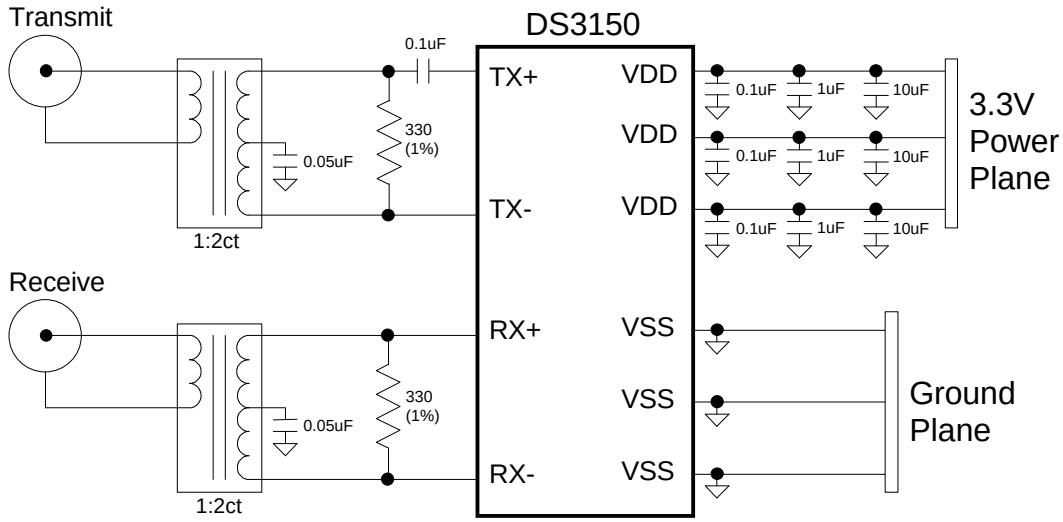
Receiver

The DS3150 interfaces to the receive T3/E3/STS-1 COAX line via a 1:2 step up transformer. See Figure 1B. The receiver automatically adapts to COAX cable loses from 0 to 15dB which translates into 0 to 380 meters (T3) or 440 meters (E3) or 360 meters (STS-1) of COAX cable (AT&T 734A or equivalent). The receiver has the ability to interface to monitor jacks as well. Via the RMON input (see Table 2A), the device can be configured to insert a 20dB flat boost into the incoming signal. Monitor jacks typically have series resistors that result in a resistive loss of 20dB. The receiver has excellent jitter tolerance characteristics. See Figure 1C.

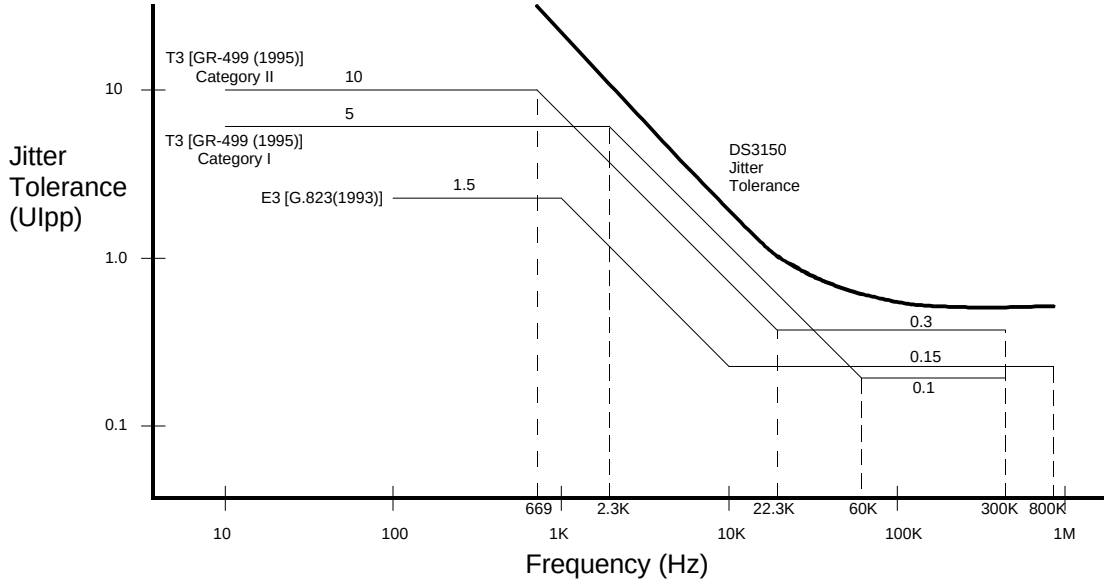
The receiver contains both analog and a digital loss of signal detectors. The analog loss of signal detector resides in the equalizer. If the incoming signal drops below -24dB of the nominal signal level, the analog loss of signal detector will activate and it will squelch the recovered data and force all zeros out of the data recovery circuitry. The analog loss of signal detector will not clear until the signal level is above -18dB of the nominal signal level. The digital Loss Of Signal (LOS) detector is activated when it detects 192 consecutive zeros. LOS is cleared when there are no Excessive Zero occurrences over a span of 192 clock periods. An Excessive Zero occurrence is defined as 3 or more consecutive zeros in the T3 & STS-1 modes and 4 or more zeros in the E3 mode. The status of the digital LOS is reflected at the LOS* output (see Table 2A). There is no status output available for the analog loss of signal detector. While the device is in a loss of signal state, the RCLK output will be referenced to the MCLK input (or the TCLK input if MCLK is tied low). The analog loss of signal detector has a longer time constant than the digital LOS. Hence when the incoming signal is lost, the digital LOS will fire first followed by the analog loss of signal detector. When a signal is restored, the digital LOS will not be allowed to qualify a signal for no Excessive Zero violations until the analog loss of signal detector has seen the signal rise above –18dB. Governing specifications for the loss of signal detectors is ANSI T1.231 and ITU G.775.

The recovered data from the receiver can be output in either it's native form (which is a bipolar format) or a Non Return to Zero (NRZ) format. To select the bipolar format, the ZCSE* input is tied high. In this format, the B3ZS/HDB3 decoder is disabled and the raw data as recovered is buffered and then output on the RPOS and RNEG outputs. To select the NRZ format, the ZCSE* input is tied low. In this format, the B3ZS/HBD3 decoder is enabled and the recovered data is B3ZS/HBD3 decoded and then logically OR'ed together and output at the RPOS output while the RNEG output is forced low.

DS3150 External Connection Figure 1B



DS3150 Jitter Tolerance Figure 1C



Transmitter
Via the ZCSE* input, the device is configured to accept either bipolar data or NRZ data to be input to the transmitter. When the ZCSE* input is tied high, bipolar data must be applied at the TPOS and TNEG inputs. In this mode, the device will not B3ZS/HDB3 encode the outgoing data stream. When the ZCSE* input is tied low, a NRZ data stream must be applied at the TPOS input (TNEG is ignored). In this mode, the device will B3ZS/HDB3 encode the outgoing data stream.

The clock applied at the TCLK input is used to transmit data out onto the T3/E3/STS-1 line. Hence TCLK must be of transmission quality (i.e. accurate to ±20ppm). The duty cycle of TCLK is not a key parameter as long as the clock high and low times listed in Section 3 are met.

The DS3150 also has ability to generate a number of different patterns. It can generate either an unframed all ones pattern (which is also the E3 AIS signal), a 101010… pattern, or a T3 Alarm Indication Signal (AIS). See Figure 1E for a description of the T3 AIS. The TDS0 and TDS1 inputs are used to select these onboard patterns. See Tables 2A and 2B.

The DS3150 interfaces to the transmit T3/E3/STS-1 COAX cable via a 1:2 step up transformer. See Figure 1B. It will drive the 75 ohm cable and create the proper waveforms required for interfacing to T3/E3/STS-1 lines. Tables 1C through 1G and Figure 1D detail the waveform template specifications and testing parameters.

The transmitter can be disabled and the TX+ and TX- outputs tri-stated via the TTS* input. See Table 2A for details.

The transmit driver monitor constantly checks the analog signal output at TX+ and TX-. If the output fails, then the PRBS/DM output will be forced to source an inverted RCLK. See Figures 1F and 1G. When the transmitter is disabled (TTS* = 0), the driver monitor is also disabled.

T3 Transmit Waveform Template Table 1C

Time Axis Range	**Normalized Amplitude Equations**
Upper Curve	
$-0.85 \le T \le -0.68$	0.03
$-0.68 \le T \le 0.36$	$0.5 \{1 + \sin[(\pi/2)(1 + T/0.34)]\} + 0.03$
$0.36 \le T \le 1.4$	$0.08 + 0.407e^{-1.84(T - 0.36)}$
Lower Curve	
$-0.85 \le T \le -0.36$	-0.03
$-0.36 \le T \le 0.36$	$0.5 \{1 + \sin[(\pi/2)(1 + T/0.18)]\} - 0.03$
$0.36 \le T \le 1.4$	-0.03

Governing Specifications: ANSI T1.102-1993 and Bellcore GR-499.

T3 Transmit Waveform Test Parameters and Limits Table 1D

Parameter	Specification
Rate	44.736Mbit/s (± 20 ppm)
Line code	B3ZS
Transmission medium	COAX cable (AT&T 734A or equivalent)
Test measurement point	At the end of 0 to 450 feet of COAX cable
Test termination	75 ohms (± 1%) resistive
Pulse amplitude	Between 0.36V and 0.85V
Pulse shape	An isolated pulse (preceded by two zeros and followed by one or more zeros) falls within the curved listed in Table 1C
Unframed All Ones Power level @ 22.368MHz	Between –1.8dBm and +5.7dBm
Unframed All Ones Power level @ 44.736MHz	At least 20dB less than the power measured at 22.368MHz
Pulse imbalance of isolated pulses	Ratio of positive and negative pulses must be between 0.90 and 1.10

STS-1 Transmit Waveform Template Table 1E

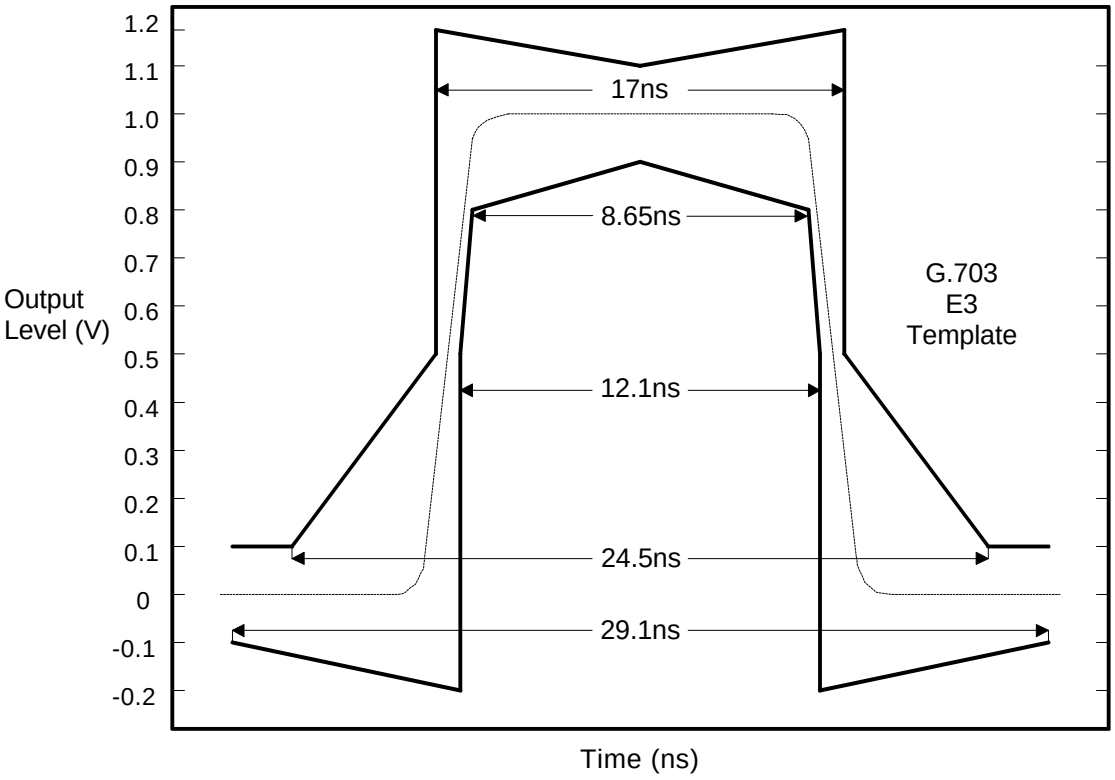
Time Axis Range	Normalized Amplitude Equations
Upper Curve	
$-0.85 \le T \le -0.68$	0.03
$-0.68 \le T \le 0.26$	$0.5 \{1 + \sin[(\pi/2)(1 + T/0.34)]\} + 0.03$
$0.26 \le T \le 1.4$	$0.1 + 0.61e^{-2.4(T - 0.26)}$
Lower Curve	
$-0.85 \le T \le -0.36$	-0.03
$-0.36 \le T \le 0.36$	$0.5 \{1 + \sin[(\pi/2)(1 + T/0.18)]\} - 0.03$
$0.36 \le T \le 1.4$	-0.03

Governing Specifications: Bellcore GR-253 and Bellcore GR-499.

STS-1 Transmit Waveform Test Parameters and Limits Table 1F

Parameter	Specification
Rate	51.840Mbit/s (± 20 ppm)
Line code	B3ZS
Transmission medium	COAX cable (AT&T 734A or equivalent)
Test measurement point	At the end of 0 to 450 feet of COAX cable
Test termination	75 ohms (± 1%) resistive
Pulse shape	An isolated pulse (preceded by two zeros and followed by one or more zeros) falls within the curved listed in Table 1E
Unframed All Ones Power level @ 25.92MHz	Between –1.8dBm and +5.7dBm
Unframed All Ones Power level @ 51.84MHz	At least 20dB less than the power measured at 25.92MHz

E3 Transmit Waveform Template Figure 1D



E3 Transmit Waveform Test Parameters and Limits Table 1G

Parameter	Specification
Rate	34.368Mbit/s (± 20 ppm)
Line code	HDB3
Transmission medium	COAX cable (AT&T 734A or equivalent)
Test measurement point	At the transmitter
Test termination	75 ohms (± 1%) resistive
Pulse amplitude	1.0V (nominal)
Pulse shape	An isolated pulse (preceded by two zeros and followed by one or more zeros) falls within the template shown in Figure 1D
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05

T3 AIS Structure Figure 1E

M1 Subframe

X1 (1)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

M2 Subframe

X2 (1)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

M3 Subframe

P1 (0)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

M4 Subframe

P2 (0)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

M5 Subframe

M1 (0)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

M6 Subframe

M2 (1)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

M7 Subframe

M3 (0)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

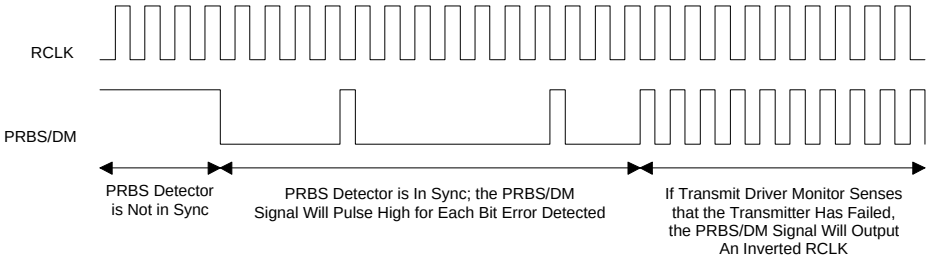
Notes:
1. X1 is transmitted first.
2. The 84 Info Bits are the sequence 101010… where the one (“1”) starts after each X, P, F, C, or M bit.

Diagnostics

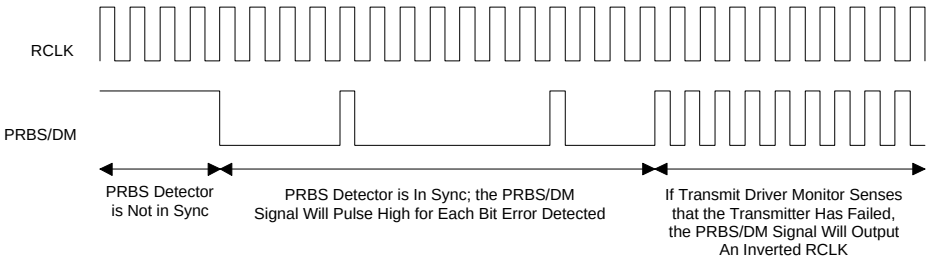
The DS3150 contains an onboard Pseudo Random Binary Sequence (PRBS) generator and detector. This function is useful in testing the device at the physical layer. It will generate and detect either a $2^{15} - 1$ (T1 or STS-1) or $2^{23} - 1$ PRBS according to the ITU O.151 specification. The PRBS pattern generated and detected by the DS3150 is an unframed pattern. In other words, no T3, E3, or STS-1 framing patterns are inserted in the transmit data stream nor expected in the received data stream. The PRBS generator is enabled via the TDS0 and TDS1 inputs. See Tables 2A and 2B for details. The PRBS detector is always enabled and will report it's status via the PRBS/DM output. When the PRBS detector is out of synchronization, the PRBS/DM output will be forced high. When the PRBS detector synchronizes to the incoming pseudorandom pattern, the PRBS/DM output will go low and then pulse high for each bit detected in error. The status of the PRBS detector is overridden when the transmitter driver monitor detects a faulty transmitter. When this occurs, the PRBS/DM will source an inverted RCLK regardless of the current state of the PRBS detector. See Figures 1F and 1G. On the receive side, the recovered data is B3ZS/HDB3 decoded before it is routed to the PRBS decoder.

The DS3150 also has two internal loopbacks that can be used for testing. See Figure 1A. The Analog Loopback loops the outgoing transmit waveform back to the receiver. When this loopback is enabled, data will be transmitted as it normally would be and the incoming data at RX+ and RX- is ignored. The Remote Loopback loops data from the receive side to the transmit side. When this loopback is enabled, data will continue to pass through the receive side as it normally would and data at the TPOS and TNEG inputs is ignored. These two loopbacks are invoked via the LBKS* input. See Table 2A.

PRBS/DM Output With Normal RCLK Operation (ICE = 0 or 1) Figure 1F



PRBS/DM Output With Inverted RCLK Operation (ICE = Float) Figure 1G



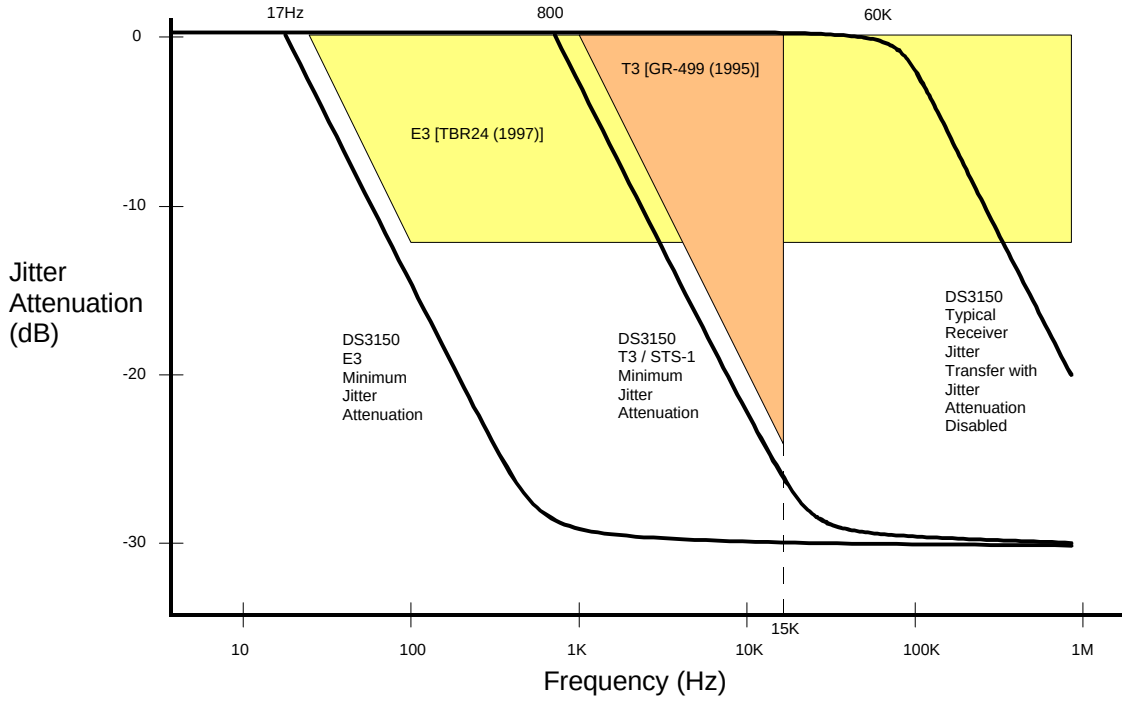
Jitter Attenuator

The DS3150 contains an onboard jitter attenuator that can be placed in either the receive path or the transmit path or disabled. This selection is made via the RMON and TTS* input signals. See Table 1H below for details. Figure 1H shows the minimum jitter attenuation for the device when the jitter attenuator is enabled. Figure 1H also shows the receive jitter transfer when the jitter attenuator is disabled. Depending on whether the device is in the T3/STS-1 or E3 mode, the jitter attenuation will be adjusted.

RMON & TTS* Signal Decode Table 1H

RMON	TTS*	Receive 20dB Flat Gain	Transmit Line Driver	Jitter Attenuator
0	0	disabled	tri-stated	disabled
0	1	disabled	enabled	disabled
0	Float	disabled	enabled	enabled in TX path
1	0	enabled	tri-stated	disabled
1	1	enabled	enabled	disabled
1	Float	enabled	enabled	enabled in TX path
Float	0	disabled	tri-stated	enabled in RX path
Float	1	disabled	enabled	enabled in RX path
Float	Float	disabled	enabled	enabled in RX path

DS3150 Jitter Attenuation / Jitter Transfer Figure 1H



SECTION 2: SIGNAL DESCRIPTION

Table 2A below lists all of the signals on the DS3150 and their function. The signals are listed in order by their pin number.

Signal Descriptions Table 2A

Pin	Signal Name	I/O	Description
1	RX+	I	**Receive Analog Input.** This analog input is coupled to the T3, STS-1, or E3 75 Ω COAX line via a 1:2 step-up transformer. See Figure 1B for details.
2	EFE	I3	**Enhanced Feature & Test Mode Enable.** This signal selects whether the enhanced features (ability to transmit all ones, T3 AIS, or a 1010… pattern and PRBS generation/detection and the transmit driver monitor) are enabled or not. **0 = Enhanced Features Disabled:** pins 4 & 5 are ignored and pin 12 is tri-stated. **1 = Enhanced Features Enabled:** pins 4 & 5 are active and defined as TDS0 & TDS1 respectively and pin 12 is active and defined as PRBS/DM. **FLOAT = Test Mode Enabled:** pins 4, 5, 12 & 27 are redefined as test pins.
3	RX-	I	**Receive Analog Input.** This analog input is coupled to the T3, STS-1, or E3 75 Ω COAX line via a 1:2 step-up transformer. See Figure 1B for details.
4	TDS0	I	**Transmit Data Select Bit 0.** This signal selects the source of the transmit data. See Table 2B. If EFE is set low, then this signal is ignored.
5	TDS1	I	**Transmit Data Select Bit 1.** This signal selects the source of the transmit data. See Table 2B. If EFE is set low, then this signal is ignored.
6	VSS	-	**Ground Reference.** All VSS signals should be tied together.
7	VDD	-	**Positive Supply.** 3.3V ± 5%. All VDD signals should be tied together.
8	VSS	-	**Ground Reference.** All VSS signals should be tied together.
9	TX+	O3	**Transmit Analog Output.** This analog output drives the T3, STS-1, or E3 signal into the 75 Ω COAX line. This signal is connected via a 2:1 step-down transformer to the COAX line. See Section 1 for details. This output can be tri-stated via the TTS* input signal.
10	ICE	I3	**Invert Clock Enable.** This signal determines on which RCLK edge RPOS/RNEG is updated and which TCLK edge TPOS/TNEG is sampled. **0 = Normal RCLK / Normal TCLK:** update RPOS/RNEG on falling edge of RCLK and sample TPOS/TNEG on rising edge of TCLK **1 = Normal RCLK / Inverted TCLK:** update RPOS/RNEG on falling edge of RCLK and sample TPOS/TNEG on falling edge of TCLK **FLOAT = Inverted RCLK / Inverted TCLK:** update RPOS/RNEG on rising edge of RCLK and sample TPOS/TNEG on falling edge of TCLK
11	TX-	O3	**Transmit Analog Output.** This analog output drives the T3, STS-1, or E3 signal into the 75 Ω COAX line. This signal is connected via a 2:1 step-down transformer to the COAX line. See Section 1 for details. This output can be tri-stated via the TTS* input signal.
12	PRBS/ DM	O3	**PRBS Detector and Transmit Driver Monitor Output.** This signal reports the status of the PRBS detector and the Transmit Driver Monitor. The PRBS detector will constantly search for either a $2^{15} - 1$ (T3 or STS-1) or $2^{23} - 1$ pseudo random pattern. This signal will remain high when the PRBS detector is out of synchronization. When the PRBS detector synchronizes to the pseudo random pattern, then this signal will go low and will create a positive going pulse (synchronous with RCLK) for each bit error detected. If the transmit driver monitor detects a faulty transmitter, then the PRBS detector output will be overridden and this output will source an inverted RCLK. See Figures 1F and 1G for more details. If EFE is set low, then this signal is tri-stated.
13	TESS	I3	**T3 / E3 / STS-1 Select.** This input determines the mode of operation for the device. **0 = E3** **1 = T3** **FLOAT = STS-1**

Pin	Signal Name	I/O	Description
14	TPOS/ TNRZ	I	**Transmit Positive Data.** If a bipolar data stream is to be transmitted, then the B3ZS/HDB3 encoder/decoder should be disabled (ZCSE* = 1) and the positive half of the bipolar data stream should be applied to TPOS and the negative half to TNEG. If a NRZ data stream is to be transmitted, then the B3ZS/HDB3 encoder/decoder should be enabled (ZCSE* = 0) and the NRZ data stream should be applied to TPOS, TNEG is ignored and can be tied either high or low. TPOS is sampled either on the falling edge of TCLK (ICE = 1 or FLOAT) or the rising edge of TCLK (ICE = 0).
15	TNEG	I	**Transmit Negative Data.** If a bipolar data stream is to be transmitted, then the B3ZS/HDB3 encoder/decoder should be disabled (ZCSE* = 1) and the positive half of the bipolar data stream should be applied to TPOS and the negative half to TNEG. If a NRZ data stream is to be transmitted, then the B3ZS/HDB3 encoder/decoder should be enabled (ZCSE* = 0) and the NRZ data stream should be applied to TPOS, TNEG is ignored and can be tied either high or low. TNEG is sampled either on the falling edge of TCLK (ICE = 1 or FLOAT) or the rising edge of TCLK (ICE = 0).
16	TCLK	I	**Transmit Clock.** Either a T3 (44.736MHz ± 20ppm), E3 (34.368MHz ± 20ppm), or STS-1 (51.84 ± 20ppm) clock should be applied at this signal. Data to be transmitted will be clocked into the device at TPOS & TNEG either on a rising edge of TCLK (ICE = 0) or falling edge of TCLK (ICE = 1 or FLOAT). The duty cycle on TCLK is not restricted as long it meets the high and low times listed in Section 3.
17	VDD	-	**Positive Supply.** 3.3V ± 5%. All VDD signals should be tied together.
18	TTS*	I3	**Transmit Tri-State Output Driver.** This input determines whether the TX+ and TX- analog output signals are forced into tri-state or are active. This input also controls the jitter attenuator. See Table 2C. **0 = tri-state the transmit output driver & disable TX jitter attenuation** **1 = enable transmit driver & disable TX jitter attenuation** **FLOAT = enable the transmit driver & enable TX jitter attenuation**
19	MCLK	I	**Master Clock.** The clock input at this signal is used by the clock and data recovery machine. Either a T3 (44.736MHz ± 20ppm), E3 (34.368MHz ± 20ppm), or STS-1 (51.84 ± 20ppm) clock should be applied at this signal. Tying this pin low forces the device to use the clock applied at the TCLK input for the receive side clock and data recovery.
20	ZCSE*	I	**Zero Code Suppression Enable.** **0 = B3ZS/HDB3 encoder/decoder enabled** (NRZ interface enabled) **1 = B3ZS/HDB3 encoder/decoder disabled** (NRZ interface disabled)
21	RMON	I3	**Receive Monitor Mode.** This input determines whether or not a 20db flat gain will be applied to the incoming signal before it is feed to the receive equalizer. This mode is invoked when the device is being used to monitor signals that have been resistively attenuated by a monitor jack. In this mode, the maximum input signal allowed at RX+ and RX- is reduced by 20dB. This input also controls the jitter attenuator. See Table 2C. **0 = disable the 20dB gain & disable RX jitter attenuation** **1 = enable the 20dB gain & disable RX jitter attenuation** **FLOAT = disable the 20dB gain & enable RX jitter attenuation**
22	VSS	-	**Ground Reference.** All VSS signals should be tied together.
23	RCLK	O	**Receive Clock.** The recovered clock is output at the signal. When the experiences a Loss Of Signal (LOS = 0), the clock applied at MCLK (or TCLK if MCLK is tied low) appears at this signal. The recovered data is updated at the RPOS & RNEG outputs on either the falling edge of RCLK (ICE = 0 or 1) or the rising edge of RCLK (ICE = FLOAT).
24	RNEG	O	**Receive Negative Data.** When the B3ZS/HBD3 encoder/decoder is disabled (ZCSE* = 1), this signal will contain the negative half of the recovered bipolar data steam. When the B3ZS/HDB3 encoder/decoder is enabled (ZCSE* = 0), this signal will be forced low and the NRZ data stream will be output at RPOS. This signal will be updated either on the rising edge of RCLK (ICE = FLOAT) or the falling edge of RCLK (ICE = 0 or 1) with the recovered data stream.

Pin	Signal Name	I/O	Description
25	RPOS/ RNRZ	O	**Receive Positive or NRZ Data.** When the B3ZS/HBD3 encoder/decoder is disabled (ZCSE* = 1), this signal will contain the positive half of the recovered bipolar data steam. When the B3ZS/HDB3 encoder/decoder is enabled (ZCSE* = 0), this signal will contain the recovered NRZ data stream. This signal will be updated either on the rising edge of RCLK (ICE = FLOAT) or the falling edge of RCLK (ICE = 0 or 1) with the recovered data stream.
26	VDD	-	**Positive Supply.** 3.3V ± 5%. All VDD signals should be tied together.
27	LOS*	O	**Loss Of Signal.** Loss Of Signal (LOS) is an active low signal. It will be asserted upon detection of 192 consecutive zeros. Signals lower than 21db below nominal are squelched. LOS is cleared when there are no Excessive Zero occurrences over a span of 192 clock periods. An Excessive Zero occurrence is defined as 3 or more consecutive zeros in the T3 & STS-1 modes and 4 or more zeros in the E3 mode. Governing Specifications are ANSI T1.231 and ITU G.775.
28	LBKS*	I3	**Loopback Select.** This input determines if either the Analog Loopback or the Remote Loopback is enabled. See the Block Diagram in Section 1 for details. **0 = Analog Loopback Enabled** **1 = No Loopback Enabled** **FLOAT = Remote Loopback Enabled**

Notes:
1. I3 is an input capable of detecting 3 states, high, low and float.
2. O3 is an output that is tri-state capable.
3. Symbols appended with an asterisks (*) are active low signals.

Transmit Data Mode Select Pin Descriptions Table 2B

TDS1	TDS0	TESS	Transmit Mode Selected
0	0	X	Transmit data normally as input at TPOS and TNEG
0	1	X	Transmit Unframed All Ones
1	0	E3 or STS-1	Transmit an Unframed 101010… pattern
1	0	T3	Transmit T3 AIS as per ANSI T1.107 (see Figure 1C)
1	1	E3	Transmit a 2^{23} – 1 PRBS pattern as per ITU O.151
1	1	T3 or STS-1	Transmit a 2^{15} – 1 PRBS pattern as per ITU O.151

Notes:
1. TESS = 0 for E3 / TESS = 1 for T3 / TESS = float for STS-1
2. TDS0 & TDS0 are ignored when EFE is tied low and the device will transmit data as input at TPOS & TNEG

RMON & TTS* Signal Decode Table 2C

RMON	TTS*	Receive 20dB Flat Gain	Transmit Line Driver	Jitter Attenuator
0	0	disabled	tri-stated	disabled
0	1	disabled	enabled	disabled
0	Float	disabled	enabled	enabled in TX path
1	0	enabled	tri-stated	disabled
1	1	enabled	enabled	disabled
1	Float	enabled	enabled	enabled in TX path
Float	0	disabled	tri-stated	enabled in RX path
Float	1	disabled	enabled	enabled in RX path
Float	Float	disabled	enabled	enabled in RX path

SECTION 3: AC CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Lead with Respect to VSS (except VDD)	-0.3V to 5.5V
Supply Voltage (VDD) with Respect to VSS	-0.3V to 3.63V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Note: the typical values listed below are not production tested.

RECOMMEND DC OPERATING CONDITIONS (-40°C to +85°C)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Logic 1	VIH	2.4		5.5	V	
Logic 0	VIL	-0.3		0.8	V	
Supply (VDD)	VDD	3.165		3.465	V	

DC CHARACTERISTICS (-40°C to +85°C; VDD = 3.135V to 3.465V)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Supply Current @ VDD = 3.465V	IDD		TBD		mA	1
Power Down Current @ VDD = 3.465V	IPD		TBD		mA	2
Lead Capacitance	CIO		7		pF	
Input Leakage	IIL	-10		+10	uA	3
Input Leakage (w/ pull-ups or float)	IILP	-500		+500	uA	3
Output Leakage	ILO	-10		+10	uA	4
Output Current (2.4V)	IOH	-4.0			mA	
Output Current (0.4V)	IOL	+4.0			mA	

Notes:
1. TCLK = MCLK = 44.736MHz & TX+ and TX- driving all ones into a 75 ohm load / other inputs at VDD or grounded / other outputs left open circuited
2. MCLK = 44.736MHz & TTS* = 0 / other inputs at VDD or grounded / other outputs left open circuited
3. 0V < Vin < VDD
4. Outputs in Tri-State

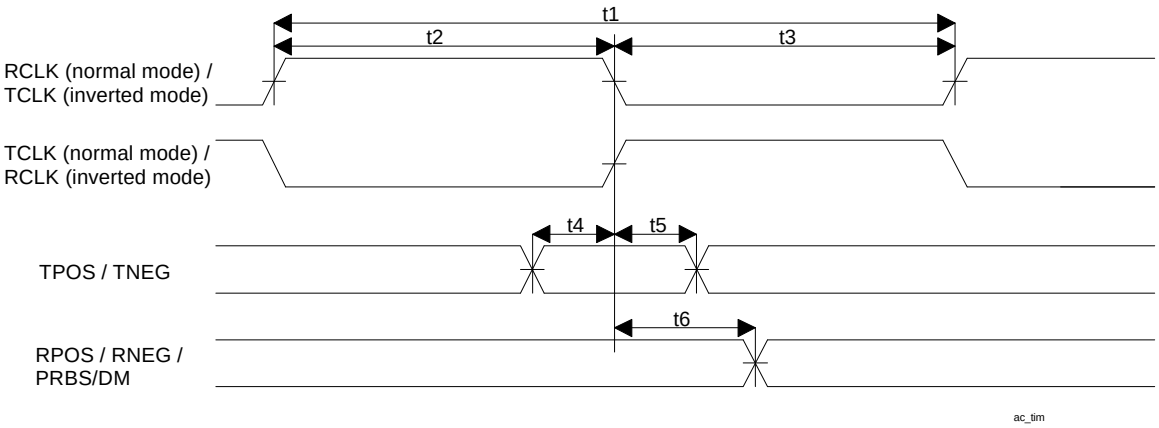
AC CHARACTERISTICS – Digital

(-40°C to +85°C; VDD = 3.135V to 3.465V)

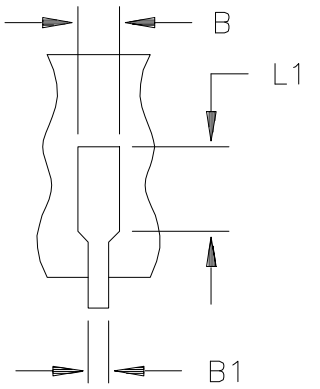
Parameter	Symbol	Min	Typ	Max	Units	Notes
RCLK / TCLK Clock Period	t1		22.4		ns	1
	t1		29.1		ns	2
	t1		19.3		ns	3
RCLK Clock High / Low Time	t2 / t3	9.0	11.2	13.4	ns	1
	t2 / t3	11.6	14.5	17.4	ns	2
	t2 / t3	7.7	9.6	11.5	ns	3
TCLK Clock High / Low Time	t2 / t3	7			ns	
TPOS or TNEG Set Up Time to the Falling Edge or Rising Edge of TCLK	t4	2			ns	
TPOS or TNEG Hold Time from the Falling Edge or Rising Edge of TCLK	t5	2			ns	
Delay from the Rising Edge or Falling Edge of RCLK to Data Valid on RPOS or RNEG or Signal Change on PRBS/DM	t6	2		6	ns	4,5

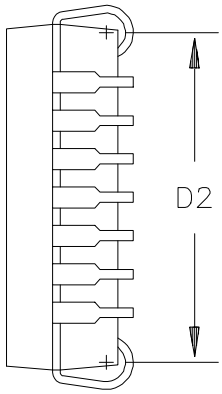
Notes:
1. T3 Mode
2. E3 Mode
3. STS-1 Mode
4. In Normal Mode, TPOS and TNEG are sampled on the rising edge of TCLK and RPOS and RNEG are updated on the falling edge of RCLK
5. In Inverted Mode, TPOS and TNEG are sampled on the falling edge of TCLK and RPOS and RNEG are updated on the rising edge of RCLK

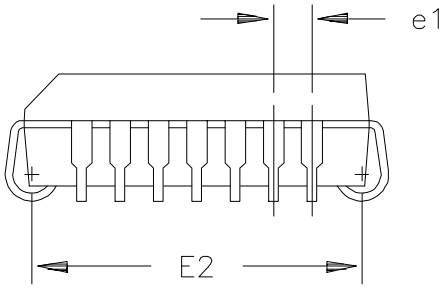
AC TIMING DIAGRAM Figure 3A

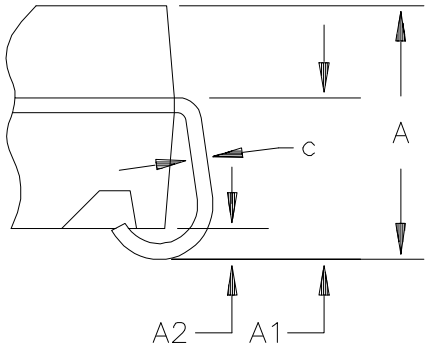


SECTION 4: MECHANICAL DIMENSIONS

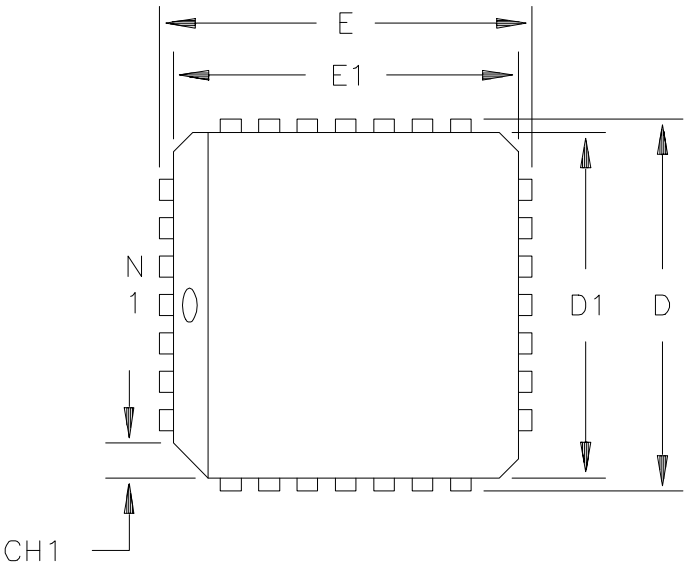






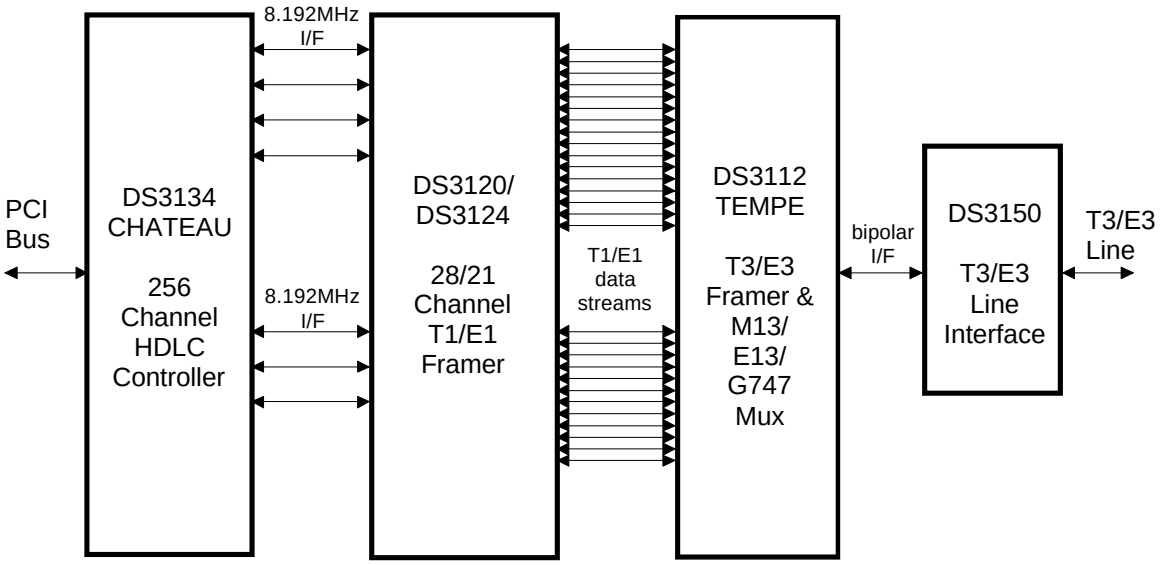


LTR	MIN	MAX
A	.165	.180
A1	.090	.120
A2	.020	–
B	.026	.033
B1	.013	.021
c	.009	.012
D	.485	.495
D1	.450	.456
D2	.390	.430
E	.485	.495
E1	.450	.456
E2	.390	.430
L1	.060	–
N	28	–
e1	.050 BSC	
CH1	.042	.048



SECTION 5: APPLICATIONS

Channelized T3/E3 Application Figure 5A



Dual Unchannelized T3/E3 Application Figure 5B