

## 74VCX163245

### Low Voltage 16-Bit Dual Supply Translating Transceiver with 3-STATE Outputs

#### General Description

The VCX163245 is a dual supply, 16-bit translating transceiver that is designed for 2 way asynchronous communication between busses at different supply voltages by providing true signal translation. The supply rails consist of  $V_{CCA}$ , which is a higher potential rail operating at 2.3V to 3.6V and  $V_{CCB}$ , which is the lower potential rail operating at 1.65V to 2.7V. ( $V_{CCB}$  must be less than or equal to  $V_{CCA}$  for proper device operation). This dual supply design allows for translation from 1.8V to 2.5V busses to busses at a higher potential, up to 3.3V.

The Transmit/Receive ( $T/\bar{R}$ ) input determines the direction of data flow. Transmit (active-HIGH) enables data from A Ports to B Ports; Receive (active-LOW) enables data from B Ports to A Ports. The Output Enable ( $\overline{OE}$ ) input, when HIGH, disables both A and B Ports by placing them in a High-Z condition. The A Port interfaces with the higher voltage bus (2.7V to 3.3V); The B Port interfaces with the lower voltage bus (1.8V to 2.5V). Also the VCX163245 is designed so that the control pins ( $T/\bar{R}_n$ ,  $\overline{OE}_n$ ) are supplied by  $V_{CCB}$ .

The 74VCX163245 is suitable for mixed voltage applications such as notebook computers using a 1.8V CPU and 3.3V peripheral components. It is fabricated with an Advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

#### Features

- Bidirectional interface between busses ranging from 1.65V to 3.6V
- Supports Live Insertion and Withdrawal (Note 1)
- Static Drive ( $I_{OH}/I_{OL}$ )
  - ±24 mA @ 3.0V  $V_{CC}$
  - ±18 mA @ 2.3V  $V_{CC}$
  - ±6 mA @ 1.65V  $V_{CC}$
- Uses patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 16245
- Latchup performance exceeds 300 mA
- ESD performance:
  - Human Body Model >2000V
  - Machine model >200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

**Note 1:** To ensure the high impedance state during power up or power down,  $\overline{OE}_n$  should be tied to  $V_{CCB}$  through a pull up resistor. The minimum value of the resistor is determined by the current sourcing capability of the driver.

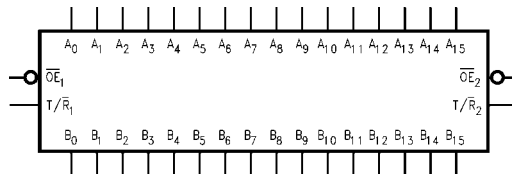
#### Ordering Code:

Order Number	Package Number	Package Description
74VCX163245GX (Note 2)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [Tape and Reel]
74VCX163245MTD (Note 3)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

**Note 2:** BGA package available in Tape and Reel only.

**Note 3:** Device also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

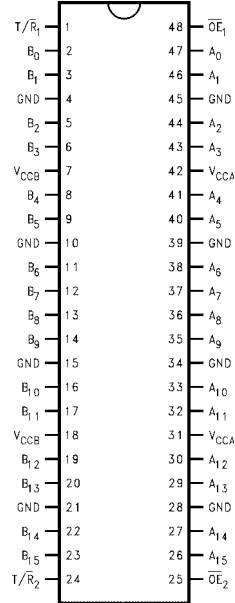
#### Logic Diagram



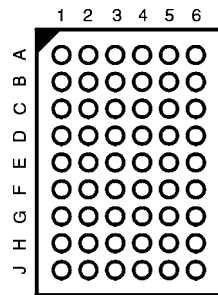
Quiet Series™ is a trademark of Fairchild Semiconductor Corporation.

### Connection Diagrams

Pin Assignment for TSSOP



Pin Assignment for FBGA



(Top Thru View)

### Pin Descriptions

Pin Names	Description
OE <sub>n</sub>	Output Enable Input (Active LOW)
T/R <sub>n</sub>	Transmit/Receive Input
A <sub>0</sub> -A <sub>15</sub>	Side A Inputs or 3-STATE Outputs
B <sub>0</sub> -B <sub>15</sub>	Side B Inputs or 3-STATE Outputs
NC	No Connect

### FBGA Pin Assignments

	1	2	3	4	5	6
<b>A</b>	B <sub>0</sub>	NC	T/R <sub>1</sub>	OE <sub>1</sub>	NC	A <sub>0</sub>
<b>B</b>	B <sub>2</sub>	B <sub>1</sub>	NC	NC	A <sub>1</sub>	A <sub>2</sub>
<b>C</b>	B <sub>4</sub>	B <sub>3</sub>	V <sub>CCB</sub>	V <sub>CCA</sub>	A <sub>3</sub>	A <sub>4</sub>
<b>D</b>	B <sub>6</sub>	B <sub>5</sub>	GND	GND	A <sub>5</sub>	A <sub>6</sub>
<b>E</b>	B <sub>8</sub>	B <sub>7</sub>	GND	GND	A <sub>7</sub>	A <sub>8</sub>
<b>F</b>	B <sub>10</sub>	B <sub>9</sub>	GND	GND	A <sub>9</sub>	A <sub>10</sub>
<b>G</b>	B <sub>12</sub>	B <sub>11</sub>	V <sub>CCB</sub>	V <sub>CCA</sub>	A <sub>11</sub>	A <sub>12</sub>
<b>H</b>	B <sub>14</sub>	B <sub>13</sub>	NC	NC	A <sub>13</sub>	A <sub>14</sub>
<b>J</b>	B <sub>15</sub>	NC	T/R <sub>2</sub>	OE <sub>2</sub>	NC	A <sub>15</sub>

### Truth Tables

Inputs		Outputs
OE <sub>1</sub>	T/R <sub>1</sub>	
L	L	Bus B <sub>0</sub> -B <sub>7</sub> Data to Bus A <sub>0</sub> -A <sub>7</sub>
L	H	Bus A <sub>0</sub> -A <sub>7</sub> Data to Bus B <sub>0</sub> -B <sub>7</sub>
H	X	HIGH Z State on A <sub>0</sub> -A <sub>7</sub> , B <sub>0</sub> -B <sub>7</sub>

Inputs		Outputs
OE <sub>2</sub>	T/R <sub>2</sub>	
L	L	Bus B <sub>8</sub> -B <sub>15</sub> Data to Bus A <sub>8</sub> -A <sub>15</sub>
L	H	Bus A <sub>8</sub> -A <sub>15</sub> Data to Bus B <sub>8</sub> -B <sub>15</sub>
H	X	HIGH-Z State on A <sub>8</sub> -A <sub>15</sub> , B <sub>8</sub> -B <sub>15</sub>

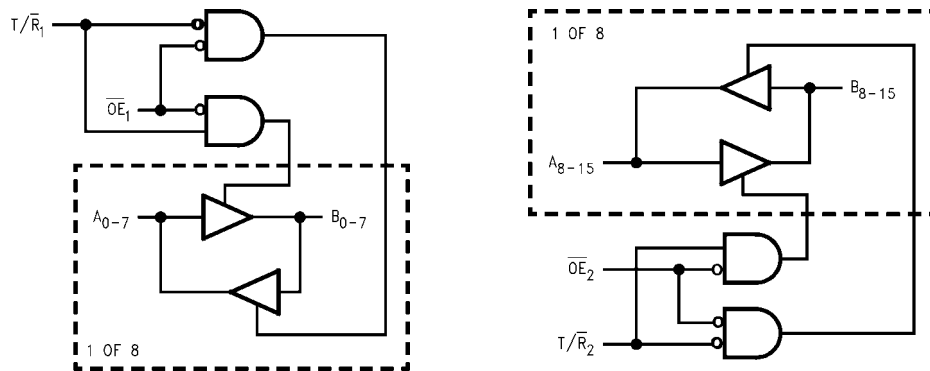
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial (HIGH or LOW, inputs may not float)  
 Z = High Impedance

## VCX163245 Translator Power Up Sequence Recommendations

To guard against power up problems, some simple guidelines need to be adhered to. The VCX163245 is designed so that the control pins ( $\overline{T/R}_n$ ,  $\overline{OE}_n$ ) are supplied by  $V_{CCB}$ . Therefore the first recommendation is to begin by powering up the control side of the device,  $V_{CCB}$ . The  $\overline{OE}_n$  control pins should be ramped with or ahead of  $V_{CCB}$ , this will guard against bus contentions and oscillations as all A Port and B Port outputs will be disabled. To ensure the high impedance state during power up or power down,  $\overline{OE}_n$  should be tied to  $V_{CCB}$  through a pull up resistor. The minimum value of the resistor is determined by the current sourcing capability of the driver. Second, the  $\overline{T/R}_n$  control

pins should be placed at logic LOW (0V) level, this will ensure that the B-side bus pins are configured as inputs to help guard against bus contention and oscillations. B-side Data Inputs should be driven to a valid logic level (0V or  $V_{CCB}$ ), this will prevent excessive current draw and oscillations.  $V_{CCA}$  can then be powered up after  $V_{CCB}$ , however  $V_{CCA}$  must be greater than or equal to  $V_{CCB}$  to ensure proper device operation. Upon completion of these steps the device can then be configured for the users desired operation. Following these steps will help to prevent possible damage to the translator device as well as other system components.

### Logic Diagrams



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 4)		Recommended Operating Conditions (Note 6)	
Supply Voltage			
$V_{CCA}$	-0.5V to +4.6V	Power Supply (Note 7)	
$V_{CCB}$	-0.5V to $V_{CCA}$	$V_{CCA}$	2.3V to 3.6V
DC Input Voltage ( $V_I$ )	-0.5V to +4.6V	$V_{CCB}$	1.65V to 2.7V
DC Output Voltage ( $V_{I/O}$ )		Input Voltage ( $V_I$ ) @ $\overline{OE}$ , $T/\overline{R}$	0V to $V_{CCB}$
Outputs 3-STATE	-0.5V to +4.6V	Input/Output Voltage ( $V_{I/O}$ )	
Outputs Active (Note 5)		$A_n$	0V to $V_{CCA}$
$A_n$	-0.5V to $V_{CCA} + 0.5V$	$B_n$	0V to $V_{CCB}$
$B_n$	-0.5V to $V_{CCB} + 0.5V$	Output Current in $I_{OH}/I_{OL}$	
DC Input Diode Current ( $I_{IK}$ )		$V_{CCA} = 3.0V$ to 3.6V	$\pm 24$ mA
$V_I < 0V$	-50 mA	$V_{CCA} = 2.3V$ to 2.7V	$\pm 18$ mA
DC Output Diode Current ( $I_{OK}$ )		$V_{CCB} = 2.3V$ to 2.7V	$\pm 18$ mA
$V_O < 0V$	-50 mA	$V_{CCB} = 1.65V$ to 1.95V	$\pm 6$ mA
$V_O > V_{CC}$	+50 mA	Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA	Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	
DC $V_{CC}$ or Ground Current	$\pm 100$ mA	$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V
Supply Pin ( $I_{CC}$ or Ground)		<b>Note 4:</b> The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.	
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C	<b>Note 5:</b> $I_O$ Absolute Maximum Rating must be observed.	
		<b>Note 6:</b> Unused inputs or I/O pins must be held HIGH or LOW. They may not float.	
		<b>Note 7:</b> Operation requires: $V_{CCB} \leq V_{CCA}$	

### DC Electrical Characteristics (1.65V < $V_{CCB} \leq 1.95V$ , 2.3V < $V_{CCA} \leq 2.7V$ )

Symbol	Parameter	Conditions	$V_{CCB}$ (V)	$V_{CCA}$ (V)	Min	Max	Units
$V_{IHA}$	HIGH Level Input Voltage	$A_n$	1.65-1.95	2.3-2.7	1.6		V
$V_{IHB}$		$B_n$ , $T/\overline{R}$ , $\overline{OE}$	1.65-1.95	2.3-2.7	$0.65 \times V_{CCB}$		V
$V_{ILA}$	LOW Level Input Voltage	$A_n$	1.65-1.95	2.3-2.7		0.7	V
$V_{ILB}$		$B_n$ , $T/\overline{R}$ , $\overline{OE}$	1.65-1.95	2.3-2.7		$0.35 \times V_{CCB}$	V
$V_{OHA}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$ $I_{OH} = -18 \text{ mA}$	1.65-1.95 1.65	2.3-2.7 2.3-2.7	$V_{CCA} - 0.2$ 1.7		V
$V_{OHB}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$ $I_{OH} = -6 \text{ mA}$	1.65-1.95 1.65-1.95	2.3-2.7 2.3	$V_{CCB} - 0.2$ 1.25		V
$V_{OLA}$	Low Level Output Voltage	$I_{OL} = 100 \mu A$ $I_{OL} = 18 \text{ mA}$	1.65-1.95 1.65	2.3-2.7 2.3-2.7		0.2 0.6	V
$V_{OLB}$	Low Level Output Voltage	$I_{OL} = 100 \mu A$ $I_{OL} = 6 \text{ mA}$	1.65-1.95 1.65-1.95	2.3-2.7 2.3		0.2 0.3	V
$I_I$	Input Leakage Current @ $\overline{OE}$ , $T/\overline{R}$	$0V \leq V_I \leq 3.6V$	1.65-1.95	2.3-2.7		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0V \leq V_O \leq 3.6V$ $\overline{OE} = V_{CCB}$ $V_I = V_{IH}$ or $V_{IL}$	1.65-1.95	2.3-2.7		$\pm 10$	$\mu A$
$I_{OFF}$	Power Off Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0	0		10	$\mu A$
$I_{CCA}/I_{CCB}$	Quiescent Supply Current, per supply, $V_{CCA}/V_{CCB}$	$A_n = V_{CCA}$ or GND $B_n$ , $\overline{OE}$ , & $T/\overline{R} = V_{CCB}$ or GND	1.65-1.95	2.3-2.7		20	$\mu A$
		$V_{CCA} \leq A_n \leq 3.6V$ $V_{CCB} \leq B_n$ , $\overline{OE}$ , $T/\overline{R} \leq 3.6V$	1.65-1.95	2.3-2.7		$\pm 20$	$\mu A$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input, $B_n$ , $T/\overline{R}$ , $\overline{OE}$	$V_I = V_{CCB} - 0.6V$	1.65-1.95	2.3-2.7		750	$\mu A$
	Increase in $I_{CC}$ per Input, $A_n$	$V_I = V_{CCA} - 0.6V$	1.65-1.95	2.3-2.7		750	$\mu A$

DC Electrical Characteristics (1.65V < V <sub>CCB</sub> ≤ 1.95V, 3.0V < V <sub>CCA</sub> ≤ 3.6V)								
Symbol	Parameter		Conditions	V <sub>CCB</sub> (V)	V <sub>CCA</sub> (V)	Min	Max	Units
V <sub>IHA</sub>	HIGH Level Input Voltage	A <sub>n</sub>		1.65–1.95	3.0–3.6	2.0		V
V <sub>IHB</sub>		B <sub>n</sub> , T/R, OE		1.65–1.95	3.0–3.6	0.65 x V <sub>CCB</sub>		V
V <sub>ILA</sub>	LOW Level Input Voltage	A <sub>n</sub>		1.65–1.95	3.0–3.6		0.8	V
V <sub>ILB</sub>		B <sub>n</sub> , T/R, OE		1.65–1.95	3.0–3.6		0.35 x V <sub>CCB</sub>	V
V <sub>OHA</sub>	HIGH Level Output Voltage		I <sub>OH</sub> = –100 μA I <sub>OH</sub> = –24 mA	1.65–1.95 1.65	3.0–3.6 3.0–3.6	V <sub>CCA</sub> –0.2 2.2		V
V <sub>OHB</sub>	HIGH Level Output Voltage		I <sub>OH</sub> = –100 μA I <sub>OH</sub> = –6 mA	1.65–1.95 1.65–1.95	3.0–3.6 3.0	V <sub>CCA</sub> –0.2 1.25		V
V <sub>OLA</sub>	LOW Level Output Voltage		I <sub>OL</sub> = 100 μA I <sub>OL</sub> = 24 mA	1.65–1.95 1.65	3.0–3.6 3.0–3.6		0.2 0.55	V
V <sub>OLB</sub>	LOW Level Output Voltage		I <sub>OL</sub> = 100 μA I <sub>OL</sub> = 6 mA	1.65–1.95 1.65–1.95	3.0–3.6 3.0		0.2 0.3	V
I <sub>I</sub>	Input Leakage Current @ OE, T/R		0V ≤ V <sub>I</sub> ≤ 3.6V	1.65–1.95	3.0–3.6		±5.0	μA
I <sub>OZ</sub>	3-STATE Output Leakage		0V ≤ V <sub>O</sub> ≤ 3.6V OE* = V <sub>CCB</sub> V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	1.65–1.95	3.0–3.6		±10	μA
I <sub>OFF</sub>	Power OFF Leakage Current		0 ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V	0	0		10	μA
I <sub>CCA</sub> /I <sub>CCB</sub>	Quiescent Supply Current, per supply, V <sub>CCA</sub> /V <sub>CCB</sub>		A <sub>n</sub> = V <sub>CCA</sub> or GND B <sub>n</sub> , OE, & T/R = V <sub>CCB</sub> or GND	1.65–1.95	3.0–3.6		20	μA
			V <sub>CCA</sub> ≤ A <sub>n</sub> ≤ 3.6V V <sub>CCB</sub> ≤ B <sub>n</sub> , OE, T/R ≤ 3.6V	1.65–1.95	3.0–3.6		±20	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input, B <sub>n</sub> , T/R, OE		V <sub>I</sub> = V <sub>CCB</sub> – 0.6V	1.65–1.95	3.0–3.6		750	μA
	Increase in I <sub>CC</sub> per Input, A <sub>n</sub>		V <sub>I</sub> = V <sub>CCA</sub> – 0.6V	1.65–1.95	3.0–3.6		750	μA

DC Electrical Characteristics (2.3V < V <sub>CCB</sub> ≤ 2.7V, 3.0V ≤ V <sub>CCA</sub> ≤ 3.6V)								
Symbol	Parameter		Conditions	V <sub>CCB</sub> (V)	V <sub>CCA</sub> (V)	Min	Max	Units
V <sub>IHA</sub>	HIGH Level Input Voltage	A <sub>n</sub>		2.3–2.7	3.0–3.6	2.0		V
V <sub>IHB</sub>		B <sub>n</sub> , T/R, OE		2.3–2.7	3.0–3.6	1.6		V
V <sub>ILA</sub>	LOW Level Input Voltage	A <sub>n</sub>		2.3–2.7	3.0–3.6		0.8	V
V <sub>ILB</sub>		B <sub>n</sub> , T/R, OE		2.3–2.7	3.0–3.6		0.7	V
V <sub>OHA</sub>	HIGH Level Output Voltage		I <sub>OH</sub> = –100 μA I <sub>OH</sub> = –24 mA	2.3–2.7 2.3	3.0–3.6 3.0–3.6	V <sub>CCA</sub> –0.2 2.2		V
V <sub>OHB</sub>	HIGH Level Output Voltage		I <sub>OH</sub> = –100 μA I <sub>OH</sub> = –18 mA	2.3–2.7 2.3–2.7	3.0–3.6 3.0	V <sub>CCB</sub> –0.2 1.7		V
V <sub>OLA</sub>	LOW Level Output Voltage		I <sub>OL</sub> = 100 μA I <sub>OL</sub> = 24 mA	2.3–2.7 2.3	3.0–3.6 3.0–3.6		0.2 0.55	V
V <sub>OLB</sub>	LOW Level Output Voltage		I <sub>OL</sub> = 100 μA I <sub>OL</sub> = 18 mA	2.3–2.7 2.3–2.7	3.0–3.6 3.0		0.2 0.6	V
I <sub>I</sub>	Input Leakage Current @ OE, T/R		0V ≤ V <sub>I</sub> ≤ 3.6V	2.3–2.7	3.0–3.6		±5.0	μA
I <sub>OZ</sub>	3-STATE Output Leakage @ A <sub>n</sub>		0V ≤ V <sub>O</sub> ≤ 3.6V OE = V <sub>CCA</sub> V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.3–2.7	3.0–3.6		±10	μA
I <sub>OFF</sub>	Power OFF Leakage Current		0 ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V	0	0		10	μA
I <sub>CCA</sub> /I <sub>CCB</sub>	Quiescent Supply Current, per supply, V <sub>CCA</sub> /V <sub>CCB</sub>		A <sub>n</sub> = V <sub>CCA</sub> or GND B <sub>n</sub> , OE, & T/R = V <sub>CCB</sub> or GND	2.3–2.7	3.0–3.6		20	μA
			V <sub>CCA</sub> ≤ A <sub>n</sub> ≤ 3.6V V <sub>CCB</sub> ≤ B <sub>n</sub> , OE, T/R ≤ 3.6V	2.3–2.7	3.0–3.6		±20	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input, B <sub>n</sub> , T/R, OE		V <sub>I</sub> = V <sub>CCB</sub> – 0.6V	2.3–2.7	3.0–3.6		750	μA
	Increase in I <sub>CC</sub> per Input, A <sub>n</sub>		V <sub>I</sub> = V <sub>CCA</sub> – 0.6V	2.3–2.7	3.0–3.6		750	μA

## AC Electrical Characteristics

Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}, C_L = 30\text{ pF}, R_L = 500\Omega$						Units
		$V_{CCB} = 1.65\text{V to } 1.95\text{V}$		$V_{CCB} = 1.65\text{V to } 1.95\text{V}$		$V_{CCB} = 2.3\text{V to } 2.7\text{V}$		
		$V_{CCA} = 2.3\text{V to } 2.7\text{V}$		$V_{CCA} = 3.0\text{V to } 3.6\text{V}$		$V_{CCA} = 3.0\text{V to } 3.6\text{V}$		
		Min	Max	Min	Max	Min	Max	
$t_{PHL}, t_{PLH}$	Propagation Delay, A to B	1.5	5.8	1.5	6.2	0.8	4.4	ns
$t_{PHL}, t_{PLH}$	Propagation Delay, B to A	0.8	5.5	0.6	5.1	0.6	4.0	ns
$t_{PZL}, t_{PZH}$	Output Enable Time, OE to B	1.5	8.3	1.5	8.2	0.8	4.6	ns
$t_{PZL}, t_{PZH}$	Output Enable Time, OE to A	0.8	5.3	0.6	5.1	0.6	4.0	ns
$t_{PLZ}, t_{PHZ}$	Output Disable Time, OE to B	0.8	4.6	0.8	4.5	0.8	4.4	ns
$t_{PLZ}, t_{PHZ}$	Output Disable Time, OE to A	0.8	5.2	0.6	5.6	0.6	4.8	ns
$t_{osHL}$ $t_{osLH}$	Output to Output Skew (Note 8)		5.0		0.5		0.75	ns

**Note 8:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{osHL}$ ) or LOW-to-HIGH ( $t_{osLH}$ ).

## Dynamic Switching Characteristics

Symbol	Parameter	Conditions	$V_{CCB}$ (V)	$V_{CCA}$ (V)	$T_A = +25^\circ\text{C}$	Units
					Typical	
$V_{OLP}$	Quiet Output Dynamic Peak $V_{OL}$ , A to B	$C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	1.8	2.5	0.25	V
			1.8	3.3	0.25	
			2.5	3.3	0.6	
$V_{OLP}$	Quiet Output Dynamic Peak $V_{OL}$ , B to A	$C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	1.8	2.5	0.6	V
			1.8	3.3	0.8	
			2.5	3.3	0.8	
$V_{OLV}$	Quiet Output Dynamic Valley $V_{OL}$ , A to B	$C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	1.8	2.5	-0.25	V
			1.8	3.3	-0.25	
			2.5	3.3	-0.6	
$V_{OLV}$	Quiet Output Dynamic Valley $V_{OL}$ , B to A	$C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	1.8	2.5	-0.6	V
			1.8	3.3	-0.8	
			2.5	3.3	-0.8	
$V_{OHV}$	Quiet Output Dynamic Valley $V_{OH}$ , A to B	$C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	1.8	2.5	1.3	V
			1.8	3.3	1.3	
			2.5	3.3	1.7	
$V_{OHV}$	Quiet Output Dynamic Valley $V_{OH}$ , B to A	$C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	1.8	2.5	1.7	V
			1.8	3.3	2.0	
			2.5	3.3	2.0	

## Capacitance

Symbol	Parameter	Conditions	$T_A = +25^\circ\text{C}$	Units
$C_{IN}$	Input Capacitance	$V_{CCB} = 2.5\text{V}, V_{CCA} = 3.3\text{V}, V_I = 0\text{V or } V_{CCA/B}$	5	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CCB} = 2.5\text{V}, V_{CCA} = 3.3\text{V}, V_I = 0\text{V or } V_{CCA/B}$	6	pF
$C_{PD}$	Power Dissipation Capacitance	$V_{CCB} = 2.5\text{V}, V_{CCA} = 3.3\text{V}, V_I = 0\text{V or } V_{CCA/B}$ $f = 10\text{MHz}$	20	pF

## AC Loading and Waveforms

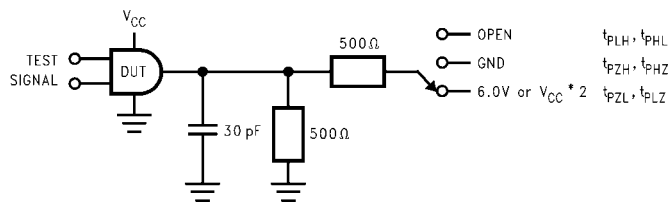


FIGURE 1. AC Test Circuit

TEST	SWITCH
$t_{PLH}, t_{PHL}$	OPEN
$t_{PZL}, t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ ; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V; 1.8V \pm 0.15V$
$t_{PZH}, t_{PHZ}$	GND

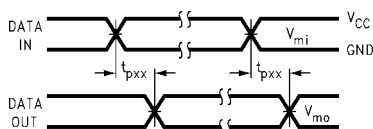


FIGURE 2. Waveform for Inverting and Non-inverting Functions  
 $t_R = t_F \leq 2.0 \text{ ns}, 10\% \text{ to } 90\%$

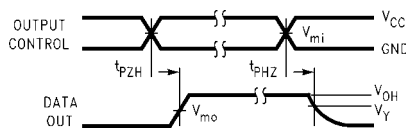


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic  
 $t_R = t_F \leq 2.0 \text{ ns}, 10\% \text{ to } 90\%$

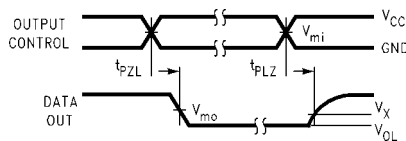
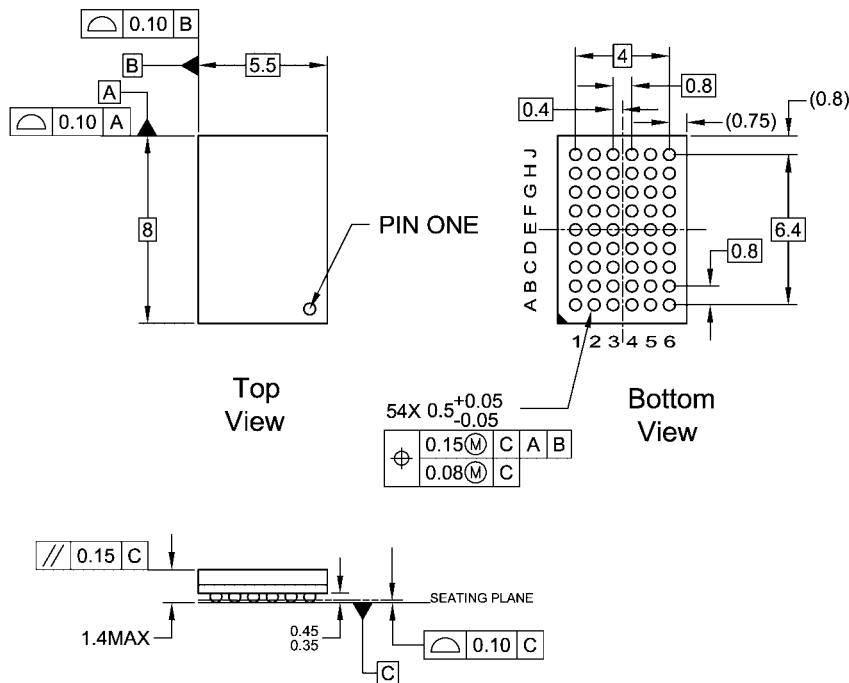


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic  
 $t_R = t_F \leq 2.0 \text{ ns}, 10\% \text{ to } 90\%$

Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	$2.5V \pm 0.2V$	$1.8V \pm 0.15V$
$V_{mi}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
$V_Y$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

**Physical Dimensions** inches (millimeters) unless otherwise noted



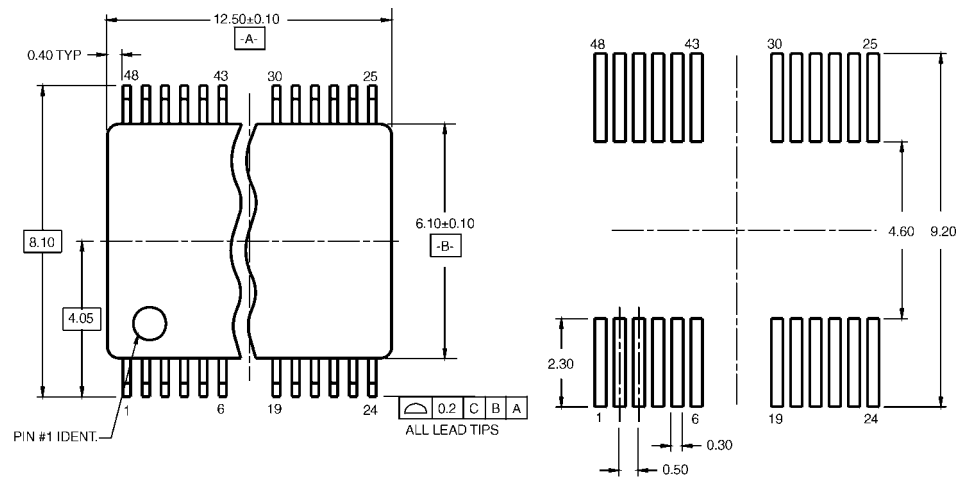
- NOTES:
- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
  - B. ALL DIMENSIONS IN MILLIMETERS
  - C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)  
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
  - D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

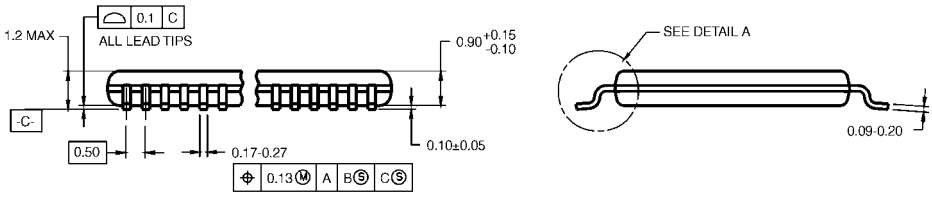
**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC M0-205, 5.5mm Wide  
Package Number BGA54A  
(Preliminary)**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**LAND PATTERN RECOMMENDATION**

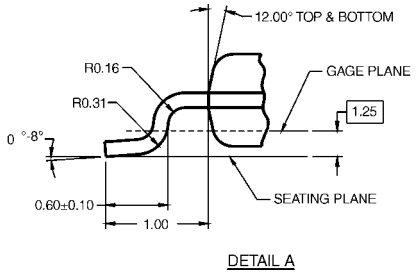


DIMENSIONS ARE IN MILLIMETERS

- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
  - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48**



Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)