



# 74LVXC3245

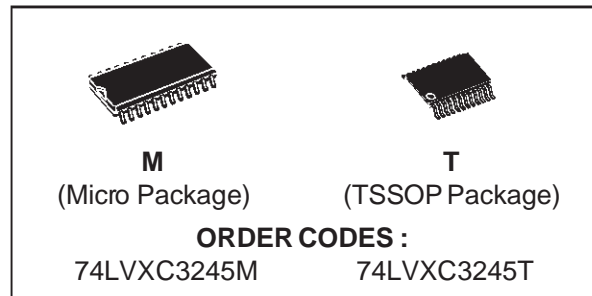
## OCTAL DUAL SUPPLY BUS TRANSCEIVER

PRELIMINARY DATA

- HIGH SPEED:  $t_{PD} = 6 \text{ ns}$  (TYP.) at  $V_{CC} = 3.3\text{V}$
- LOW POWER DISSIPATION:  
 $I_{CC} = 8 \mu\text{A}$  (MAX.) at  $T_A = 25^\circ\text{C}$
- LOW NOISE:  $V_{OLP} = 0.3\text{V}$  (TYP.) at  $V_{CC} = 3.3\text{V}$
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 4 \text{ mA}$  (MIN)
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CCA}$  (OPR) = 2.7V to 3.6V (1.2V Data Retention)
- $V_{CCB}$  (OPR) = 2.7V to 5.5V (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 3245
- IMPROVED LATCH-UP IMMUNITY

### DESCRIPTION

The LVXC3245 is a dual supply 8 bit configurable low voltage CMOS OCTAL BUS TRANSCEIVER fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology. Designed for use as an interface between a 3.3V bus and a 3.3V to 5V bus in mixed 3.3V/5V



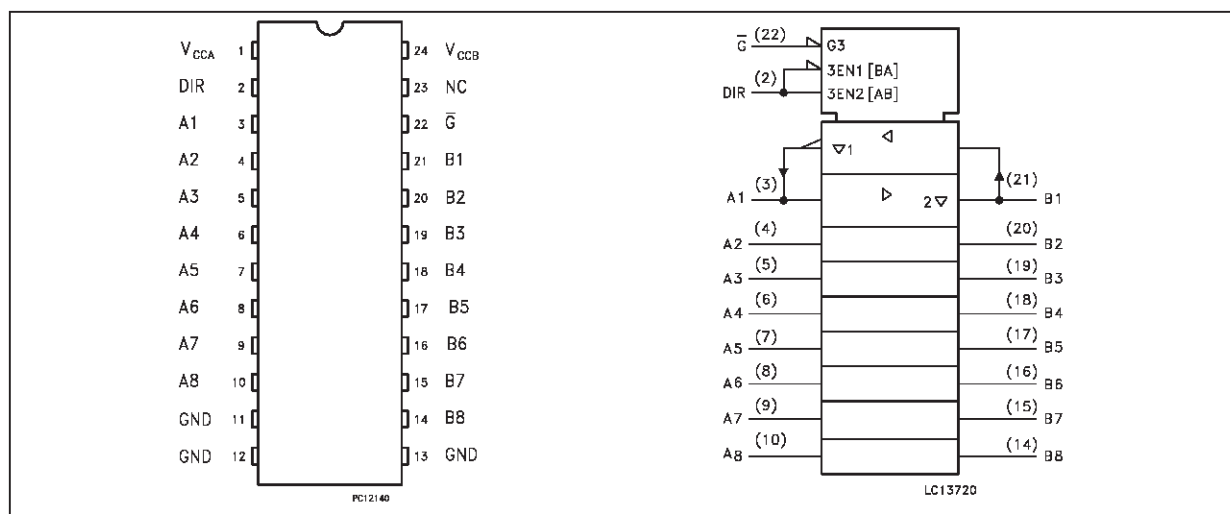
supply systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

This IC is intended for two-way asynchronous communication between data buses; the direction of data transmission is determined by DIR input. The enable input  $\bar{G}$  can be used to disable the device so that the buses are effectively isolated.

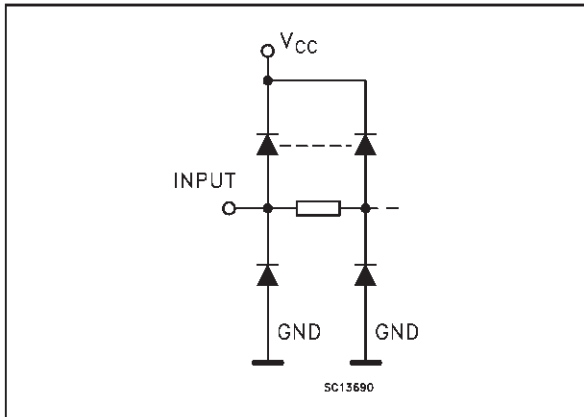
The A-port interfaces with the 5V bus, the B-port with the 3.3V to 5V bus.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess

### PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
2	DIR	Directional Control
3, 4, 5, 6, 7, 8, 9, 10	A1 to A8	Data Inputs/Outputs
21, 20, 19, 18, 17, 16, 15, 14	B1 to B8	Data Inputs/Outputs
22	$\overline{G}$	Output Enable Input
11, 12, 13	GND	Ground (0V)
23	NC	Not Connected
1	V <sub>CCA</sub>	Positive Supply Voltage
24	V <sub>CCB</sub>	Positive Supply Voltage

TRUTH TABLE

INPUT		FUNCTION		OUTPUT
$\overline{G}$	DIR	A BUS	B BUS	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	Z	Z	Z

X: "H" or "L"

Z: High impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CCA</sub>	Supply Voltage	-0.5 to +7.0	V
V <sub>CCB</sub>	Supply Voltage	-0.5 to +7.0	V
V <sub>I</sub>	DC Input Voltage	-0.5 to V <sub>CCA</sub> + 0.5	V
V <sub>I/OA</sub>	DC I/O Voltage	-0.5 to V <sub>CCA</sub> + 0.5	V
V <sub>I/OB</sub>	DC I/O Voltage	-0.5 to V <sub>CCB</sub> + 0.5	V
I <sub>IK</sub>	DC Input Diode Current	± 20	mA
I <sub>OK</sub>	DC Output Diode Current	± 50	mA
I <sub>OA</sub>	DC Output Current	± 50	mA
I <sub>OB</sub>	DC Output Current	± 50	mA
I <sub>CCA</sub>	DC V <sub>CC</sub> or Ground Current	± 200	mA
I <sub>CCB</sub>	DC V <sub>CC</sub> or Ground Current	± 100	mA
P <sub>d</sub>	Power Dissipation	180	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(\*) 500mW: ≅ 65 °C derated to 300 mW by 10 mW/°C: 65 °C to 85 °C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V <sub>CCA</sub>	Supply Voltage	2.7 to 3.6	V
V <sub>CCB</sub>	Supply Voltage	2.7 to 5.5	V
V <sub>I</sub>	Input Voltage	0 to V <sub>CCA</sub>	V
V <sub>I/OA</sub>	I/O Voltage	0 to V <sub>CCA</sub>	V
V <sub>I/OB</sub>	I/O Voltage	0 to V <sub>CCB</sub>	V
T <sub>op</sub>	Operating Temperature (note 1)	-40 to +85	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (note 2, 3n)	0 to 8	ns/V

1) V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub>2) V<sub>CCA</sub> = 4.5 to 5.5; V<sub>CCB</sub> = 2.7 to 3.6VDC SPECIFICATIONS FOR V<sub>CCA</sub>

Symbol	Parameter	Test Conditions			Value					Unit
		V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)		T <sub>A</sub> = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V <sub>IHA</sub>	High Level Input Voltage	2.7	3.0		2.0			2.0		V
		3.0	3.6		2.0			2.0		
		3.6	5.5		2.0			2.0		
V <sub>ILA</sub>	Low Level Input Voltage	2.7	3.0				0.8		0.8	V
		3.0	3.6				0.8		0.8	
		3.6	5.5				0.8		0.8	
V <sub>OHA</sub>	High Level Output Voltage	3.0	3.0	I <sub>O</sub> = -100 μA	2.9	2.99		2.9		V
		3.0	3.0	I <sub>O</sub> = -12 mA	2.56	2.85		2.46		
		3.0	3.0	I <sub>O</sub> = -24 mA	2.35	2.65		2.25		
		2.7	3.0	I <sub>O</sub> = -12 mA	2.3	2.5		2.2		
		2.7	4.5	I <sub>O</sub> = -24 mA	2.1	2.3		2.0		
V <sub>OLA</sub>	Low Level Output Voltage	3.0	3.0	I <sub>O</sub> = 100 μA		0.0	0.1		0.1	V
		3.0	3.0	I <sub>O</sub> = 24 mA		0.21	0.36		0.44	
		2.7	3.0	I <sub>O</sub> = 12 mA		0.11	0.36		0.44	
		2.7	4.5	I <sub>O</sub> = 24 mA		0.22	0.42		0.5	
I <sub>IA</sub>	Input Leakage Current	5.5	3.6	V <sub>I</sub> = V <sub>CCA</sub> or GND			±0.1		±1.0	μA
I <sub>OZA</sub>	3 State Output Leakage Current	5.5	3.6	V <sub>IA</sub> = V <sub>IHA</sub> or V <sub>ILA</sub> V <sub>IB</sub> = V <sub>IHB</sub> or V <sub>ILB</sub> V <sub>I/OA</sub> = V <sub>CCA</sub> or GND			±0.5		±5.0	μA
I <sub>CCA</sub>	Quiescent Supply Current	5.5	3.6	V <sub>IA</sub> = V <sub>CCA</sub> or GND V <sub>IB</sub> = V <sub>CCB</sub> or GND			8		80	mA
I <sub>CCTA</sub>		5.5	3.6	V <sub>IA</sub> = 3.4V, other V <sub>I</sub> = V <sub>CCA</sub> or GND			1.35		1.5	mA

DC SPECIFICATIONS FOR  $V_{CCB}$ 

Symbol	Parameter	Test Conditions			Value					Unit
		$V_{CCA}$ (V)	$V_{CCB}$ (V)		$T_A = 25\text{ }^\circ\text{C}$			$-40\text{ to }85\text{ }^\circ\text{C}$		
					Min.	Typ.	Max.	Min.	Max.	
$V_{IHB}$	High Level Input Voltage	2.7	3.0		2.0			2.0		V
		3.0	3.6		2.0			2.0		
		3.6	5.5		3.85			3.85		
$V_{ILB}$	Low Level Input Voltage	2.7	3.0				0.8		0.8	V
		3.0	3.6				0.8		0.8	
		3.6	5.5				1.65		1.65	
$V_{OHB}$	High Level Output Voltage	3.0	3.0	$I_O = -100\text{ }\mu\text{A}$	2.9	3.0		2.9		V
		3.0	3.0	$I_O = -12\text{ mA}$	2.56	2.85		2.46		
		3.0	3.0	$I_O = -24\text{ mA}$	2.35	2.65		2.25		
		3.0	4.5	$I_O = -24\text{ mA}$	3.86	4.25		3.76		
$V_{OLB}$	Low Level Output Voltage	3.0	3.0	$I_O = 100\text{ }\mu\text{A}$		0.0	0.1		0.1	V
		3.0	3.0	$I_O = 24\text{ mA}$		0.21	0.36		0.44	
		3.0	4.5	$I_O = 24\text{ mA}$		0.18	0.36		0.44	
$I_{IB}$	Input Leakage Current	5.5	3.6	$V_I = V_{CCA}$ or GND			$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$
$I_{OZB}$	3 State Output Leakage Current	3.6	3.6	$V_{IA} = V_{IHA}$ or $V_{ILA}$ $V_{I/OB} = V_{CCB}$ or GND			$\pm 0.5$		$\pm 5.0$	$\mu\text{A}$
$I_{CCB}$	Quiescent Supply Current	3.6	3.6	$V_{IA} = V_{CCA}$ or GND $V_{IB} = V_{CCB}$ or GND			5		50	mA
$I_{CCTB}$		3.6	5.5	$V_{IB} = 3.4\text{V}$ , other $V_I = V_{CCB}$ or GND			0.35		0.5	mA

## DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions			Value					Unit
		$V_{CCA}$ (V)	$V_{CCB}$ (V)		$T_A = 25\text{ }^\circ\text{C}$			$-40\text{ to }85\text{ }^\circ\text{C}$		
					Min.	Typ.	Max.	Min.	Max.	
$V_{OLPA}$	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	3.3			1.0	1.5			V
					-1.2	-0.6				
$V_{OLPB}$	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	3.3			0.8	1.2			V
					-0.8	-0.5				
$V_{IHDA}$	Dynamic High Voltage Input (note 1, 3)	5.0	3.3				2			V
$V_{ILDA}$	Dynamic Low Voltage Input (note 1, 3)	5.0	3.3		0.8					V
$V_{IHDB}$	Dynamic High Voltage Input (note 1, 3)	5.0	3.3				2			V
$V_{ILDB}$	Dynamic Low Voltage Input (note 1, 3)	5.0	3.3		0.8					V

1) Worst case package

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND

3) max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold ( $V_{ILD}$ ), 0V to threshold ( $V_{IHD}$ ).  $f = 1\text{MHz}$

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r = t_f = 3$  ns,  $V_{CCA} = 2.7$  to  $3.6$  V,  $C_L = 50$  pF)

Symbol	Parameter	Value										Unit
		$V_{CCB} = 5 \pm 0.5$ V					$V_{CCB} = 3 \pm 0.3$ V					
		$T_A = 25$ °C			$-40$ to $85$ °C		$T_A = 25$ °C			$-40$ to $85$ °C		
		Min.	Typ. (*)	Max.	Min.	Max.	Min.	Typ. (**)	Max.	Min.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time An to Bn	1.0	4.8	8.0	1.0	8.5	1.0	5.5	8.5	1.0	9.0	ns
		1.0	3.9	6.5	1.0	7.0	1.0	5.2	8.0	1.0	8.5	
$t_{PZL}$ $t_{PZH}$	Output Enable Time $\bar{G}$ to Bn	1.0	4.7	8.0	1.0	8.5	1.0	6.0	9.0	1.0	9.5	ns
		1.0	4.8	8.5	1.0	9.0	1.0	6.1	9.5	1.0	10.0	
$t_{PLZ}$ $t_{PHZ}$	Output Disable Time $\bar{G}$ to Bn	1.0	4.0	8.0	1.0	8.5	1.0	6.3	9.5	1.0	10.0	ns
		1.0	3.8	7.5	1.0	8.0	1.0	4.5	8.0	1.0	8.5	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time Bn to An	1.0	3.8	6.5	1.0	7.0	1.0	4.4	7.0	1.0	7.5	ns
		1.0	4.3	7.5	1.0	8.0	1.0	5.1	7.5	1.0	8.0	
$t_{PZL}$ $t_{PZH}$	Output Enable Time $\bar{G}$ to An	1.0	5.9	9.5	1.0	10.0	1.0	6.4	10.0	1.0	10.5	ns
		1.0	5.4	9.0	1.0	9.5	1.0	5.8	9.0	1.0	9.5	
$t_{PLZ}$ $t_{PHZ}$	Output Disable Time $\bar{G}$ to An	1.0	4.6	9.5	1.0	10.0	1.0	5.2	9.5	1.0	10.0	ns
		1.0	3.1	6.5	1.0	7.0	1.0	3.4	6.5	1.0	7.0	
$t_{OSLZ}$ $t_{OSHL}$	Output to Output Skew Time (note 1, 2)		1.0	1.5		1.5		1.0	1.5		1.5	ns
			1.0	1.5		1.5		1.0	1.5		1.5	

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW

2) Parameter guaranteed by design

(\*) Typical values at  $V_{CCA} = 3.3$  V  $V_{CCB} = 5.0$  V

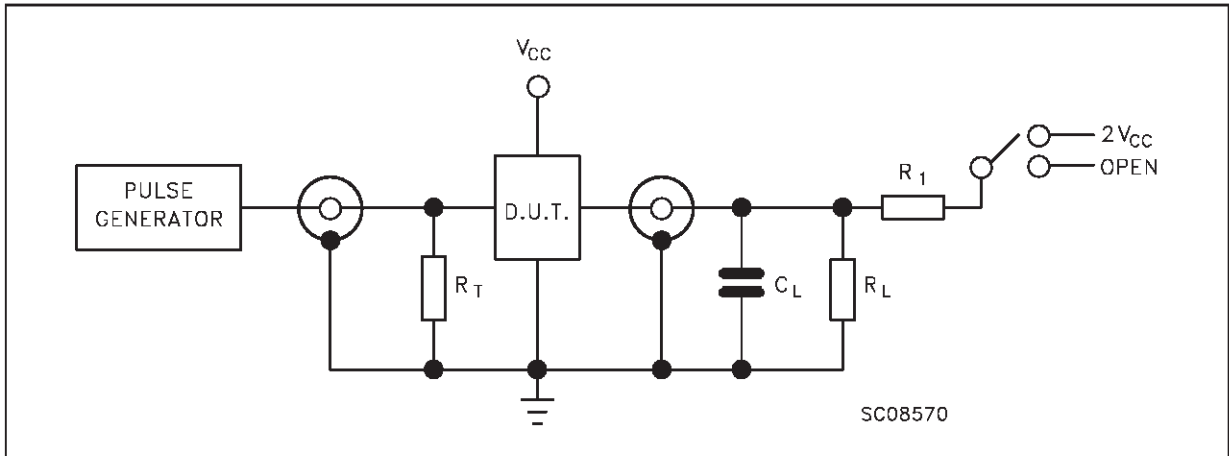
(\*\*) Typical values at  $V_{CCA} = 3.3$  V  $V_{CCB} = 3.3$  V

**CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Test Conditions			Value					Unit	
		$V_{CCB}$ (V)	$V_{CCA}$ (V)		$T_A = 25$ °C			$-40$ to $85$ °C			
					Min.	Typ.	Max.	Min.	Max.		
$C_{INA}$	Input Capacitance	open	open			4.5					pF
$C_{I/O}$	Input/Output Capacitance	3.3	5.0			10					pF
$C_{PD}$	Power Dissipation Capacitance (note 1) A to B	3.3	5.0			50					pF
$C_{PD}$	Power Dissipation Capacitance (note 1) B to A	3.3	5.0			40					pF

1)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$  (per circuit)

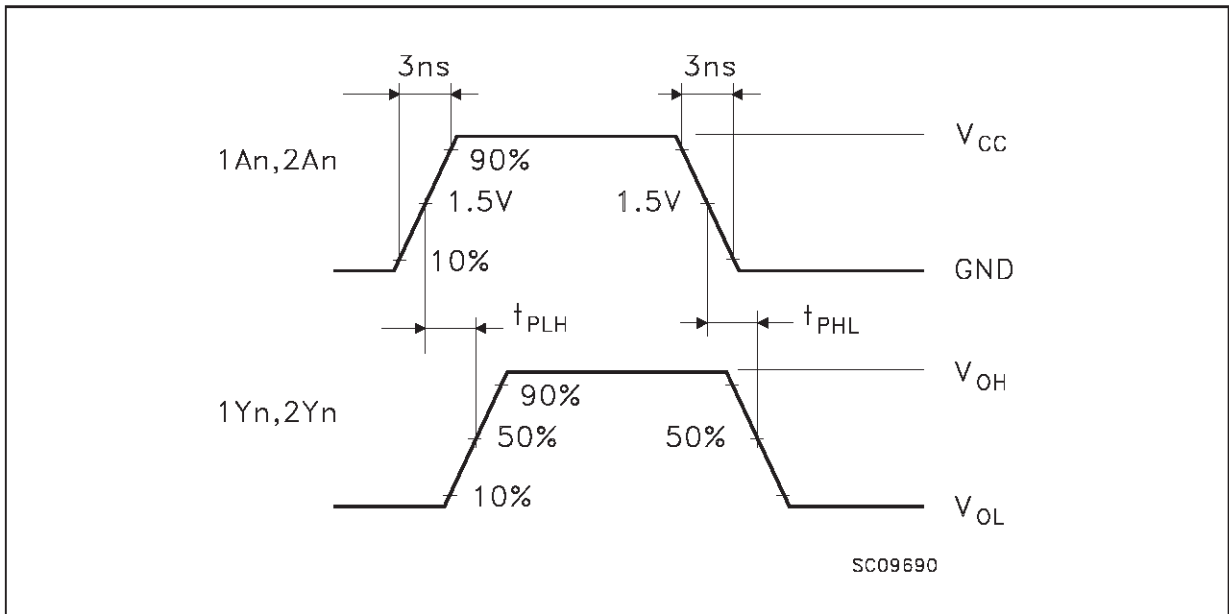
TEST CIRCUIT

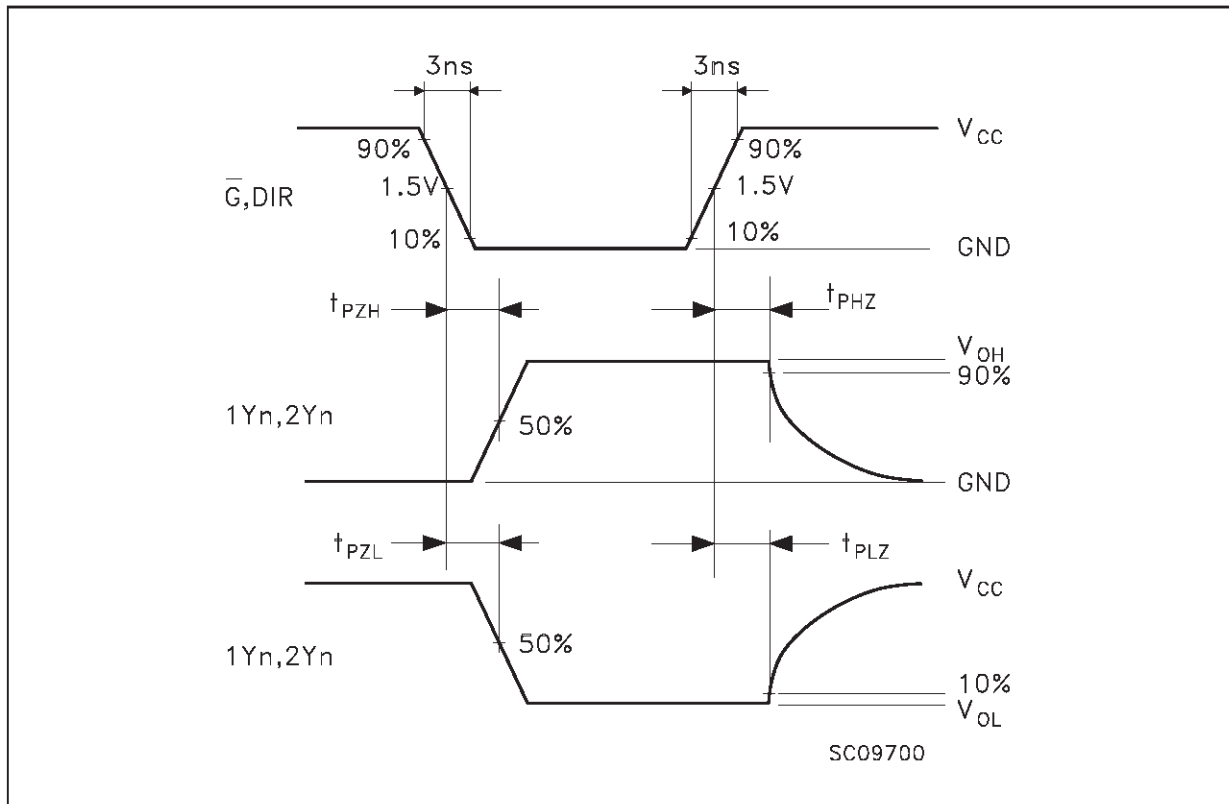


TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	$2V_{CC}$
$t_{PZH}$ , $t_{PHZ}$	Open

$C_L$  = 50 pF or equivalent (includes jig and probe capacitance)  
 $R_L = R_1 = 500\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

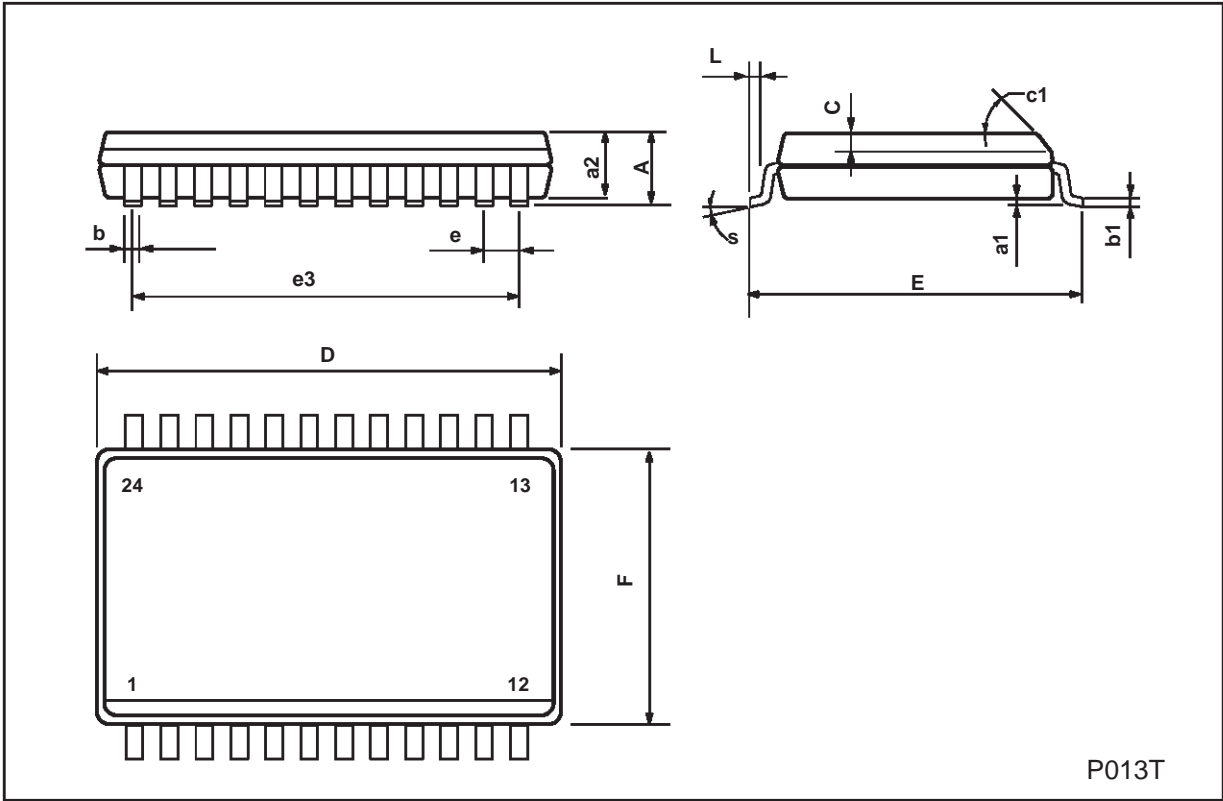
WAVEFORM 1: PROPAGATION DELAYS ( $f=1\text{MHz}$ ; 50% duty cycle)



**WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME** ( $f=1\text{MHz}$ ; 50% duty cycle)

**SO-24 MECHANICAL DATA**

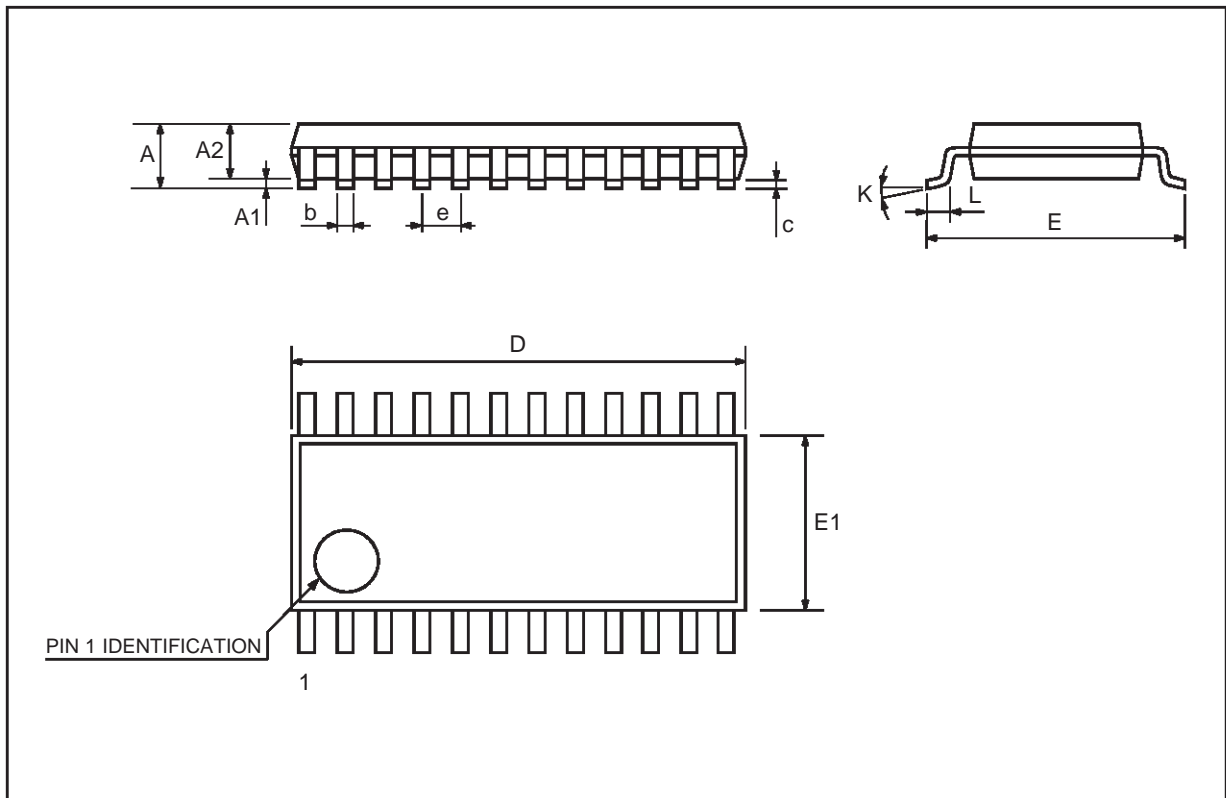
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.420
e		1.27			0.05	
e3		13.97			0.55	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
S	8 (max.)					





## TSSOP24 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	7.7	7.8	7.9	0.303	0.307	0.311
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 1999 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - France - Germany - Italy - Japan - Korea - Malaysia - Malta - Mexico - Morocco - The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.

<http://www.st.com>