Advanced Information

XV750C *NTSC/PAL/SECAM Digital Video Decoder*

Data Sheet

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1. General Description

The XV750C is a high quality video decoder capable of converting NTSC, PAL and SECAM video signals or analog component video signals into digital video signals.

Its built-in scaling function makes it possible to independently set the horizontal and vertical scaling ratios, enabling, for example, of giving output images at the aspect ratio of square pixels.

Two kinds of video output ports namely SV port for streaming output (image data synchronized with input video sync) and DV port for scaling data output, can simultaneously provide image data.

The functional block diagram is shown in Figure 2.1.

2. Features

- Built-in three (3) channel 10-bit ADCs
- Analog composite (CVBS) and S-video inputs
- Supports analog component signal input
- Four (4) line inputs (CVBS, S-video or component is selectable for each line input)
- Supports NTSC-M, NTSC-(Jpn), NTSC-4.43, PAL-B, D, G, H, I, PAL-N, PAL-M, PAL-CombinationN, PAL-60, and SECAM
- Detects Video systems and automatically switches over
- Built-in high image quality Y/C separation circuit (adaptive comb filter[1])
- Built-in Holizontal/Vertical aperture correction circuit
- Built-in automatic-gain control AGC/ACC circuit
- Built-in programmable filter (24 taps)
- Built-in scaler (Horizontal: 1/8 to 2 times, Vertical: 1/8 to 1 time)
- Supports ITU-R BT.601 and 656 output formats (only for SV line output)
- Selectable YCbCr/ RGB color spaces
- MacroVision Detection Function
- VBI (Closed Caption/CGMS/WSS) data extraction and raw data
- 10-bit GPIO pins (availing various status outputs)
- Generating interrupt
- Single 27 MHz clock
- Selection among free-running clock/burst-lock VCXO/line-lock VCXO[2]

[1] Applicable only to NTSC-(Jpn),M, PAL-B,D,G,H,I,N, PAL-M, PAL-CombinationN. Adaptive 3-line comb filter for NTSC, adaptive 5-line comb filter or adaptive 3-line hybrid filter for PAL.
[2] External components are required to form a VCXO circuit for VCXO operation.

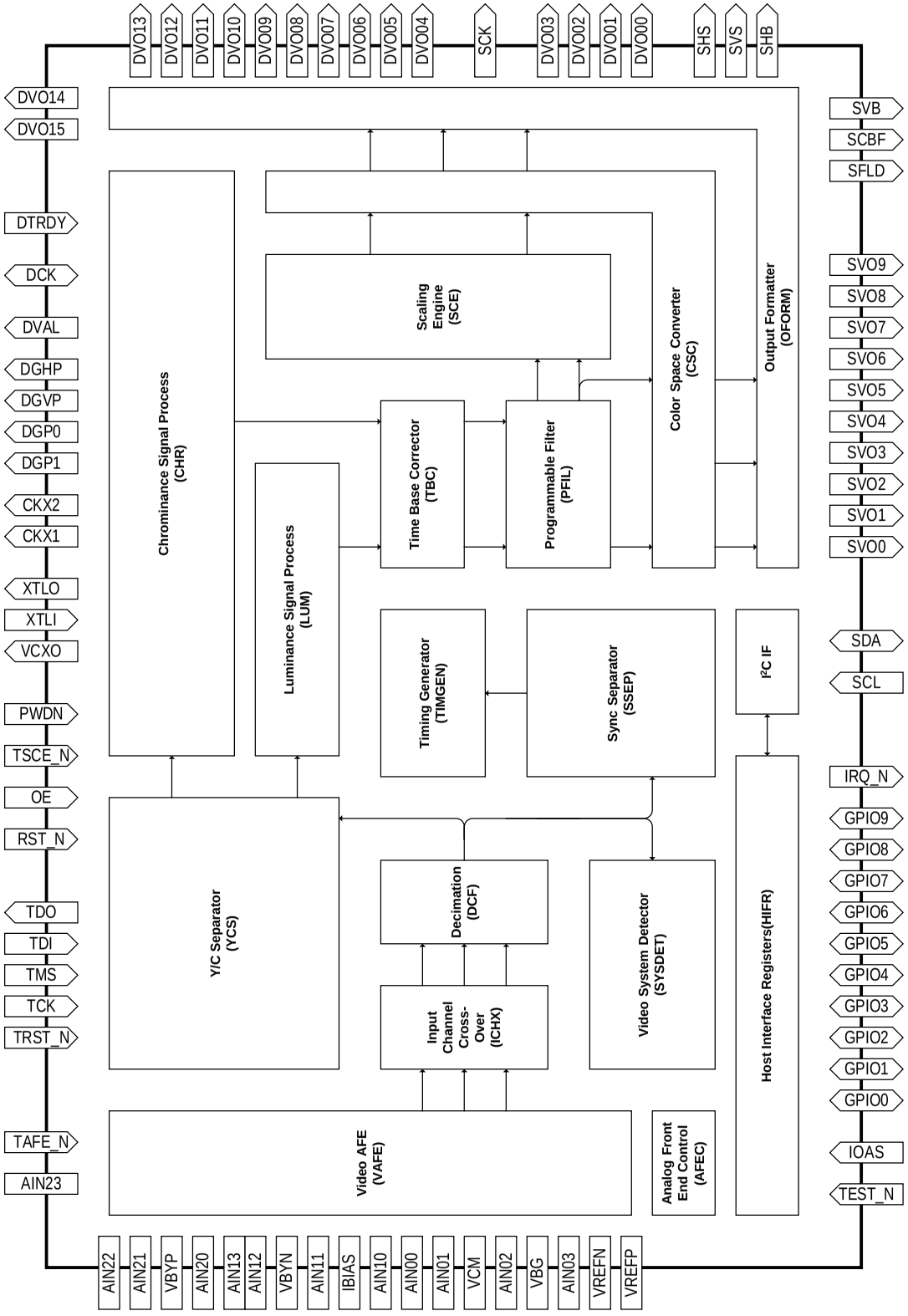


Figure 2.1. Functional block diagram

3. Pins

3.1. Pin Layout

128pin QFP (XV750CQ1)

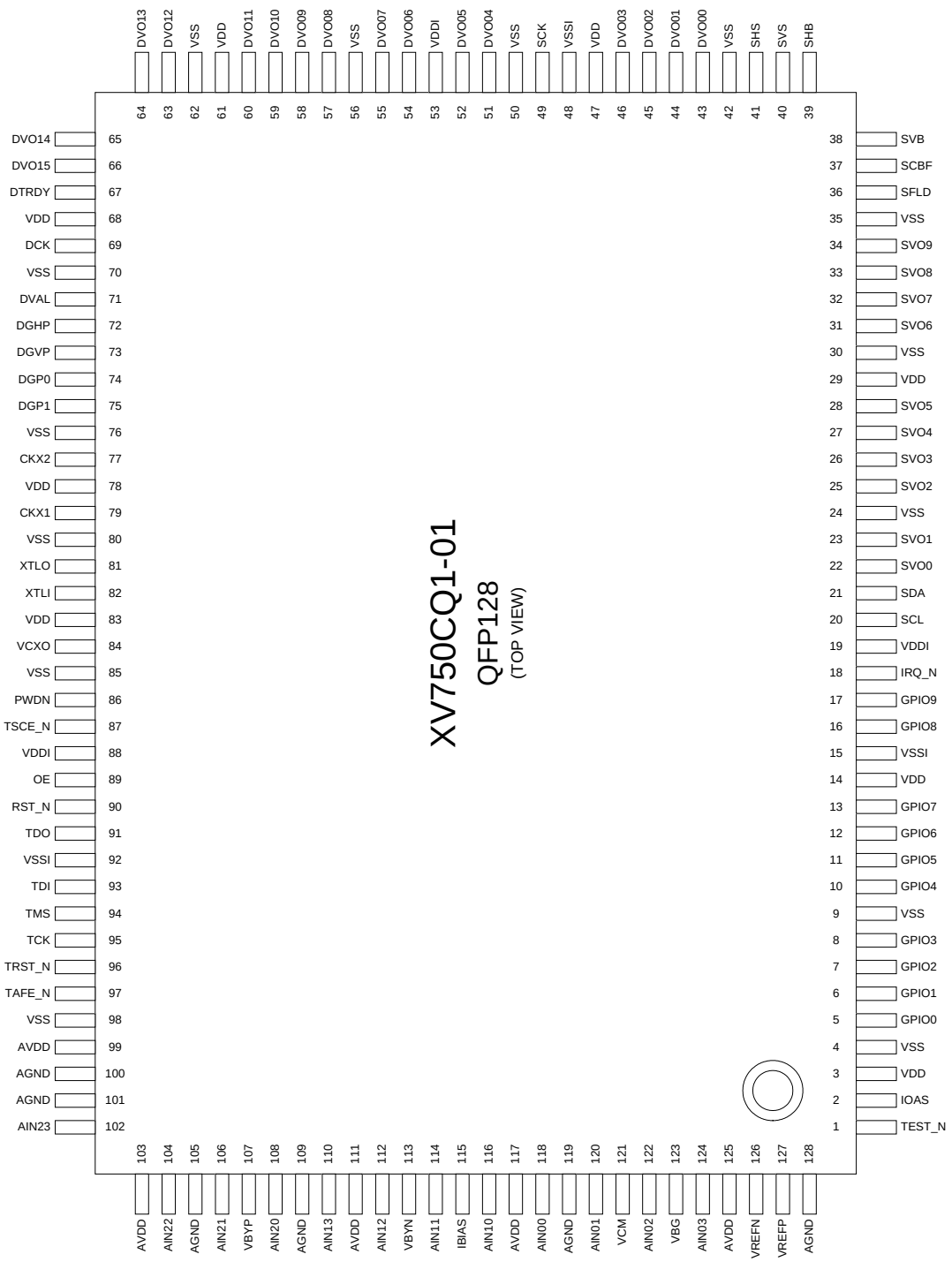


Figure 3.1 Pin layout

3.2. List of Pins

Table 3.1 Pin description

Pin#	Pin Name	I/O	Buffer Type	Description
1	TEST_N	I	Pull Up	Test pin: Normally open or pulled-up
2	IOAS	I	Pull Up	I2C Slave address setting (L:1000100x, H:1000101x)
5-8, 10-13, 16-17	GPIO[9:0]	I/O	Pull Up	General purpose port: Register IO mode, Status output, etc.
18	IRQ_N	O	Open Drain	Interrupt request
20	SCL	I	---	I2C Bus clock
21	SDA	I/O	Open Drain	I2C Bus data
22-23, 25-28, 31-34	SVO[9:0]	O	Tri State	SV port - Video out For details, please refer to "0 Video Port Interface" on page 45.
36	SFLD	O	Tri State	SV port - Field display
37	SCBF	O	Tri State	SV port - Cb display
38	SVB	O	Tri State	SV port - Vertical blanking signal
39	SHB	O	Tri State	SV port - Horizontal blanking signal
40	SVS	O	Tri State	SV port - Vertical sync signal
41	SHS	O	Tri State	SV port - Horizontal sync signal /CSYNC
43-46, 51-52, 54-55, 57-60, 63-66,	DVO[15:00]	O	Tri State	DV port - Video out For details, please refer to "0 Video Port Interface" on page 45.
49	SCK	O	---	SV port - Clock
67	DTRDY	I	Pull Up	DV port - Target ready signal
69	DCK	I/O	---	DV port - Clock
71	DVAL	O	Tri State	DV port - Data enable/Gated clock
72	DGHP	O	Tri State	DV port - Horizontal general purpose signal
73	DGVP	O	Tri State	DV port - Vertical general purpose signal
74	DGP0	O	Tri State	DV port - General purpose signal 0
75	DGP1	O	Tri State	DV port - General purpose signal 1
77	CKX2	O	---	Clock output (double the pixel clock frequency)
79	CKX1	O	---	Clock output (pixel clock frequency)
81	XTLO	O	---	Crystal output
82	XTLI	I	---	Crystal input
84	VCXO	O	Tri State	PWM output for VCXO control voltage
86	PWDN	I	---	Power down: When "H" is applied, power down mode (releasable by register setting) When "L" is applied, normal mode
87	TSCE_N	I	Pull Up	Test pin: Normally open or pulled-up

Pin#	Pin Name	I/O	Buffer Type	Description
89	OE	I	---	Output port enable: When "H" is applied, output ports (SVO, DVO) are enabled. (Only the used pins will be enabled. For example, when in SV port 8-bit output mode, unused lower 2 bits will be "Hi-Z") When "L" is applied, the SVO and DVO ports will be forced to "Hi-Z"
90	RST_N	I	Pull Up	Reset signal. Reset by "L" input.
91	TDO	O	Tri State	JTAG
93	TDI	I	Pull Up	JTAG
94	TMS	I	Pull Up	JTAG
95	TCK	I	Pull Up	JTAG
96	TRST_N	I	Pull Up	JTAG
97	TAFE_N	I	Pull Up	VAFE test pin: Normally open or pulled-up
102	AIN23	I	Analog	Analog video input, CH2 - 3(SV-C/D1-Pb/D1-Pr)
104	AIN22	I	Analog	Analog video input, CH2 - 2(SV-C/D1-Pb/D1-Pr)
106	AIN21	I	Analog	Analog video input, CH2 - 1(SV-C/D1-Pb/D1-Pr)
107	VBYP	I	Analog	Analog chroma - Clamp voltage-in: usually connected with VCM
108	AIN20	I	Analog	Analog video input, CH2 - 0(SV-C/D1-Pb/D1-Pr)
110	AIN13	I	Analog	Analog video input, CH1 - 3(SV-C/D1-Pb/D1-Pr)
112	AIN12	I	Analog	Analog video input, CH1 - 2(SV-C/D1-Pb/D1-Pr)
113	VBYN	I	Analog	Analog chroma - Clamp voltage-input: usually connected to VCM
114	AIN11	I	Analog	Analog video input, CH1 - 1(SV-C/D1-Pb/D1-Pr)
115	IBIAS	I	Analog	Analog test pin: Usually connected with analog GND
116	AIN10	I	Analog	Analog video input, CH1 - 0(SV-C/D1-Pb/D1-Pr)
118	AIN00	I	Analog	Analog video input, CH0 - 0(CVBS/SV-Y/D1-Y)
120	AIN01	I	Analog	Analog video input, CH0 - 1(CVBS/SV-Y/D1-Y)
121	VCM	O	Analog	Analog common voltage
122	AIN02	I	Analog	Analog video input, CH0 - 2(CVBS/SV-Y/D1-Y)
123	VBG	O	Analog	Analog band-gap voltage
124	AIN03	I	Analog	Analog video input, CH0-3 (CVBS/SV-Y/D1-Y)
126	VREFN	O	Analog	Analog reference voltage (negative)
127	VREFP	O	Analog	Analog reference voltage (positive)
3, 14, 29, 47, 61, 68, 78, 83,	VDD	---	---	Digital VDD (+3.3V for buffer)
4, 9, 24, 30, 35, 42, 50, 56, 62, 70, 76, 80,85, 98,	VSS	---	---	Digital GND
15, 48, 92,	VSSI	---	---	Digital GND
19, 53, 88,	VDDI	---	---	Digital VDD (+2.5V)
99, 103, 111, 117, 125,	AVDD	---	---	Analog VDD (+2.5V)
100, 101, 105, 109, 119, 128	AGND	---	---	Analog GND

4. Functions

4.1. Operating Clock

The XV750C uses a 27MHz clock for digitally sampling the video signals.

As to the clock signals fed to XV750C, two kinds of solutions are readily available, namely free-running operation and VCXO operation.

4.1.1. Free Running Operation

Free-running is a mode of operation where video signal is decoded using a clock-oscillating module or a clock within the system not synchronized with the input video signal. Sample connection diagrams are shown in Figure 4.1. The dotted lines are connected as required.

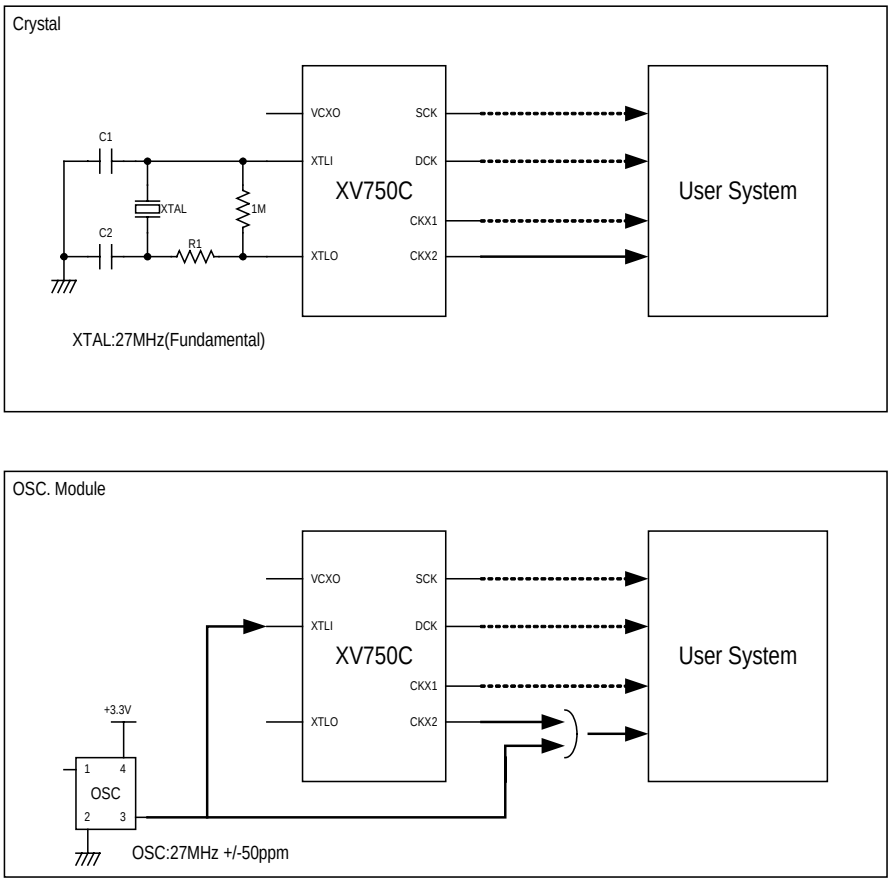


Figure 4.1 Clock connection (free-running)

4.1.2. VCXO Operation

VCXO is a mode of operation where the video signal is decoded using the clock, synchronized with the input video signal, generated by an external VCXO circuit. Sample connection diagrams are shown in Figure 4.2. The dotted lines are connected as required.

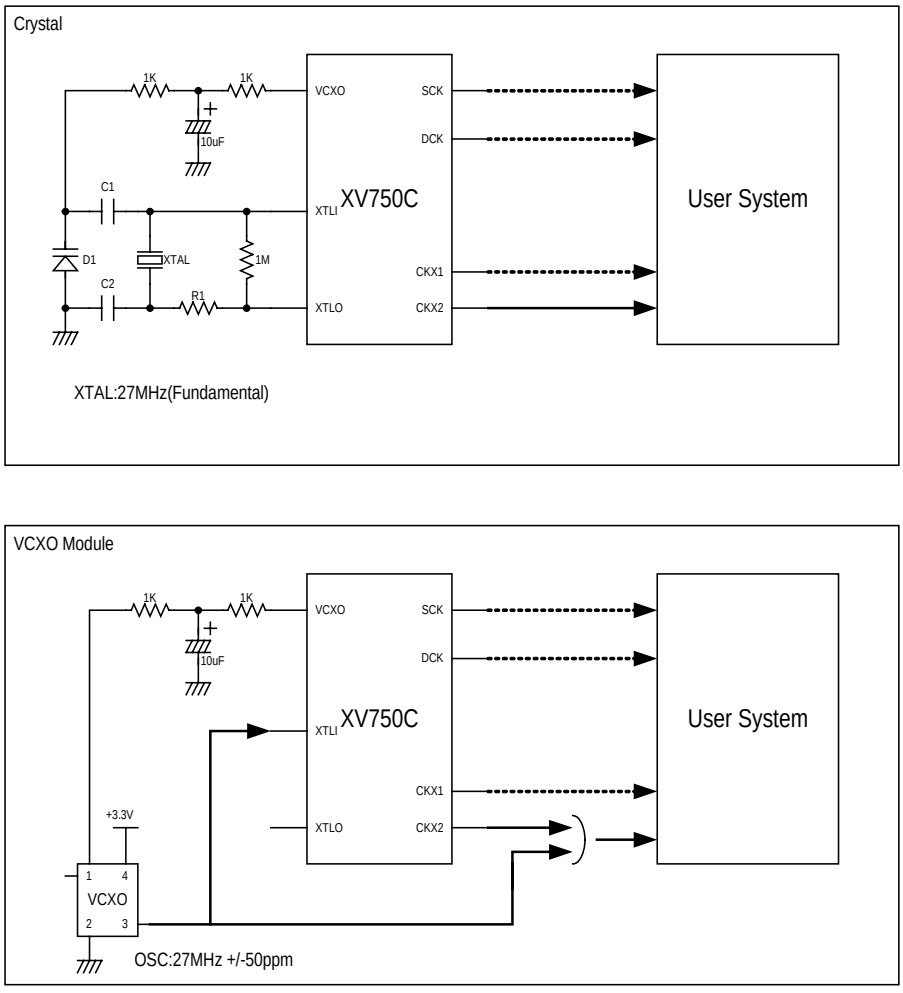


Figure 4.2 Clock connection (VCXO)

4.1.3. VCXO Control

The XV750C is furnished with an external VCXO controlling circuit to generate a sampling clock by way of burst-lock or H-lock (line-lock.), giving controlling voltage output in PWM for the external VCXO circuit.

VCXO control works in the following four (4) different modes selected by register VCXODEF_MOD:

Table 4.1 Selection of VCXO Control Modes

VCXODEF_MOD	Operation		
	CVBS/S-Video	Component	No Sync.
0	Off (Fixed voltage output)	Off (Fixed voltage output)	Off (Fixed voltage output)
1	Burst lock[3]	Off (Fixed voltage output)	Freeze
2	H-lock (Line lock)	H-lock (Line lock)	Freeze
3	Automatic	Automatic	Freeze

Conditions that H-lock is selected when Automatic; Logical OR below:
1: NTSC-4.43
2: PAL-60
3: SECAM
4: Color killer detected
5: Non-standard signal detected
6: Non-interlaced
7:Component
Conditions that Burst lock is selected when Automatic:
1: When the above conditions are all False.

4.2. Input Video Interface

4.2.1. Conforming Video Standards (Video Systems)

For composite video (CVBS) and S-video inputs, the XV750C can decode the video signals in NTSC-M, NTSC-(Jpn), NTSC-4.43, PALB, D, G, H, I, PAL-N, PAL-M, PAL-CombinationN, PAL-60, and SECAM standard.

It also accepts component signals, where 7:3 Video/Sync Ratio or 10:4 Video/Sync ratio is selectable.

Table 4.2 Conforming video standards

Video System	Line / Frame	Fh	Fv	Blanking Setup	Fsc
NTSC-(Japan)	525Lines	15.734264KHz	59.94Hz	0IRE	3.579545MHz
NTSC-M	525Lines	15.734264KHz	59.94Hz	7.5IRE	3.579545MHz
NTSC-4.43	525Lines	15.734264KHz	59.94Hz	0IRE	4.43361875MHz
PAL-B,D,G,H,I	625Lines	15.625KHz	50Hz	0IRE	4.43361875MHz
PAL-N	625Lines	15.625KHz	50Hz	7.5IRE	4.43361875MHz
PAL-M	525Lines	15.734264KHz	59.94Hz	7.5IRE	3.57561149MHz
PAL-CombiN	625Lines	15.625KHz	50Hz	0IRE	3.58205625MHz
PAL-60	525Lines	15.734264KHz	59.94Hz	0IRE	4.43361875MHz
SECAM	625Lines	15.625KHz	50Hz	0IRE	---

For each video standards' register settings, please refer to "4.17 Video Standard Detection/Automatic Switching Circuit " on page 68.

[3] Unstable with signal without color burst.

4.2.2. Analog Front-end

The XV750C has built-in analog front-end (VAFE) that consists of 27MHz sampling 10-bit video-ADCs, variable-gain video amplifiers, clamp circuits and 4-to-1 multiplexers (Figure 4.3.)

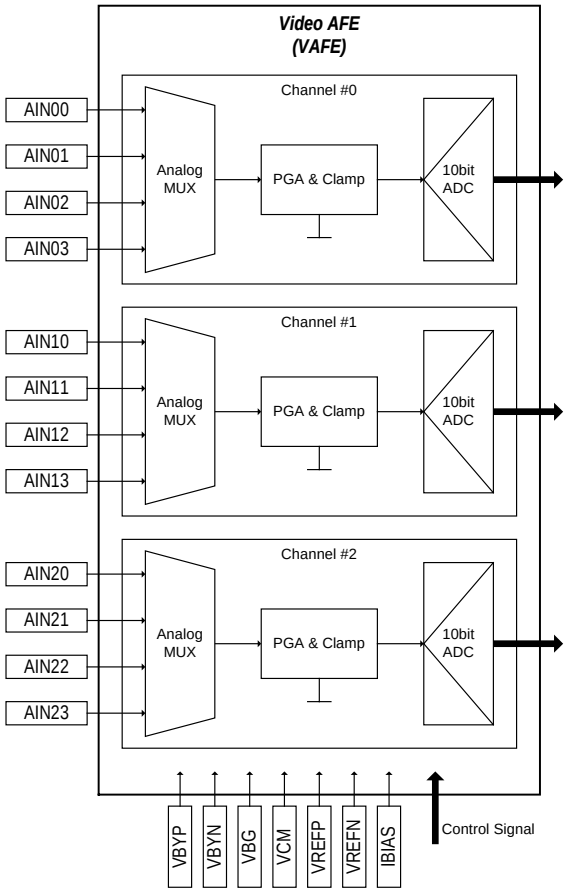


Figure 4.3 Analog Front-end Block Diagram

Please refer to Figure 4.4 for the handling of analog pins.

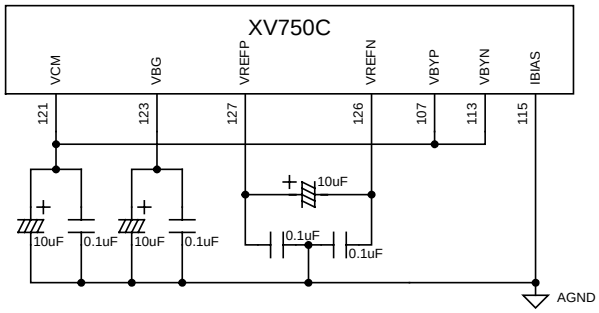


Figure 4.4 Analog pin Terminations

Using host interface register settings, the following controls can be done to the VAFE.

Auto/Manual Gain control (for each channel)

Please refer to Figure 4.9 for the 8 steps of PGA gain setting.

Power down control (for each channel)

Please refer to register LPWCS_

Analog multiplexer control (common to all channels)

4-to-1 selection. Please refer to the register AIMS_.

4.2.3. Connecting Video Signals

Pin description

N and M in the analog video input pin naming of AINnm, stands for the VAFE channel number and the input line number respectively.

Table 4.3 Analog video signal input pins

	VAFE Channel		
System	#0	#1	#2
0	AIN00	AIN10	AIN20
1	AIN01	AIN11	AIN21
2	AIN02	AIN12	AIN22
3	AIN03	AIN13	AIN23

The VAFE channel number 0 (pins AIN00, AIN01, AIN02 and AIN03) is dedicated for the composite signal, S-video or component's luminance signal and Sync on Green signal. Since the channel number 1 and 2 are interchangeable by way of register settings, please refer to Table 4.4.

The registers ICHX_DYCH, ICHX_DCCH and ICHX_DPCH are used to set the relation between the physical channel numbers (#0, #1, and #2) and the logical channel names (Ych, Cch, and Pch) of the VAFE. The logical channel names are Ych (Y channel) to give CVBS or Y input, Cch (C channel) to give C of S-Video or Cb of Component input and Pch (P channel) to give Cr input of Component signal.

Table 4.4 VAFE channels

	Register			VAFE Channel		
Input	ICHX_DYCH	ICHX_DCCH	ICHX_DPCH	#0	#1	#2
CVBS	0	d.c.	d.c.	CVBS	n.c.	n.c.
S_Video	0	1	2	Y	C	n.c.
S_Video	0	2	1	Y	n.c.	C
Component	0	1	2	Y	Cb	Cr
Component	0	2	1	Y	Cr	Cb

d.c: Don't Care

n.c.: No Connection

Connection Examples

Connection examples show the cases where analog video signals are fed to the XV750C:

Example 1 Figure 4.5: CVBS on Line 0, S-Video on Line 1, component on Line 2, CVBS on Line 3

Example 2 Figure 4.6: CVBS on Line 0 to 3

Example 3 Figure 4.7: Component on Line 0 to 3

Example 4 Figure 4.8: The case where the VAFE channels #1 and #2 are interchanged in example 1, by changing settings in the registers ICHX_DCCH and ICHX_DPCH.

By setting input video signal mode for each line (CVBS, S-Video or Component) in the register AINDEF_SELm (m means input line number) in advance, input lines change can be simply done by the register AIMS_SELP.

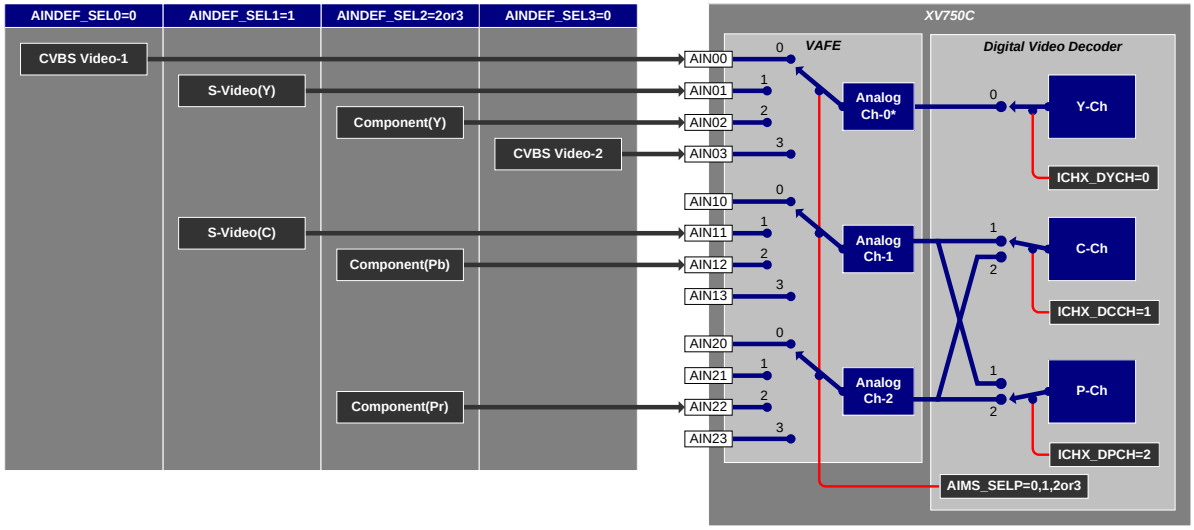


Figure 4.5 Analog Video Signal Connection Example (1)

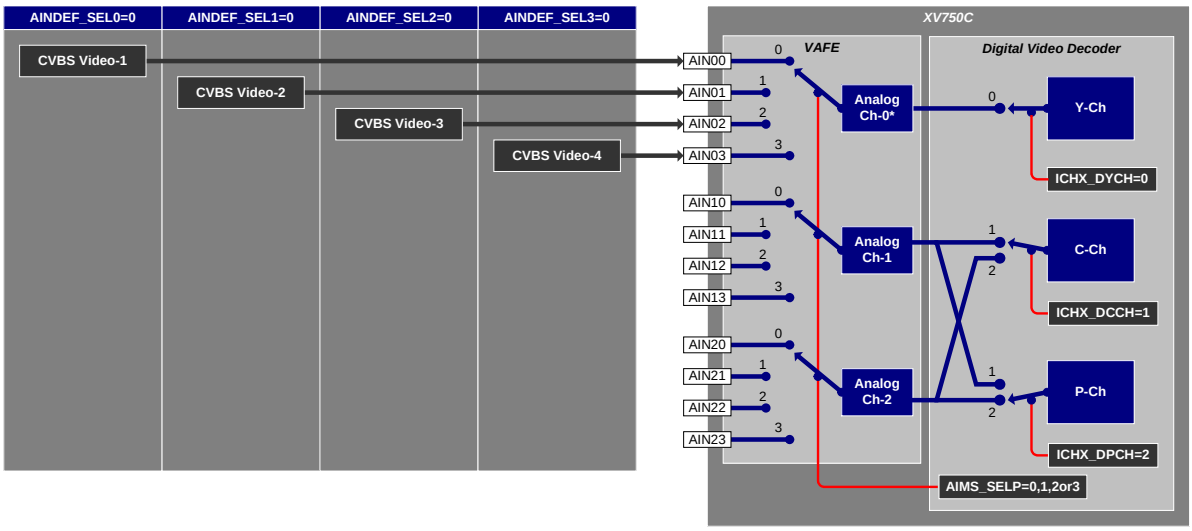


Figure 4.6 Analog Video Signal Connection Example (2)

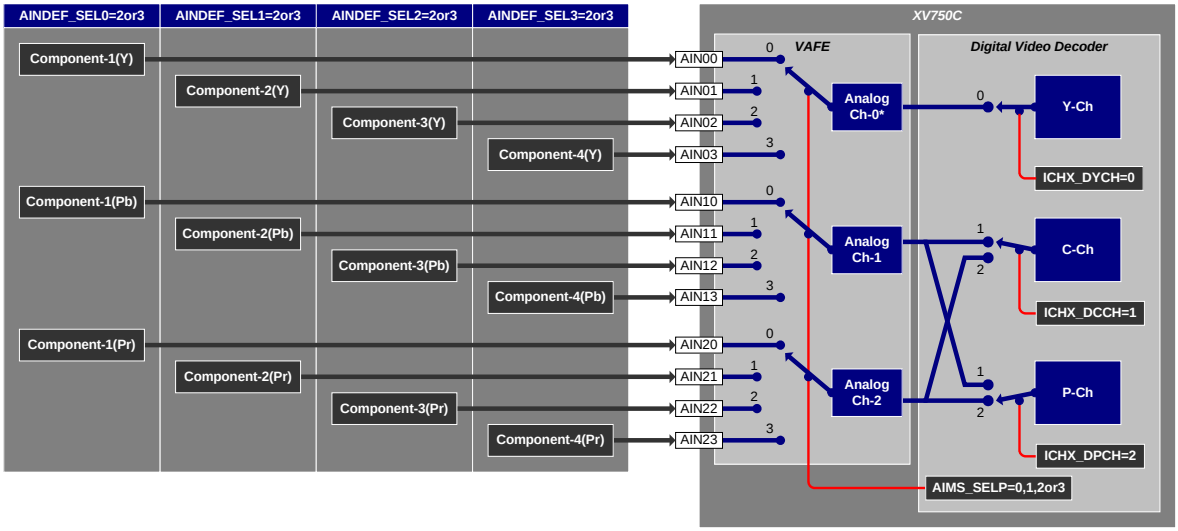


Figure 4.7 Analog Video Signal Connection Example (3)

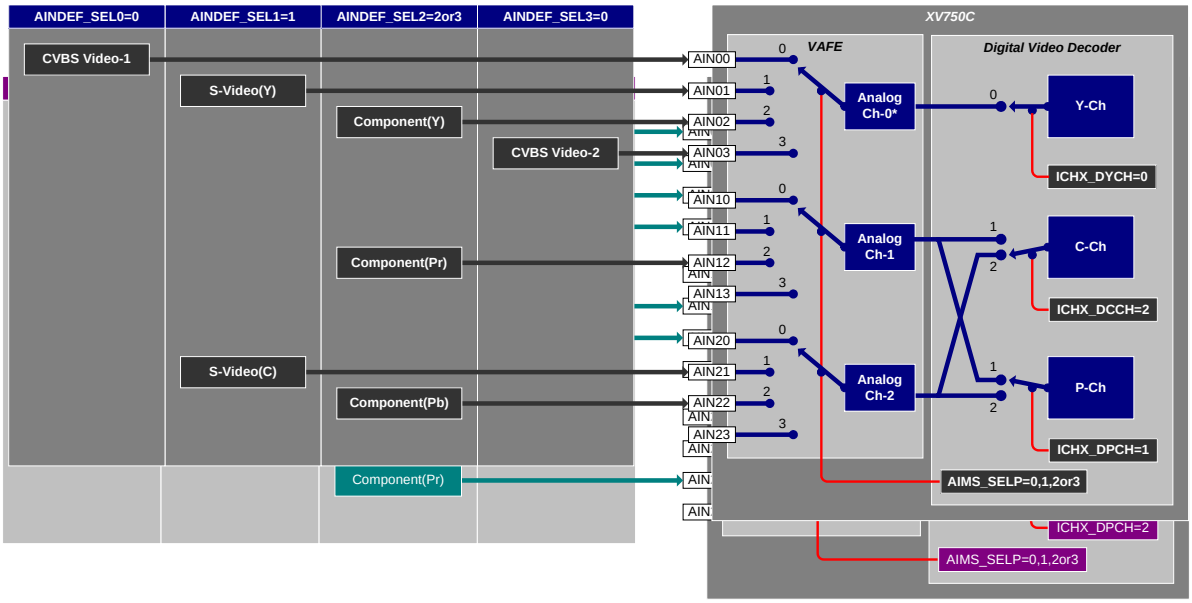


Figure 4.8 Analog Video Signal connection Example (4)

4.2.4. Video Signal Levels

Figure 4.9 shows the signal levels within VAFE when 75% color bar signal is applied at 1Vp-p. Please note that the voltage levels and the gain values below are approximate numbers (voltage levels shown: for NTSC/PAL.)

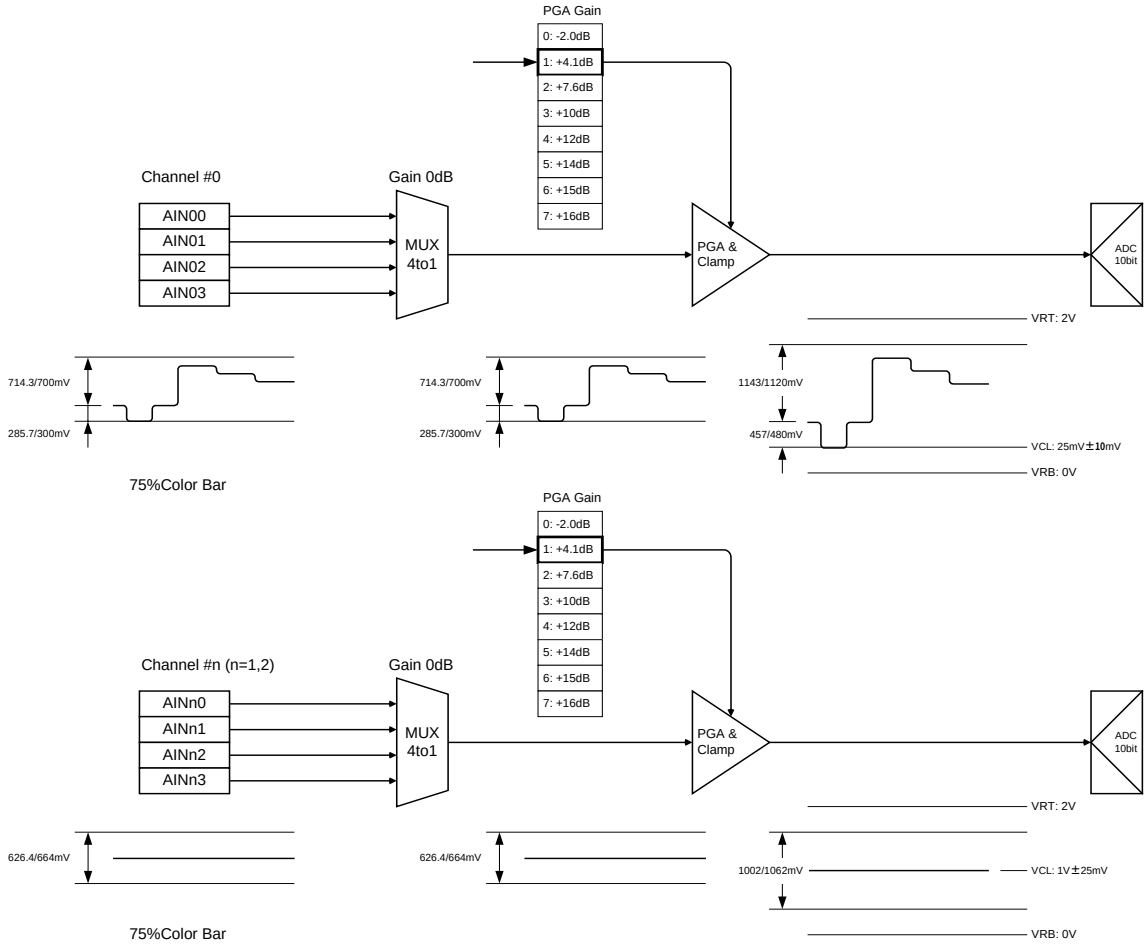


Figure 4.9 Signal levels

4.3. Decimation Filter

The XV750C has a built-in decimation filter in order to degrade the video signals that have been originally sampled at 27MHz sampling rate at the analog front end down to 13.5MHz sampling rate. Figure 4.10 shows the frequency characteristic of the decimation filter.

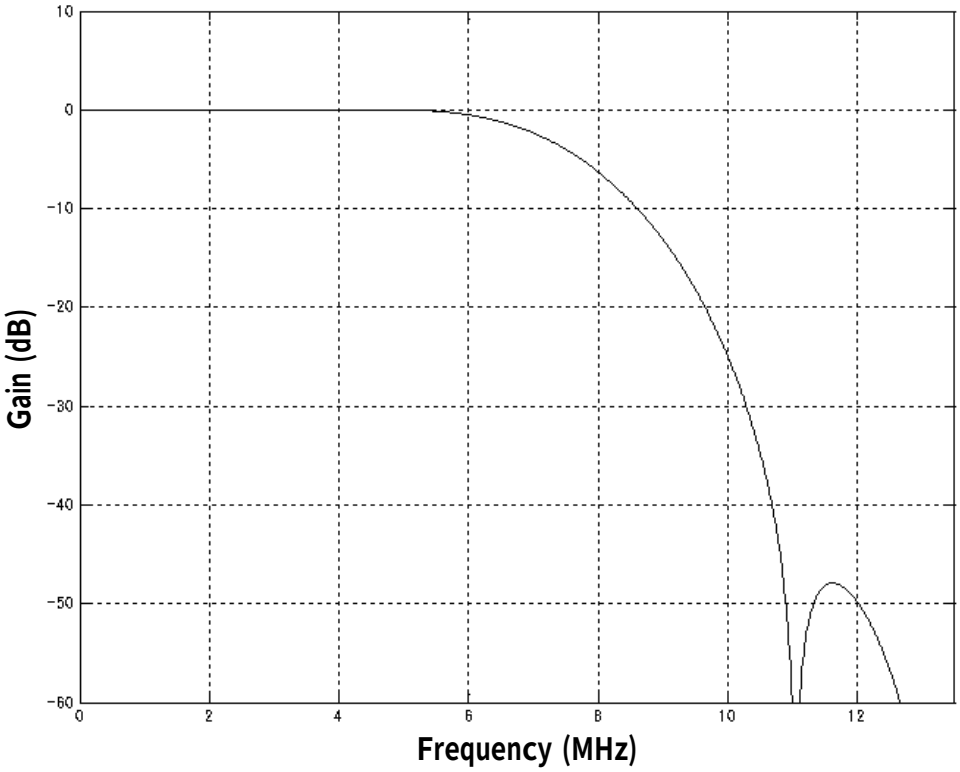


Figure 4.10 Characteristic of decimation filter

4.4. Y/C Separation

The Y/C separation circuit automatically selects the optimal filter based on the video system used. Please refer to Table 4.5 for the register settings.

Note. The case where comb filter is selected is limited when color sub-carriers on adjacent lines bear 180-degree (90-degree in the case of PAL) phase difference. Even in the case of such video system, if once the color sub-carriers move away from the above mentioned standard phase difference, the filter will automatically be switched over to trap and band pass filter.

Table 4.5 Filter for Y/C separation circuit

Video System	Register COMBDEF		Y/C Separation Filter
	COMS	PAFS	
NTSC-Jan,M	0	d.c.	Adaptive 3-line comb filter
	1	d.c.	Fixed 3-line comb filter
NTSC-4.43	d.c.	d.c.	Trap and band pass filter
PAL-B,D,G,H,I,N,M,cN	0	0	Adaptive 5-line comb filter
	0	1	Adaptive 3-line hybrid filter
	1	0	Fixed 5-line comb filter
	1	1	Fixed 3-line comb filter
PAL-60	d.c.	d.c.	Trap and band pass filter
SECAM	d.c.	d.c.	Trap and band pass filter

d.c. ： Don't care

4.4.1. Adaptive 3-line Comb Filter (NTSC-Jpn,M)

The adaptive 3-line comb filter utilize three (3) lines; the decoding line (LN0) together with its previous line and the next line (LN-1 and LN+1.). The pixel correlative judgment between the lines, switches between 3-line comb filter (LN-1, LN0 and LN+1) and 2-line comb filter [LN-1 and LN0] or [LN0 and LN+1].

4.4.2. Adaptive 5-line Comb Filter (PAL-B,D,G,H,I,N,M,cN)

The adaptive 5-line comb filter is identical to adaptive 3-line comb filter in its comb filter operation except the numbers of line used. It uses three (3) lines; decoding line (LN0) together with LN-2 and LN+2 lines, skipping the directly adjacent lines. Setting the register, this can be switched to 3-line adaptive hybrid filter. The adaptive 5-line comb filter produces the video signal with less cross-color in comparison with the 3-line adaptive hybrid filter.

4.4.3. Adaptive 3-line hybrid filter (PAL-B,D,G,H,I,N,M,cN)

The 3-line adaptive hybrid filter automatically switches and uses comb filter using LN-1 and LN+1 or band-pass filter using LN0, resulting of adaptability judgment. It gives better color reproducibility for horizontal-stripe color in comparison with the case using 5-line adaptive comb filter.

4.4.4. Trap Filter and Band-pass Filters

Y/C separation is performed using band-pass and trap filters. There are two band-pass filters; for 3.58MHz and for 4.43MHz. Three types of trap filters are available; for 3.58MHz, for 4.43MHz and for SECAM. The characteristics of those filters are shown in Figure4.11 and Figure 4.15.

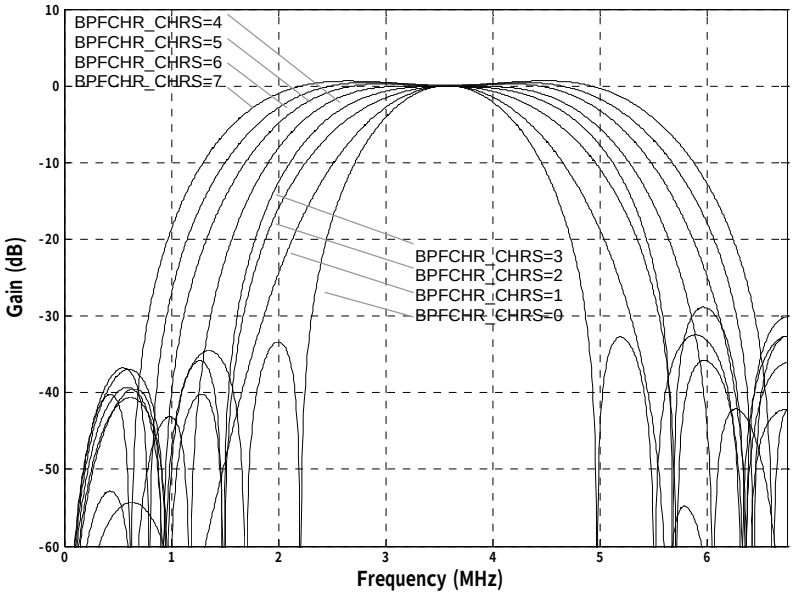


Figure4.11 Characteristics of band-pass filter (3.58MHz)

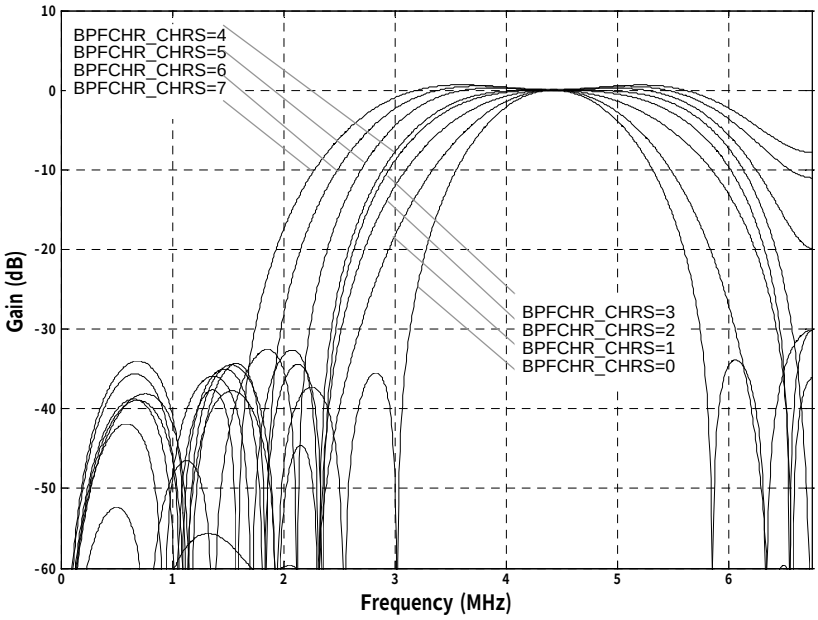


Figure 4.12 Characteristics of band-pass filter (4.43MHz)

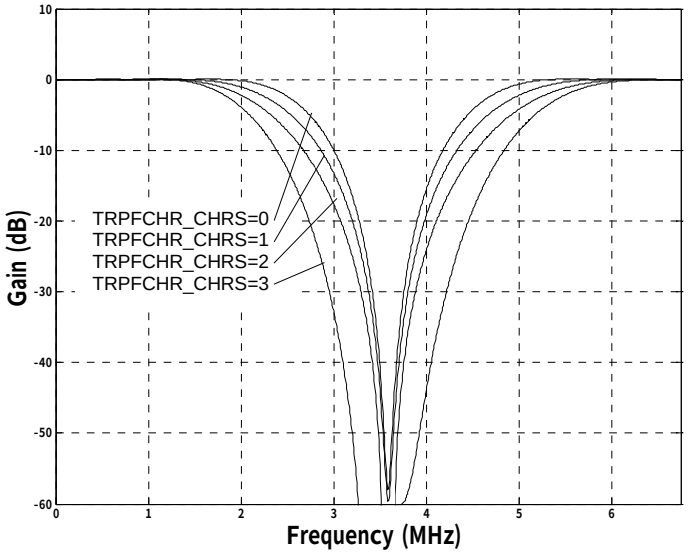


Figure 4.13 Characteristics of trap filter (3.58MHz)

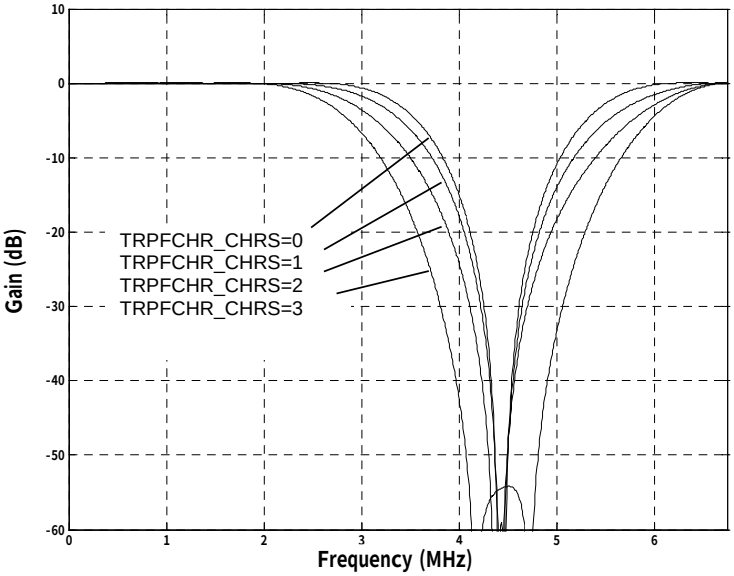


Figure 4.14 Characteristics of trap filter (4.43MHz)

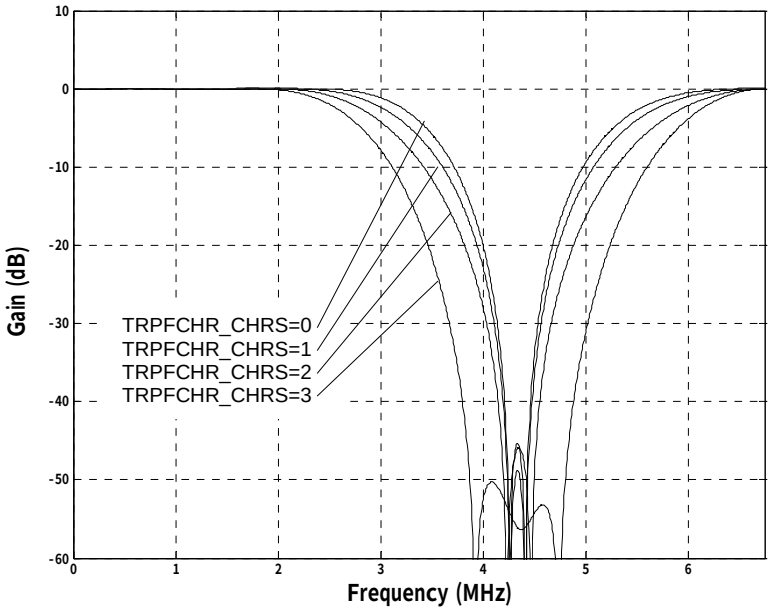


Figure 4.15 Characteristics of trap filter (SECAM)

4.5. Chrominance Signal Processing

In the chrominance signal processing, chrominance signal is decoded out from chrominance signal after Y/C separation.

4.5.1. ACC

Except for SECAM video, the XV750C can function ACC on the chrominance signal after Y/C separation. The ACC circuit, monitoring the color burst amplitude of the input video signal, automatically calculates the appropriate gain. Digital multiplier then, will provide adequate chrominance signal, based on the calculated gain.

There are three (3) modes of operation in ACC based on the register values; 0 for fixed gain (gain value being set by register), 1 for digital ACC (for C channel and P channel, analog gain can be separately set by register) and 3 for automatic gain control. In automatic gain control mode, the analog gains for C channel and P channel become identical to the one for Y channel. When component input is applied, the digital AGC gain value will be used as digital U/V gain.

Alternately it is possible through a register setting, to freeze the gain value to the then current value.

The ACC time constant can be adjusted in eight (8) steps by register setting.

4.5.2. Chrominance Decoding Circuit

This Chrominance decoding circuit supports various video systems of NTSC, PAL and SECAM, and processes the input chrominance modulated components through high precision arithmetic circuit. For SECAM decoding built-in Bell Filter, De-emphasis Filter and FM Demodulation Circuit are provided with. Figure 4.16 shows the Bell Filter characteristics while Figure 4.17 shows the De-emphasis Filter characteristics respectively.

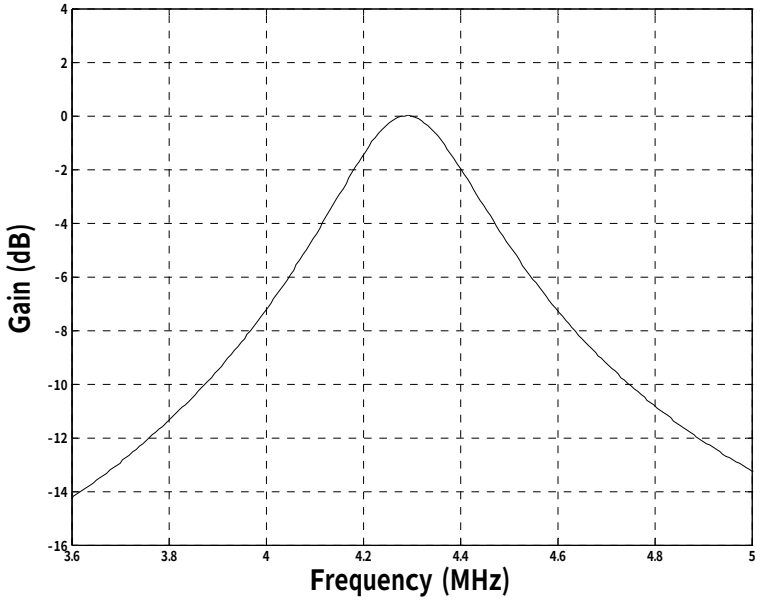


Figure 4.16 Characteristic of SECAM BELL filter

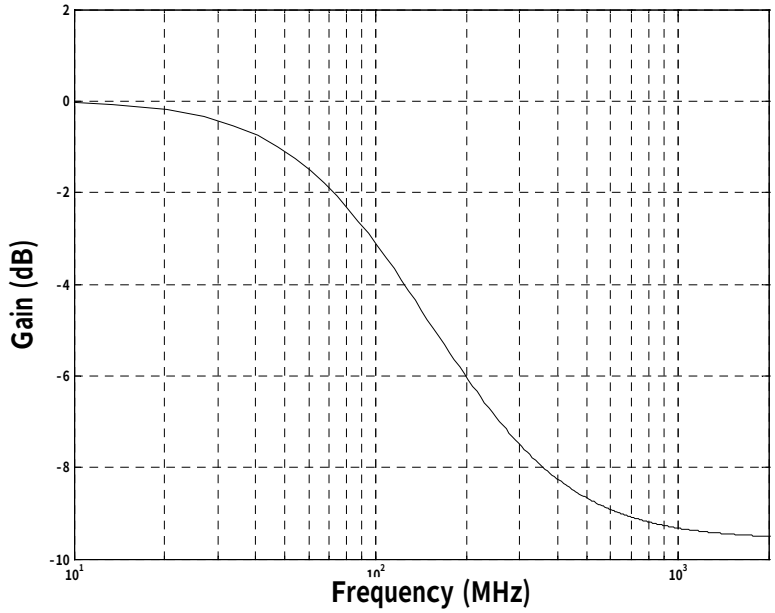


Figure 4.17 Characteristic of SECAM De-Emphasis filter

4.5.3. Color Density Adjustment

Color density adjustment (chrominance adjustment) before decoding is available for NTSC and PAL only, and is performed commonly for U and V.

Post-decoding color density adjustment (color trimming) is available for U and V independently for all the video standards. For details, please refer to the description of the register CLMK_.

4.5.4. Hue Trimming

Hue Trimming is only available for NTSC color modulating mode. For PAL, Hue Trimming in a minimal manner avails. Hue Trimming is provided targeting for the case used during decoding video signal in NTSC color modulating mode (color mode = 0). Generally due to the inherent restrictions, PAL and SECAM color modulation modes will not avail Hue Trimming; the XV750C makes it possible for PAL color modulation mode (color mode = 1) to undergo Hue Trimming in a pseudo-manner. In case of SECAM, however, the register value shall be neglected.

4.5.5. Detection of Color Field Sequence

Detecting the color field information, the following pin output will be made available.

- CFR: pulse output in the designated color field. For output pin, please refer to 4.15.1 Timing Output Pins.

-CFSINF: color field number at the time of the input. For output pin, please refer to 4.21.4 CFR/CFS Signal Output.

-CFS: strobe pulse to latch CFSINF. For output pin, please refer to 4.21.2 Status Output Mode.

4.6. Luminance Signal Processing

The luminance signal processing extracts brightness signal by eliminating sync signal component from the luminance signal after Y/C separation.

4.6.1. AGC

The XV750C provides with AGC function over luminance signal after Y/C separation. The AGC circuit automatically calculates the adequate gain and functions, monitoring the amplitude of the input video sync signal and the peak value of the luminance signal. (It is also possible to cut off the peak control, operating AGC only on the sync.) The total gain, output versus input signal, shall be obtained by the function of the circuits of both analog programmable gain amplifier (PGA) and digital AGC. There are four (4) AGC operation modes: selections are available on the register AGCDEF_MOD namely 0 for fixed gain (fixed for both analog PGA gain, digital gain), 1 for digital AGC operation (with analog PGA gain fixed), and 2 for analog and digital AGC operation (up to input level 120%), and 3 for analog and digital AGC operation (up to input level 200%). The fixed gain value for analog PGA and total gain can be preset respectively on the registers YGFXA_FXGA and LGFXD_FXGD. It is also possible to freeze the gain through the register setting, at the then current value,

when operating in both of the digital AGC and analog digital AGC. Please refer to the related register: AGCDEF_ for details. When operating in digital AGC and analog & digital AGC, based on the calculated gain for Analog PGA and Digital Multiplier, Programmable Gain Amplifier (PGA) and Digital Multiplier will yield an adequate luminance signal. Figure 4.18 shows Input video signal level versus PGA gain.

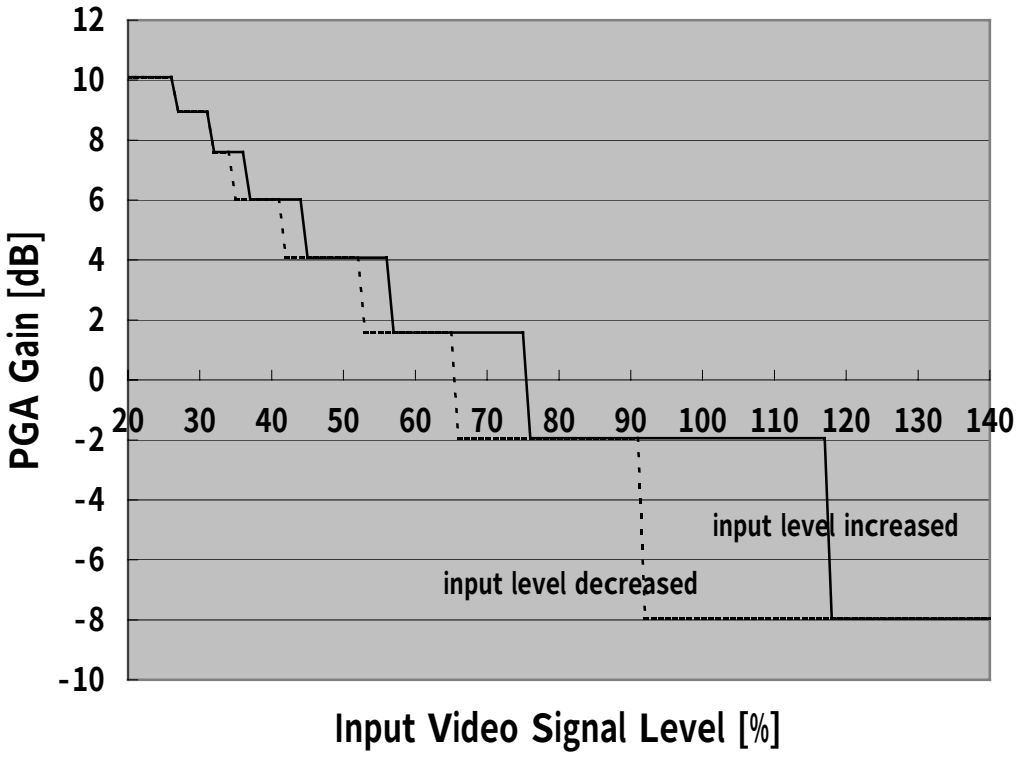


Figure 4.18 Input video signal level versus PGA gain

4.6.2. Pedestal clamp

The pedestal clamp removes the sync signal from the luminance signal. The setup level of 7.5IRE can be supported using register setting.

Setup level setting for NTSC-M or NTSC-Jpn:	Register MNVM_MOD[5]
Setup level setting for PAL-B, D, G, H, I, N:	Register MNVM_MOD[6]
Setup level setting for PAL-M:	Register MNVM_MOD[7]

4.6.3. Brightness and Contrast Adjustment

The brightness and contrast controls are readily available. The adjustment can be done through the register settings; register BRTT_BRTT for brightness adjustment and register CONT_CONT for contrast adjustment.

4.6.4. Horizontal Aperture Correction

The XV750C is capable of enhancing aperture by detecting the horizontal directional edge of the luminance signal. The frequency bandwidth for the enhancement and the level of enhancement are also adjustable. For details please refer to the description on the related register APCOR_.

Figure 4.19 shows the frequency response characteristics.

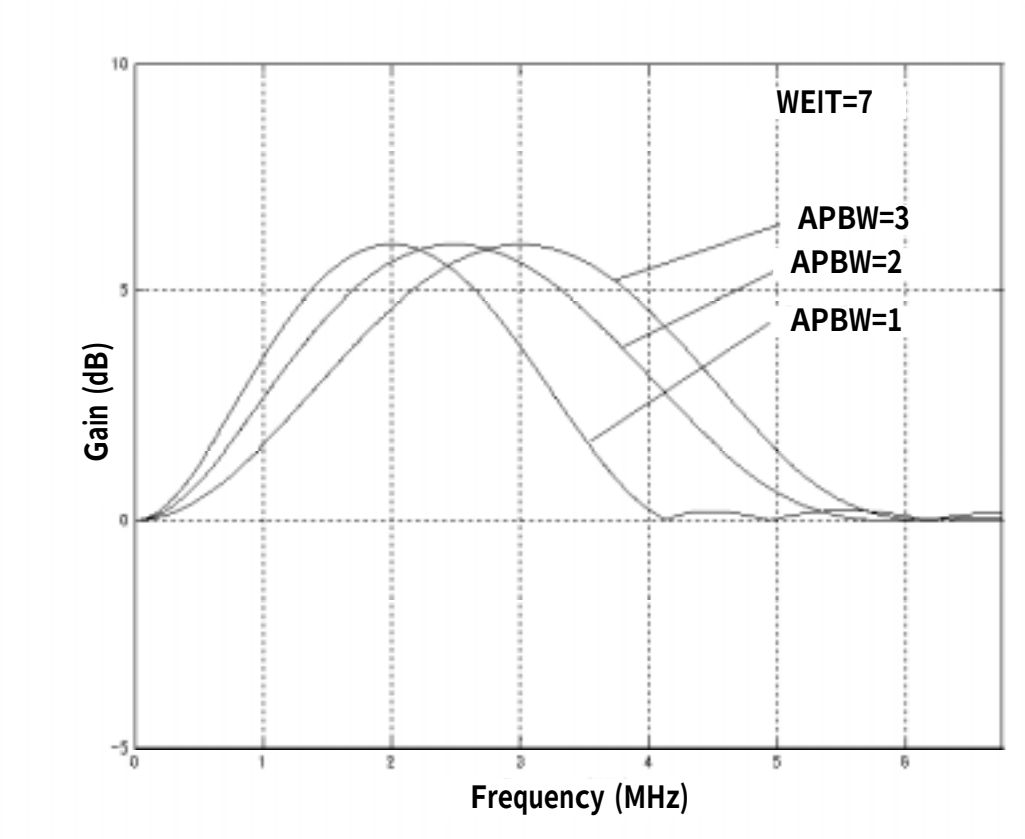


Figure 4.19 Characteristics of horizontal aperture correction filter

In addition, XV750C is provided with coring function in order to reduce the noisiness caused by the aperture correction. Figure 4.20 shows the coring characteristics.

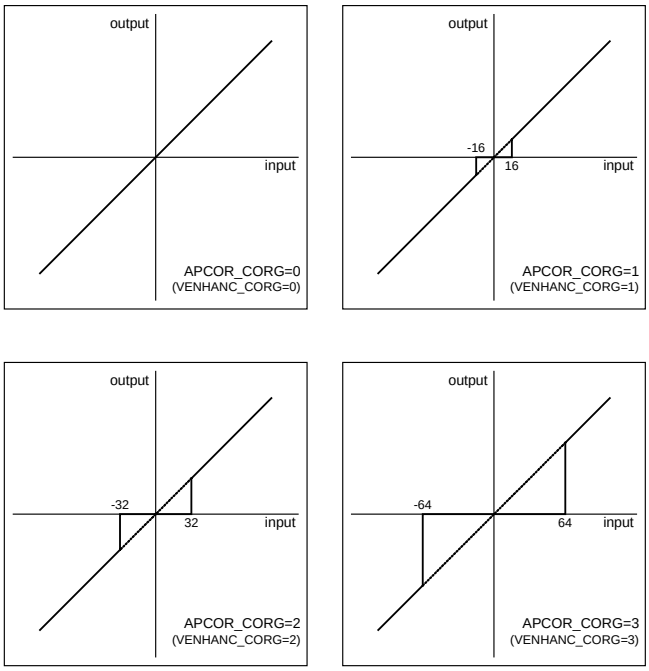


Figure 4.20 Coring characteristics

4.6.5. Vertical Aperture Correction

The XV750C is capable of enhancing apertures by detecting the vertical directional edge of the luminance signal. The level of enhancement and coring characteristics are also adjustable. For details please refer to the description on the related register VENHANC_. Figure 4.21 shows the frequency response characteristics. The coring characteristics will be same as that of Figure 4.20.

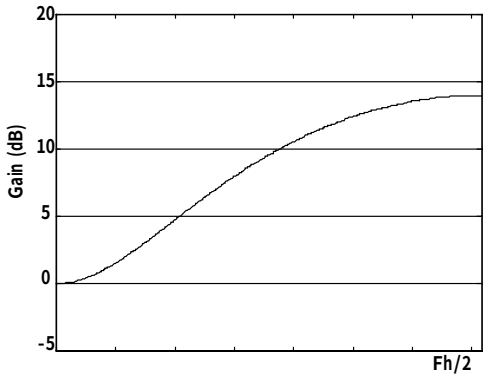


Figure 4.21 Characteristics of vertical aperture enhancement filter

4.7. PJC

The XV750C has a built-in PJC Filter to correct horizontal sampling jitter in 1/16 pixel unit both in luminance signal channel and in chrominance signal channel. With this filter functioning in order, the output phase difference of the sync signal and data could be maintained at constant. The filter characteristic is shown in the Figure 4.22. When the XV750C being driven under VCXO control, the ON/OFF of the PJC Filter will be switched over automatically. This is to make the frequency characteristics flat, switching PJC Filter off when the input signal being TV signal or the like and VCXO control working effectively. In order not to use the automatic switching, please set the register PJSCSW_AUTO to 0 (Manual).

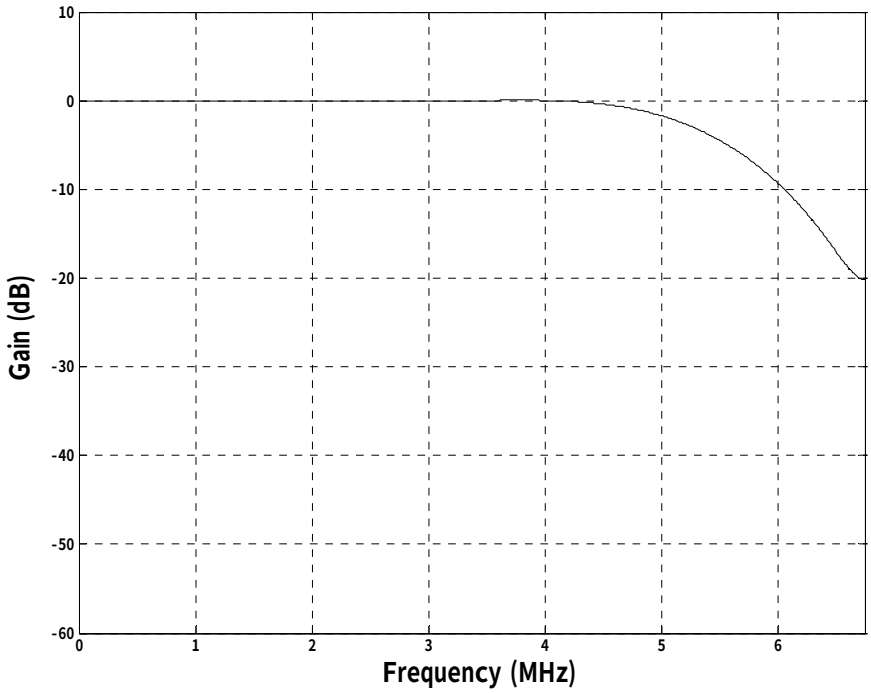


Figure 4.22 PJC Filter Characteristics

Including these functions, PJC Filter can be enabled or disabled through the register setting; for luminance signal with PJCSW_YPJC and for chrominance signal with PJCSW_CPJC, respectively.

4.8. TBC

The XV750C has a built-in Line TBC that generates output horizontal sync signal at a stable constant cycle (in pixel unit.) When the TBC is enabled [TBCDEF_ENB=1], it generates output horizontal sync (SHS) and horizontal blanking signal (SHB) so that the horizontal interval during

active line (line other than vertical blanking) interval is uniformly maintained. This functions to compensate the digitizing error caused in the output horizontal interval when the XV750C is operated in free-running clock mode, by operating in such manner as to absorb the accumulation of 1 field error caused by the compensation, during vertical blanking interval. (This operation of absorbing the accumulated errors is expressed as "TBC reset".) This means the existence of lines deviating from standard value, in its output horizontal interval during vertical blanking interval. In those cases, however, the active horizontal interval is still kept constant as far as possible[4].
When using at [TBCDEF_ENB=1], please set the PJC on by all means.

The deviation of horizontal sync frequency Fh to be absorbed by Line TBC being ±18Hz(NTSC), if in case it goes beyond the limit within 1 field, TBC becomes overflowed, when the TBC operation suspends. This situation continues till TBC resetting takes places.
If the line frequency Fh very much differs from the standard, the TBC overflow occurs. Since the register FHCTLS_TBCT can adjust the pixel cycle per line of the TBC circuit, such control is possible as to avoid the occurrence of overflow. It is also noted that the register [FHCTLS_TBCE=1] being enabled, the above register [FHCTLS_TBCE=1] becomes disabled and the XV750C will automatically select the pixel cycle per line.

The lines where TBC reset going to take place are set at each field's beginning of the vertical blanking interval (EOF reset) and ending of the vertical blanking interval (SOF reset). These are adjustable line per line by registers TBCDEF_RLE and TBCDEF_RLS, respectively.
In addition, there are two modes of TBC operation differentiated by the manner controlling the TBC reset and deviation in horizontal interval. Those two operation modes can be selected using the register TBCDEF_MOD.
It is recommended to use at the default setting of [TBCDEF_MOD=1].

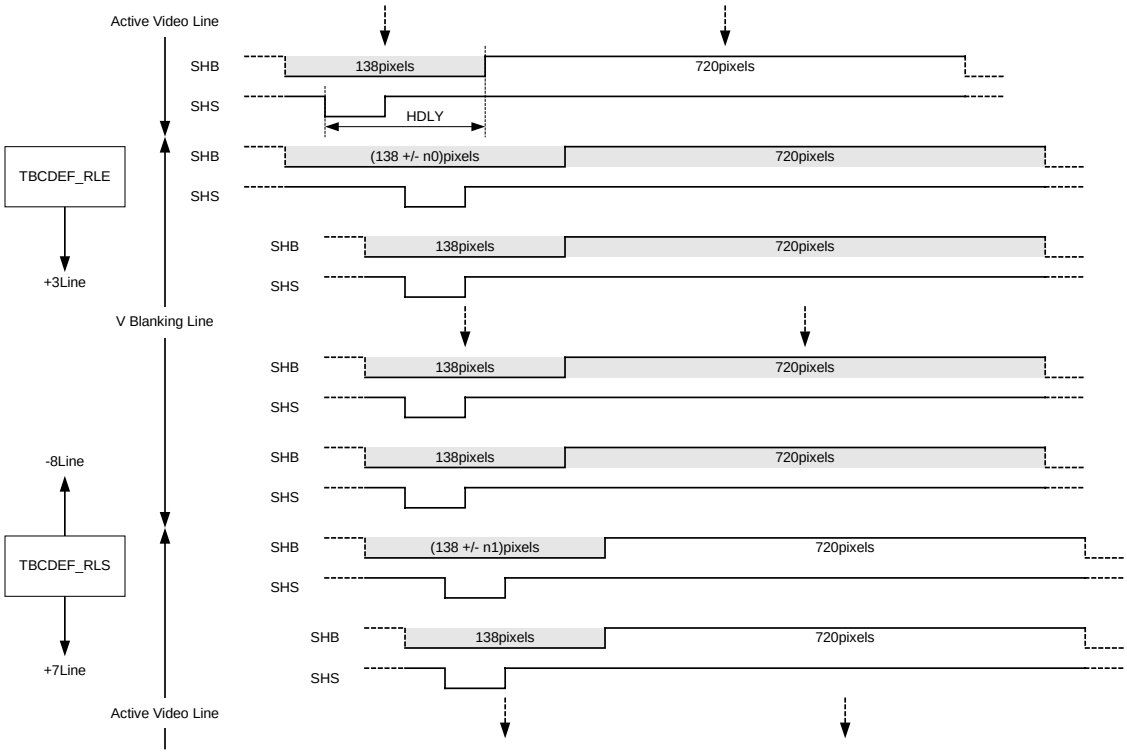
Note:! The TBC capability will work only for SV Line output.

[4] If horizontal interval becomes extremely too short to maintain standard horizontal interval, active horizontal interval might be shortened.

4.8.1. TBC Mode 0

In TBC mode 0, the TBC reset is going to be performed only twice at the EOF and SOF reset lines. The horizontal interval is kept constant except on the TBC resets.

Figure 4.23 explains the operation.



HDLY=122(fv=60Hz), HDLY=132(fv=50Hz)

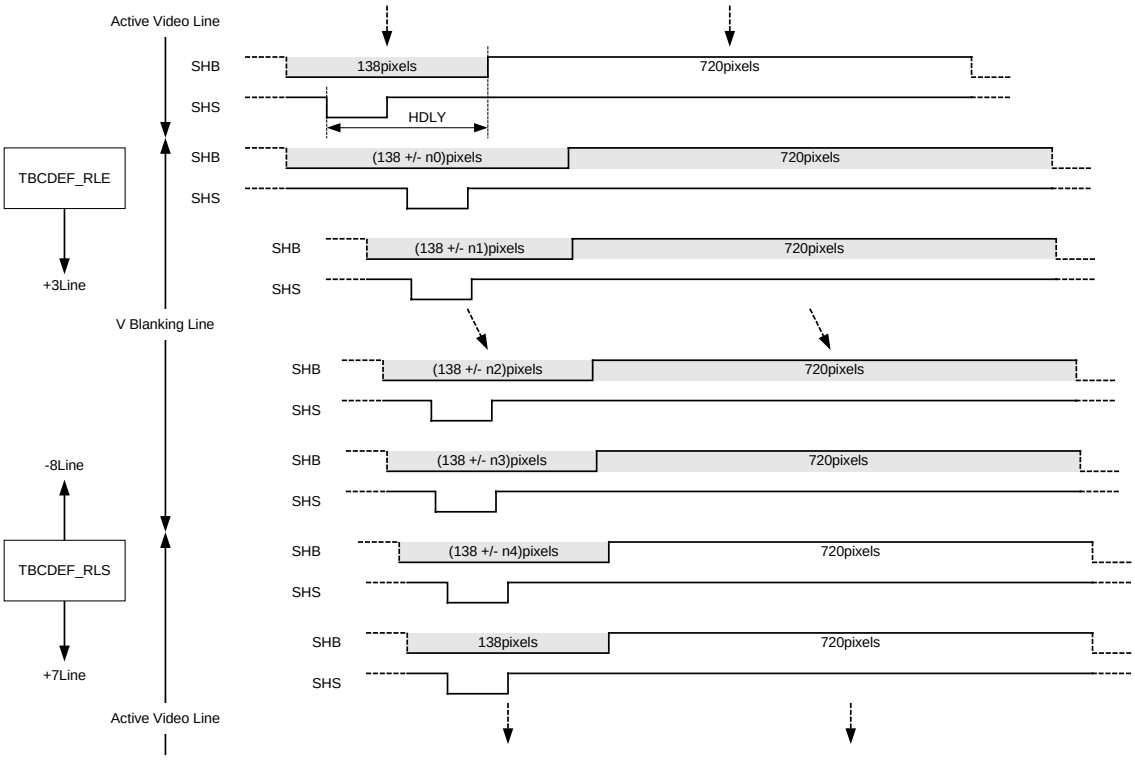
Figure 4.23 TBC Mode 0

The Line TBC is aimed to keep the horizontal interval at the standard value, during active video interval (the actual period showing on the screen). This mode especially tries to maintain the characteristics as much as possible in the whole field inclusive of blanking interval in addition to active video interval. The digitizing error accumulated during the interval, shall be released on the EOF and SOF reset lines. (Because of this, the horizontal interval shall deviate on these lines only.) Both of the reset lines release the errors, at the EOF those accumulated during active video interval while at the SOF those accumulated during blanking interval. In other words, distortions accumulated on the field are going to be released through 2 lines separately. Generally, since the number of lines is greater in the active video interval than in blanking, the accumulated distortion becomes bigger in active video interval, therefore, horizontal interval deviation at the EOF reset line becomes greater comparatively than at the SOF reset line. Because of this reason, the horizontal interval

from blanking interval to active video interval, can be relatively smoothly connected.

4.8.2. TBC Mode 1

In TBC mode1, TBC reset works effective from EOF reset line to SOF reset line. The accumulated error going to be reset at the EOF reset line first, and thereafter the output horizontal intervals deviate from its standard value every time digitizing error occurs. As the result, the deviation in the horizontal sync to be absorbed at SOF reset is not more than the error that occurs during a line. Figure 4.24 explains this operation.



HDLY=122(fv=60Hz), HDLY=132(fv=50Hz)

Figure 4.24 TBC mode 1

Although compared to TBC Mode 0, only the active video interval can maintain the constant horizontal interval, there exist no lines with big line deviation throughout from blanking interval to active video interval.

4.8.3. Fh Control

In the Line TBC circuit, jitter (in pixel unit) in input data, during active vertical video interval shall be absorbed to FIFO line by line, and the distortion shall be accumulated in TBC FIFO. Because the accumulated distortion, going to be released during vertical blanking interval, the decoded result during active vertical video interval outputs conforming to the ITU-R BT601 and BT.656.

The XV750C is so designed as to avoid a case where TBC FIFO capacity goes short against video replayed signal and the like. However, some of the video signals easily generated might see FIFO overflow and/or underflow during its active vertical video interval.

Fh Control is to perform absorption and release of jitter distortion through FIFO memory, not only during vertical blanking but also horizontal blanking interval. Setting Fh Control on, even in the cases FIFO capacity becoming short, overflow and/or underflow can be avoided by way of adjusting the horizontal blanking intervals.

For example, in the case of NTSC video signal with a standard Fh, sampling clock count during 1 line becomes 858 at the sampling clock frequency of 13.5MHz. Usually the Line TBC of the XV750C controls per line pixel number (clock number) during active vertical video interval in such manner to match with 858 clocks. Suppose Fh of the input video signal being high, the feeding signal is of sampling clock number per line of about 857 clocks. At this time, if Fh control function is enabled, it will control in such manner as to make clock number of output data per line to be 857 automatically. This adjustment is done during horizontal blanking interval. For instance, in case of ITU-R BT.656 output mode, interval length of EAV-SAV being deviated, and out of specifications, still SAV-EAV interval can satisfy the specifications. For more details, please refer to the description on the related register FHCTLS_.

4.9. Programmable Filter

The XV750C has a built-in FIR filter of 24 taps with coefficients configurable at random. This filter enables limiting the bandwidth of luminance data. Figure 4.25 shows its filter configuration. There are 24 coefficients (b1 to b24) on this filter. By setting those coefficients, a filter with an aimed frequency response can be realized. An output coefficient (scl) also need to be set in order to keep the range of the data output value, within a certain adequate range. Since every coefficient (b1 to b24) can take any value at random, all filters can be configured such as odd-symmetric filter, even-symmetric filter and asymmetric filter etc. The coefficients b1 to b24 and scl can be set at the registers PROFLT_ADRS and PROFLT_DATA. The addresses to set the filter coefficients are not assigned to ordinary registers. By first storing addresses desired to be set, on the PROFLT_ADRS registers, and then write each coefficient value into the PROFLT_DATA registers, coefficient registers can be written.

Table 4.6 shows the correspondence between the PROFLT_ADRS values and the filter coefficients.

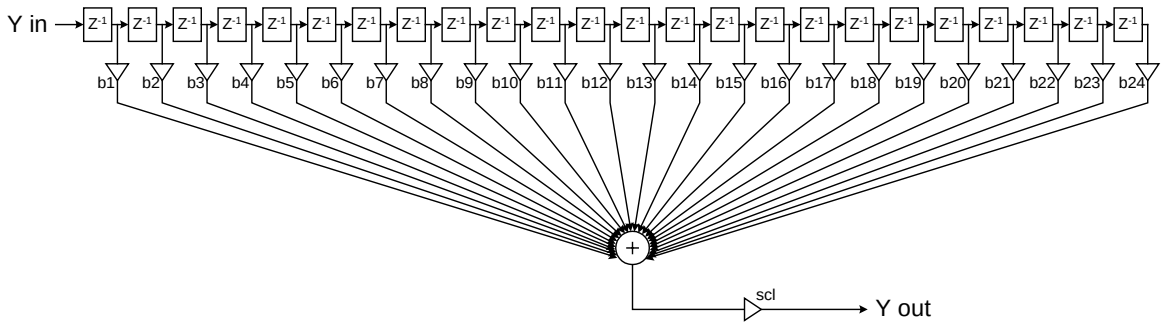


Figure 4.25 Programmable filter configuration

Table 4.6 Table of Registers for Programmable Filter

PROFLT_ADRS	PROFLT_DATA							
[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x00	b1[7:0]							
0x01	s1	0	0	0	b1[11:8]			
0x02	b2[7:0]							
0x03	s2	0	0	0	b2[11:8]			
0x04	b3[7:0]							
0x05	s3	0	0	0	b3[11:8]			
0x06	b4[7:0]							
0x07	s4	0	0	0	b4[11:8]			
0x08	b5[7:0]							
0x09	s5	0	0	0	b5[11:8]			
0x0a	b6[7:0]							
0x0b	s6	0	0	0	b6[11:8]			
0x0c	b7[7:0]							
0x0d	s7	0	0	0	b7[11:8]			
0x0e	b8[7:0]							
0x0f	s8	0	0	0	b8[11:8]			
0x10	b9[7:0]							
0x11	s9	0	0	0	b9[11:8]			
0x12	b10[7:0]							
0x13	s10	0	0	0	b10[11:8]			
0x14	b11[7:0]							
0x15	s11	0	0	0	b11[11:8]			
0x16	b12[7:0]							
0x17	s12	0	0	0	b12[11:8]			
0x18	b13[7:0]							
0x19	s13	0	0	0	b13[11:8]			
0x1a	b14[7:0]							
0x1b	s14	0	0	0	b14[11:8]			
0x1c	b15[7:0]							
0x1d	s15	0	0	0	b15[11:8]			
0x1e	b16[7:0]							
0x1f	s16	0	0	0	b16[11:8]			
0x20	b17[7:0]							
0x21	s17	0	0	0	b17[11:8]			
0x22	b18[7:0]							
0x23	s18	0	0	0	b18[11:8]			
0x24	b19[7:0]							
0x25	s19	0	0	0	b19[11:8]			
0x26	b20[7:0]							
0x27	s20	0	0	0	b20[11:8]			
0x28	b21[7:0]							
0x29	s21	0	0	0	b21[11:8]			
0x2a	b22[7:0]							
0x2b	s22	0	0	0	b22[11:8]			
0x2c	b23[7:0]							
0x2d	s23	0	0	0	b23[11:8]			
0x2e	b24[7:0]							
0x2f	s24	0	0	0	b24[11:8]			
0x30	0	0	0	0	scl[3:0]			
0x31	0	0	0	0	0	0	sv_en	dv_en

4.9.1. Filter Coefficients (b1 to b24)

Two addresses are allocated for each filter coefficient bn, where n=1 to 24, as shown in Table 1. bn [11:0] indicates the coefficient value. 1/2048 of the value set in the bn[11:0] shall be the actual coefficient value. Sn is a bit used to set the coefficient code, where Sn=0 and Sn=1 represent a positive and a negative value, respectively.

For example, to set a value of -1.25 to coefficient b1, write the registers as follows:

Write 0x00 in PROFLT_ADRS

Write 0x00 in PROFLT_DATA

Write 0x01 in PROFLT_ADRS

Write 0x8a in PROFLT_ADRS

Above steps will set a value of -1.25 to coefficient b1.

4.9.2. Output Coefficient (scl)

The relation between output coefficient set value of scl and coefficient value is given below.

Coefficient value ＝ 2^(scl-8)

The value of scl can range from zero (0) to 15.

4.9.3. Setting Filtering ON/OFF

Filtering can be enabled or disabled for SV port and DV port separately. However, since there is only one set of filter coefficients available, it is not possible to configure different filter coefficients for SV port and DV port. The filter is enabled or disabled by setting sv_ev and dv_en bits. Setting sv_ev to "1" enables filtering on SV port, and setting "0" disable it. While dv_en bit is used for the DV port likewise.

4.9.4. Delay quantity of Luminance and Chroma

Although no filtering being applied for chroma data, chroma data need to be agreeing with the data delay quantity of the luminance data. For this reason, chroma data is delayed by 12 samples. When filtering is disabled, both luminance data and chroma data will be delayed by 12 samples.

4.10. Scaling Engine

The XV750C allows scaling on output image data fed to DV port. The scaling ratio is from 1/8 to two (2) horizontally and from 1/8 to one (1) vertically. The scaling ratio can be independently set horizontally and vertically respectively.

For scaling, re-sampling process is adopted using a poly-phase filter. The XV750C can continuously (in 32 steps) vary bandwidth-limiting filter characteristics widely over the scaling range, by employing a uniquely configured bandwidth-limiting filter that prevents aliasing. For this reason, characteristics change in the bandwidth-limiting filter causes almost no changes on the image, enabling a flawless zooming while continuously changing the scaling ratio.

Since the re-sampling start-position being able to set at the unit of 1/32 pixel horizontally and 1/32 line vertically, post-scaling image can be adjusted at 1/32 pixel unit. Making use of this feature, smooth zooming become possible towards randomly chosen center point. In addition, with the function automatically shifting the vertical sampling position by 1/2 line based on the ODD/EVEN field of the input image, it is possible to generate non-interlaced image from interlaced image. Vice versa, it is also possible to generate interlaced image from non-interlaced one.

4.10.1. Vertical Scaling

1) Setting Scaling Method

There are two ways of vertical scaling. It is necessary to choose an appropriate method based on the scaling ratio required. The scaling method is going to be chosen by setting the value on the register SCALM_VFLTS.

1-1) Linear interpolation (SCALM_VFLTS =0)

Post-scaling value is going to be obtained by linear interpolation. This method is effective over all the scaling ratio, however, in order to avoid image degradation due aliasing, recommendation is given to use within the scaling ratio range from 1/2 to one (1.)

1-2) Poly-phase Filter Sampling (SCALM_VFLTS =1)

Post-scaling value is going to be obtained using a poly-phase filter. This method can only be used for the scaling ratio less than 1/2 inclusive. The image degradation due aliasing is kept minimal, since appropriate bandwidth-limiting filtering is applied corresponding to the scaling ratio. For the scaling ratio ranging from 1/8 to 1/2, the choice of this method is recommended.

2) Setting the Scaling Ratio

Setting the values of two registers VFILT_VFILT and VSCAL_VSCAL sets the scaling ratio.

The scaling ratio SV is represented by the following formula:

SV=VFILT_VFILT/VSCAL_VSCAL*512

2-1) Limitations to the setting values

There are certain limitations to the configurable values to the registers VFILT_VFILT and VSCAL_VSCAL, with the limit varying to the value of SCALM_VFLTS.

2-1-1) Limit to VFILT_VFILT

When SCALM_VFLTS =0, values 4, 8, 16 or 32 only are configurable.

When SCALM_VFLTS =1, values from 8 to 32 only are configurable.

2-1-2) Limit on VSCAL_VSCAL

When SCALM_VFLTS =0, following relation need to be satisfied.

VSCAL_VSCAL＞0x4000+(0x200*(32-VFILT_VFILT))

When SCALM_VFLTS =1, following relation need to be satisfied

VSCAL_VSCAL＞0x8000+(0x200*(32-VFILT_VFILT))

2-2) Recommended Values to be configured

Considering the limitation above and the aliasing effect caused by scaling, description is given below how to calculate the recommended values for SCALM_VFLTS, VFILT_VFILT, and VSCAL_VSCAL based on the desired scaling ratio (SV).

2-2-1) Recommended value for SCALM_VFLTS

0 for the scaling ratio of 0.5＜SV≦1

1 for the scaling ratio of SV≦0.5

2-2-2) Recommended value for VFILT_VFILT

32 for the scaling ratio of 0.5＜SV≦1: 32

The rounded-up value of 96*SV/(1+SV) for the scaling ratio of SV≦0.5

2-2-3) Recommended value for VSCAL_VSCAL

VSCAL_VSCAL is expressed in the following formula.

VSCAL_VSCAL =VFILT_VFILT *512/SV

4.10.2. Horizontal Scaling

Re-sampling using a poly-phase filter at all times, regardless of the scaling ratio, performs horizontal scaling. The image degradation caused by aliasing is kept minimal, since appropriate bandwidth-limiting filtering is performed corresponding to the scaling ratio.

1) Setting Scaling Ratio

Setting the values to the two registers HFILT_FILT and HSCAL_HSCAL, set the scaling ratio.

The scaling ratio SH is expressed by the following formula.

SH=HFILT_FILT /HSCAL_HSCAL *1024

1-1) Limitations to the setting values

There are certain limitations to the values assignable to the registers HFILT_FILT and HSCAL_HSCAL.

1-1-1) Limitations to HFILT_FILT

For the scaling ratio greater than 1, only the value of 32 is assignable.

For the scaling ratio less than 1 inclusive, only a value between 4 and 32 is assignable.

1-1-2) Limitation to HSCAL_HSCAL

If HFILT = 32, the following relation needs to be satisfied:

HSCAL_HSCAL≧0x4000

If HFILT < 32, the following relation needs to be satisfied:

HSCAL_HSCAL≧0x8000

1-2) Recommended Values to be configured

Considering the limitation above and the aliasing effect caused by scaling, description is given below how to calculate the recommended values for HFILT_FILT and HSCAL_HSCAL based on the scaling ratio (SH) desired.

1-2-1) Setting Value of HFILT_FILT

32 for the scaling ratio of 1≦SH

Rounded-up value of 32*SH for the scaling ratio of SV＜1

1-2-2) Setting Value of HSCAL_HSCAL

HSCAL_HSCAL =HFILT_FILT *1024/SH

4.10.3. Conversion between Interlaced and Non-interlaced Images

The scaler normally outputs odd-field image when odd-field is applied, and vice versa even-field when even-field is applied. Therefore, when non-interlaced image is applied, the scaler output yields non-interlaced image of only odd field or even field.

The scaling engine incorporated in the XV750C is capable of generating non-interlaced image from interlaced

image, and vice versa. These settings can be made by the registers SCALM_INTI and SCALM_INTO.

1) Setting for Interlaced to Non-interlaced

Setting SCALM_INTI=1 and SCALM_INTO=0, will make the output image all odd fields.

Given odd field input image, normal scaling being performed and odd field image output will be fed.

Given even field input image, vertical re-sampling starting position being automatically so adjusted as to position the image same with odd-field. In this manner, odd-field images can be produced from even-field image. In this setting, even if a non-interlaced image is applied, normal operation shall produce non-interlaced image output.

2) Setting for Non-interlaced input and Interlaced output

Setting SCALM_INTI=0 andSCALM_INTIO=1, odd-field and even-field are alternately repeated automatically on the output image. In this setting, the odd/even flags in the input image are ignored, and every field is treated as odd. Internally however, odd/even flag is generated and each other field alternates odd, even, odd, even. When the internal flag is even, it automatically adjusts the vertical re-sampling starting position and will produce an even field output image, shifting down a half line from the odd field output image. Please be careful, however, if an interlaced image input being fed in this setting, proper output will not be obtained.

4.10.4. Adjusting the Re-sampling Start Position

Adjustments for re-sampling start position can be done in 1/32 pixel unit horizontally and in 1/32 line unit vertically. These adjustments use registers DCROPH_CRPHS, DCROPV_CRPVS, HPHS_OFST, and VPHS_OFST. Adjustments are possible horizontally and vertically each other independently. Please note that the re-sampling start position is set as the position on the input image. Therefore, when the scaling ratio is set at 0.3 and re-sampling start position being moved by 1 pixel, the output image will move 0.3 pixel. This is because the scaling ratio of 0.3 is going to be multiplied.

1) Setting Horizontal Start Position

The registers DCROPH_CRPHS and HPHS_OFST can specify the horizontal re-sampling start position.

The re-sampling start position (HS) is expressed by the following formula.

HS=DCROPH_CRPHS *2+HPHS_OFST /32 (Unit in pixel)

For the register HPHS_OFST, any value between zero (0) and 63 is assignable but for DCROPH_CRPHS, only a value between zero (0) and 340. Because of this constraint, the re-sampling start position cannot be set close to the right edge of the input image.

2) Setting Vertical Start Position

The registers DCROPV_CRPVS and VPHS_OFST can specify the vertical re-sampling start position.

The re-sampling start position (VS) is expressed by the following formula.

VS=DCROPV_CRPVS *2 + VPHS_OFST /32 (Unit: line)

For the register VPHS any value between zero (0) and 63 is assignable, but for DCROPV_CRPVS only a value between zero (0) and 230 in case of 60Hz scanning mode, or a value between zero (0) and 280 in case of 50Hz scanning mode. Because of this constraint, the re-sampling start position cannot be set close to the bottom edge of the input image.

4.10.5. Setting the Number of Output Pixels

The numbers of both horizontal pixels and vertical lines of output image can be configurable. Making use of this function, it is possible to keep the number of output pixels constant even when the scaling ratio is varied. This will not apply, however, if the specified output pixel number and line number go beyond the effective image area.

1) Setting the Number of Output Horizontal Pixel

The register DCROPH_CRPHA defines the number of output horizontal pixel. The number of output pixel (HO) is expressed by the following formula.

HO=DCROPH_CRPHA*2

Therefore, even numbers only are configurable for the output pixel number.

Furthermore, scaling is only performed in the effective area on input image. Accordingly, the number of output pixel may become less than the value specified by DCROPH_CRPHA, depending the settings in the registers DCROPH_CRPHA,DCROPH_CRPHS and the horizontal scaling ratio. When the following equation establishes, the number of output pixels will be equal to the number set to DCROPH_CRPHA:

DCROPH_CRPHS*2+DCROPH_CRPHA*2/SH $\leqq$ 760

(Where, SH is the horizontal scaling ratio.)

2) Setting the Number of Vertical Output Lines

The register DCROPV_CRPVA defines the number of vertical output lines. The number of vertical output lines (VO) is expressed by the following equation.

VO=SCROPV_CRPVA

For the output line number, odd numbers also may be specified. However when an odd number being specified, please note that the number of lines will differ in odd-field and even-field. In this case, odd field will have one line more than even field.

In addition, scaling is only performed within the effective area of the input image, as in the horizontal scaling. Therefore, the number of output pixels may become less than the value specified by DCROPV_CRPVA, depending the settings in the registers DCROPV_CRPVA,DCROPV_CRPVS and vertical scaling ratio.

When the following equation is satisfied, output line number will meet the number set in DCROPV_CRPHV:

DCROPV_CRPVS*2+DCROPV_CRPVA/SV ≦ 496(in 60Hz scanning mode)

DCROPV_CRPVS*2+DCROPV_CRPVA/SV ≦ 600(in 50Hz scanning mode)

(Where, SV is vertical scaling ratio)

4.10.6. Re-sampling Position

Figure 4.26 shows the relation between the pixel positions in the input image and output image. The codes HS, VS, HO and VO in the figure mean as listed below.

HS: Horizontal re-sampling start position

VS: Vertical re-sampling start position

HO: Number of horizontal output pixels

VO: Number of vertical output lines

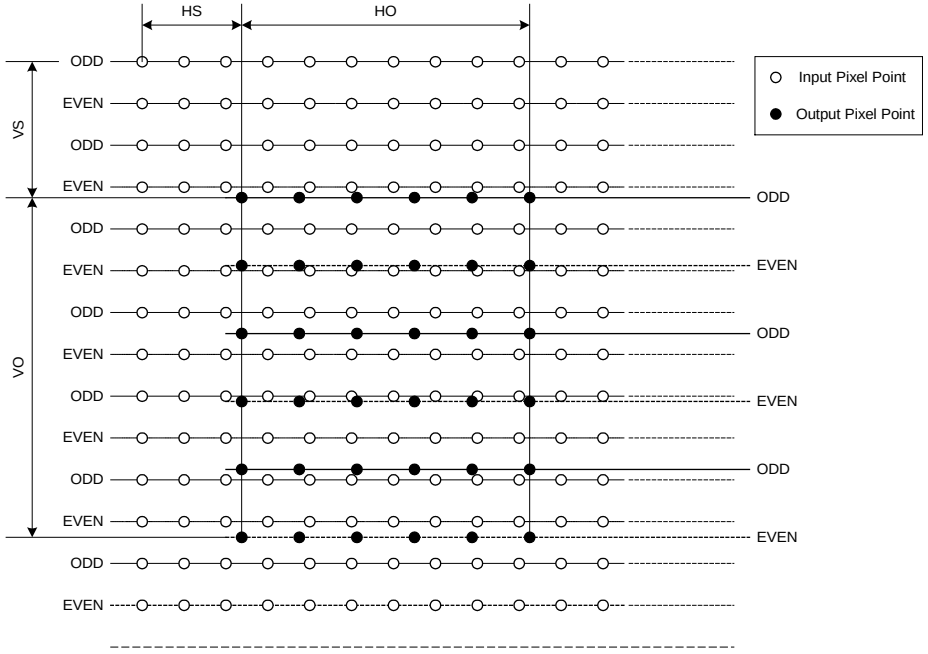


Figure 4.26 Pixel positions between input and output images.

4.11. Cropping

Cropping is the function for users to crop image at random range. For SV port output, the following two different modes are available.

Cropping mode: where the blanking signal that indicates active video interval varies in accordance with cropping.

Masking mode: where only the data is masked in accordance with cropping, while blanking signal depends on the window.

For DV port, please refer to "4.10.5. Setting the Output Pixel Number" on page 39.

The cropping area can be specified separately for SV and DV ports using the registers.

[Related registers: SCROPDEF_, SCROPH_, SCROPV_, DCROPH_, and DCROPV_]

4.12. Color Space Conversion

Color space conversion from Y, U, V to YCbCr and RGB is performed. The level of YCbCr corresponds to ITU-R. BT.601. In case of RGB, gamma correction on/off is configurable. Color space settings can be made independently for SV Line and DV Line.

Color space:

SV Line: register SVVDEF_SOLV

DV Line: register DVVDEF_DOLV

On/Off setting of RGB level and gamma correction (γ =2.2)

SV Line: register SVVDEF_SRGB

DV Line: register DVVDEF_DRGB

4.13. Video Output

The XV750C provides a SV Line that outputs video signals synchronized to the input video signal timing, and a DV Line for scaling output. DV Line output having a FIFO at the output stage, can be read out at the clock different from the internal clock used for decoding. It also provides output formatting conversion function corresponding to such like ITU-R BT.656 format.

Note:! DV Line outputs a data of an active video only. Therefore output of DV Line could not have ITU-R BT.656 format even if DV Line is a SAV/EAV addition mode.

4.13.1. Output Format

The SV Line output format is shown in Table 4.7, and the DV Line output format in Table 4.8. If the RGB output is selected as described in "4.12 Color Space Conversion" on page 41, only OUT24 or OUT24ES is effective.

Note:! Register VPDEF_MODE setting being common to SV and DV Lines, when both SV and DV Line outputs are simultaneously used, please choose "0" or "1" corresponding to the output format for the DV Line

Table 4.7 SV Line output format

Format Name	Sampling Ratio	Color Space	Description	Register		
				VPDEF_MODE	SVVDEF_S10B	SVTDEF_R656
OUT8	4:2:2	YCbCr	8bit Y/CbCr Multiplexed output	0,1	0	0
OUT10	4:2:2	YCbCr	10bit Y/CbCr Multiplexed output	0,1	1	0
OUT8ES	4:2:2	YCbCr	Format EAV and SAV are added to the 8bit Y/CbCr Multiplexed output (Equivalent to ITU-R BT.656)	0,1	0	1
OUT10ES	4:2:2	YCbCr	Format EAV and SAV are added to the 10bit Y/CbCr Multiplexed output (Equivalent to ITU-R BT.656)	0,1	1	1
OUT16	4:2:2	YCbCr	8bit Y output and CbCr output	2	0	0
OUT20	4:2:2	YCbCr	10bit Y output and CbCr output	2	1	0
OUT16ES	4:2:2	YCbCr	Format EAV and SAV are added to the 8bit Y output and CbCr output	2	0	1
OUT20ES	4:2:2	YCbCr	Format EAV and SAV are added to the 10bit Y output and CbCr output	2	1	1
OUT24	4:4:4	YCbCr, RGB	8bit Y/G, Cb/B and Cr/R output	4	0	0
OUT24ES	4:4:4	YCbCr, RGB	Format EAV and SAV are added to the 8bit Y/G, Cb/B and Cr/R output	4	0	1

Table 4.8 DV Line output format

Format Name	Sampling Ratio	Color Space	Description	Register		
				VPDEF_MODE	SVDEF_S10B	DVTDEF_R656
OUT8	4:2:2	YCbCr	8bit Y/CbCr Multiplexed output	0	d.c.	0
OUT8ES	4:2:2	YCbCr	Format SAV and EAV are added to the 8bit Y/CbCr Multiplexed output	0	d.c.	1
OUT16	4:2:2	YCbCr	8bit Y output and CbCr output	1	d.c.	0
OUT16ES	4:2:2	YCbCr	Format SAV and EAV are added to the 8bit Y and CbCr output	1	d.c.	1
OUT24	4:4:4	YCbCr, RGB	8bit Y/G, Cb/B and Cr/R output	3	d.c.	0
OUT24ES	4:4:4	YCbCr, RGB	Format SAV and EAV are added to the 8bit Y/G, Cb/B and Cr/R output	3	d.c.	1

For the meaning of output signal names, please refer to Table 4.9. Table 4.10 shows the output signal names and the data streams for each output format.

Table 4.9 Output signal names

Signal Name	Output Port System	Sampling Ratio	Bit Width	Description
SYC	SV	4:2:2	10 or 8	Y/CbCr multiplexed data
SY	SV	4:2:2 or 4:4:4	10 or 8	Y data (8bitonly when 4:4:4)
SC	SV	4:2:2	10 or 8	CbCr data
SCb	SV	4:4:4	8	Cb data
SCr	SV	4:4:4	8	Cr data
SG	SV	4:4:4	8	G data
SB	SV	4:4:4	8	B data
SR	SV	4:4:4	8	R data
DYC	DV	4:2:2	8	Y/CbCr multiplexed data
DY	DV	4:2:2 or 4:4:4	8	Y data
DC	DV	4:2:2	8	CbCr data
DCb	DV	4:4:4	8	Cb data
DCr	DV	4:4:4	8	Cr data
DG	DV	4:4:4	8	G data
DB	DV	4:4:4	8	B data
DR	DV	4:4:4	8	R data

Table 4.10 Output format and output signal name

27MHz Timeslot	OUT8/OUT10	OUT16/OUT20		OUT24		
	SYC	SY	SC	SY/SG	SCb/SB	SCr/SR
0	Cb0	Y0	Cb0	Y0/G0	Cb0/B0	Cr0/R0
1	Y0					
2	Cr0	Y1	Cr0	Y1/G1	Cb1/B1	Cr1/R1
3	Y1					
4	Cb2	Y2	Cb2	Y2/G2	Cb2/B2	Cr2/R2
5	Y2					
6	Cr2	Y3	Cr2	Y3/G3	Cb3/B3	Cr3/R3
7	Y3					
⋮	⋮	⋮	⋮	⋮	⋮	⋮
2n	Cb(n)	Y(n)	Cb(n)	Y(n)/G(n)	Cb(n)/B(n)	Cr(n)/R(n)
2n+1	Y(n)					
2n+2	Cr(n)	Y(n+1)	Cr(n)	Y(n+1/G(n+1)	Cb(n+1)/B(n+1)	Cr(n+1)/R(n+1)
2n+3	Y(n+1)					

←Output Format
←Output Signal Name

4.13.2. Video Port Interface

The video data output in its data output configuration to DVO port and SVO port, differs to the register settings. Table 4.11 indicates the relations among output signal names, SVO pins and DVO pins in each output format. As to the meaning of each output signal name used in the table, please refer to Table 4.9. Please also note that the registers relevant to the modes of video ports are VPDEF_MODE and SVVDEF_S10B, among those concerned with the output format.

Table 4.11 Video port modes

REGISTER		PORT																								
VPDEF_MODE	SVVDEF_S10B	SVO										DVO														
[2:0]		9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	SYC[7:0]										DYC[7:0]															
	1	SYC[9:0]										DYC[7:0]															
1	0	SYC[7:0]										DY[7:0]								DC[7:0]							
	1	SYC[9:0]										DY[7:0]								DC[7:0]							
2	0	SY[7:0]										SC[7:0]															
	1	SY[9:0]										SC[9:0]															
3	0	DR/DCr[7:0]										DG/DY[7:0]								DB/DCb[7:0]							
	1	DR/DCr[7:0]										DG/DY[7:0]								DB/DCb[7:0]							
4	0	SG/SY[7:0]										SB/SCb[7:0]								SR/SCr[7:0]							
		SG/SY[7:0]										SB/SCb[7:0]								SR/SCr[7:0]							

4.13.3. FIFO for DV Port

There is a FIFO provided for data output at DV port.

It is 32 stages deep and write-side uses mains 27MHz (13.5MHz) line, while read-side is read at the speed corresponding to the clock being used for input/output at the DCK port. (The maximum clock frequency to be supplied to DCK is 54MHz.)

At the FIFO read-out, timing signal necessary for the DV port is generated, corresponding to the readout clock and the mode.

As to the output timing chart, please refer to “Timing Generation Circuit” on page 49.

4.13.4. ITU-R BT.656 Output

The output formats OUT8ES and OUT10ES are equivalent to ITU-R BT.656.[5] However, if the input video signal is non-standard or decoding on free-running clock, such things are thought to happen as the pixel number may deviate from the standard or the line number may fluctuate. In terms of the number of lines, the XV750C will produce output in accordance to the input video signals. In terms of pixel number deviation, the output is given in such manner as the deviation happens during the EAV-SAV period in the vertical blanking-interval. This action may slightly differ by the settings of the TBC mode [register TBCDEF_MOD].

[5] Only for SV Line output
Refer to 4.13.5 in case of DV

Figure 4.27 shows the operation in TBC mode 0, and Figure 4.28 shows the operation in TBC mode 1.

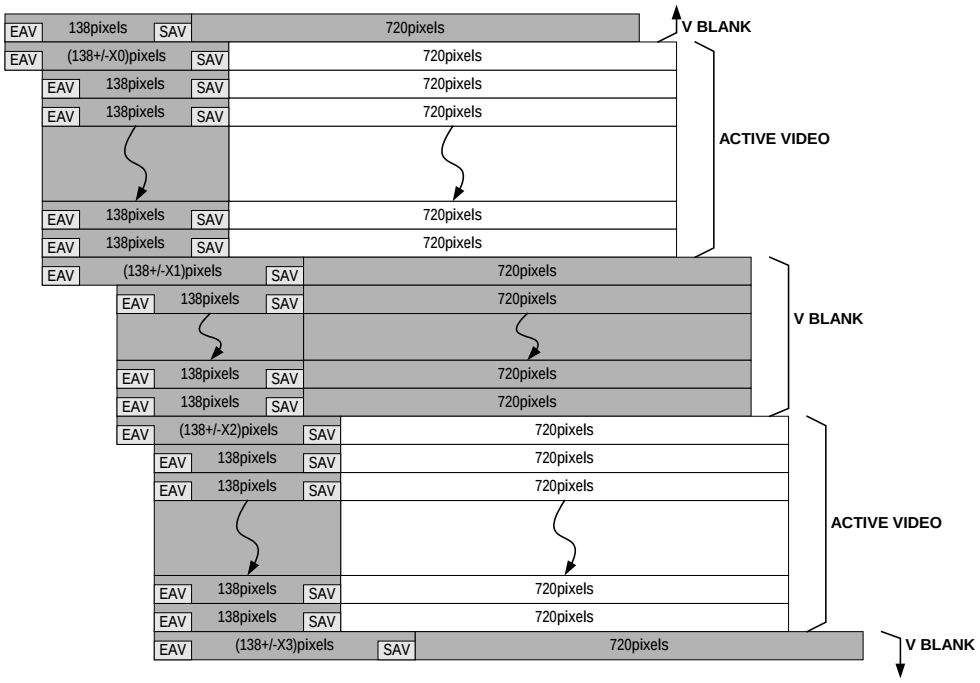


Figure 4.27 BT.656 output (TBC mode 0)

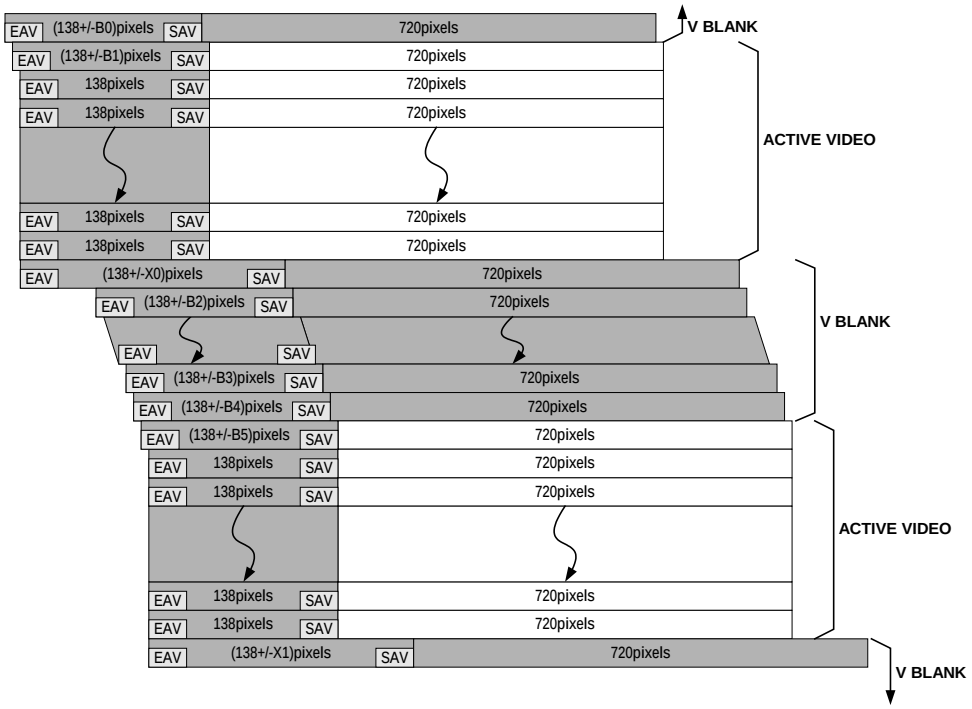


Figure 4.28 BT.656 output (TBC mode 1)

4.13.5. DV output with EAV and SAV code

The output formats OUT8ES and OUT10ES of DV output is shown in Figure 4.29.

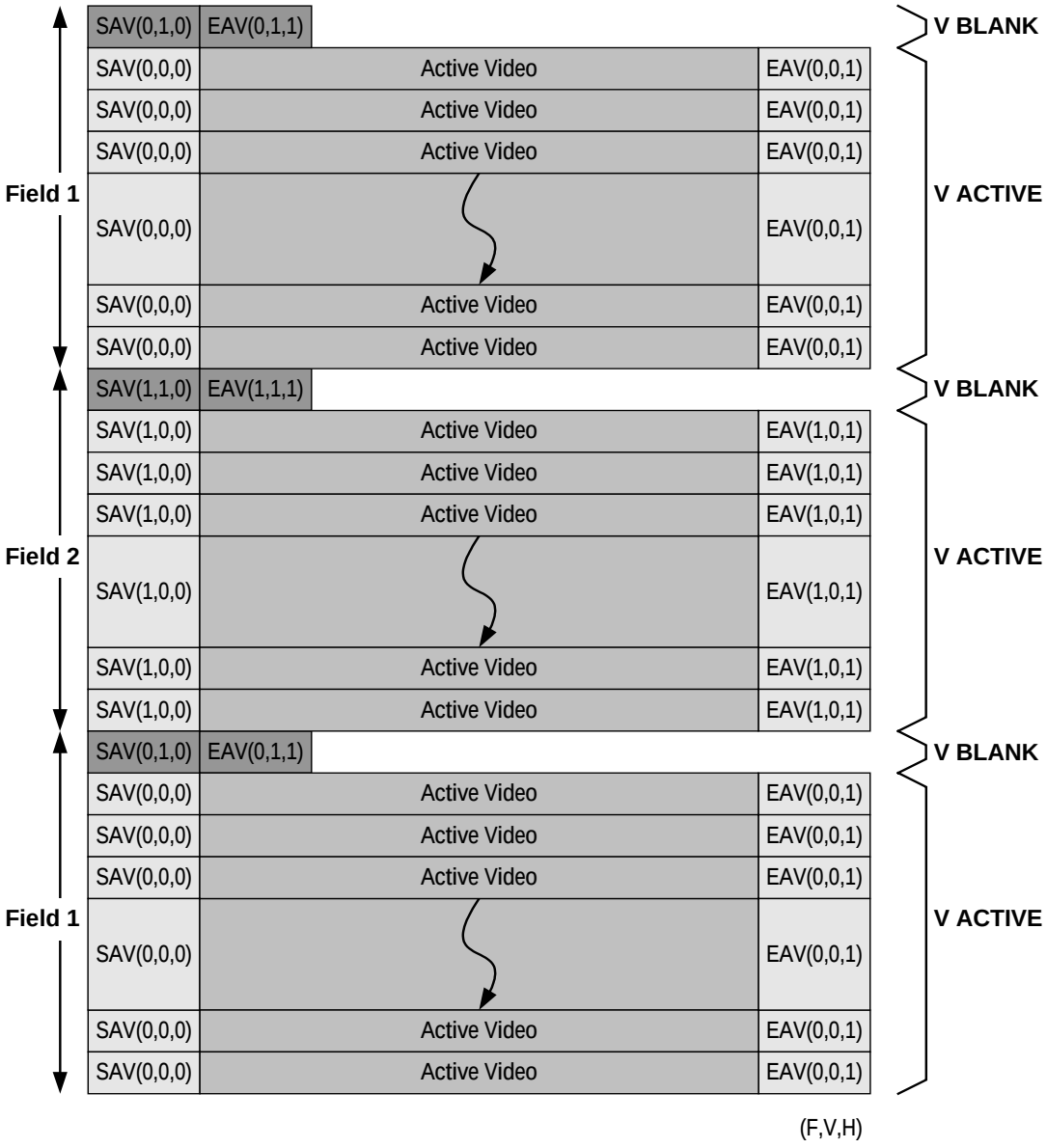


Figure 4.29 DV output with EAV and SAV

4.14. Sync Separation Circuit

This circuit separating the sync signal from the input video signal, generates various timing signals used internally.

4.14.1. Self-running Sync

The XV750C can self-produce output sync signal, synchronizing to the input video signal sync and output in line with the timing corresponding to the image decoded. When however, in such case as unstable input signal suddenly fluctuating sync position, dropping of sync and missing of sync due to noise, the XV750C will complement such sync and output. Later when the signal becomes stable, sync output resumes to synchronize to the input signal. In case when such unstable condition continues, it will switch over to self-running mode. The conditions for switching over to the self-running mode and the video output under self-running can be changed by setting the register BBDEF_MOD. In the default setting, the XV750C will output blue-back when it cannot detect the sync.

4.15. Timing Generation Circuit

This circuit generates from the separated sync signal, various timing signals for external output use, synchronized to the output image.

4.15.1. Timing Output Pins

The outputs are such various timing signals as video sync signals synchronized to SV-line output data, and DV-line output data. Table 4.12 indicates the relation between the timing-signal output pins and the output-timing signals. Each pin name is shown with the register names used to specify corresponding timing signal (As to SCK, SHS, SVS, SHB and SVB registers can not change output timing signal.)

For instance, in order to give VBI Path Through data output interval signal (VBI Term) at SFLD port, '1' shall be written into register SVCDEF_SFLDS.

Table 4.12-1 Timing output pins (1)

PORT	SCK	SHS	SVS	SHB	SVB
	SCK Output	H Sync	V Sync	H Blank	V Blank

Table 4.12-2 Timing output pins (2)

PORT	SFLD	SCBF	DGHP	DGVP	DGP0
REGISTER	SVCDEF_SFLDS	SVCDEF_SCBFS	DVCDEF_DGHP	DVCDEF_DGVP	DVCDEF_DGP0
0	Field ID	CB Flag	H End (DHEND)	V End (DVEND)	H Blank (DHB)
1	VBI Term	VBI Term	H Blank (DHB)	V Blank (DVB)	Field ID (DFLD)
2	SHB & SVB	SHB & SVB			CB Flag (DCBF)
3	SHS & SVS	SHS & SVS			VBI Term (DVBI)
4	SVS	SVS			DV FIFO not Empty
5	Field ID (Alternated)	Field ID (Alternated)			DV FIFO Almost Empty
6	Color Field Reset	Color Field Reset			DV FIFO Almost Full
7	Color Field Strobe	Color Field Strobe			DV FIFO Full

Table 4.12-3 Timing output pins (3)

PORT	DGP1	DPIO8 (DGP2)	DPIO9 (DGP3)	DCK	DVAL
REGISTER	DVGDEF_DGP1	DVGDEF_DGP2	DVGDEF_DGP3	DVCDEF_DCKS	DVCDEF_DVALG
0	H Blank (DHB)	H Blank (DHB)	H Blank (DHB)	DCK Output	Data Valid
1	Field ID (DFLD)	Field ID (DFLD)	Field ID (DFLD)	DCK Input	DCK & Data Valid
2	CB Flag (DCBF)	CB Flag (DCBF)	CB Flag (DCBF)		
3	ANC Term (DANC)	SAVEAV Term (DS AVEAV)	ANC Term (DANC)		
4	DV FIFO not Empty	DV FIFO not Empty	DV FIFO not Empty		
5	DV FIFO Almost Empty	DV FIFO Almost Empty	DV FIFO Almost Empty		
6	DV FIFO Almost Full	DV FIFO Almost Full	DV FIFO Almost Full		
7	DV FIFO Full	DV FIFO Full	DV FIFO Full		

In addition, the polarity of the following signals can be inverted by register settings.

Registers SVPOL_ SCK, SFLD, SCBF, SVB, SHB, SVS and SHS

Registers DVPOL_ DCK, DTRDY, DVAL, DGP1, DGP0, DGVP and DGHP

4.15.2. Vertical Timing

Figure 4.30 and Figure 4.31 indicate the vertical timing when the vertical frequency is 60Hz and 50Hz, respectively. The input video signal is fed out with approximate 2.5 H delay. In case of DV Line output, the output timing might differ according to the scaling ratio.

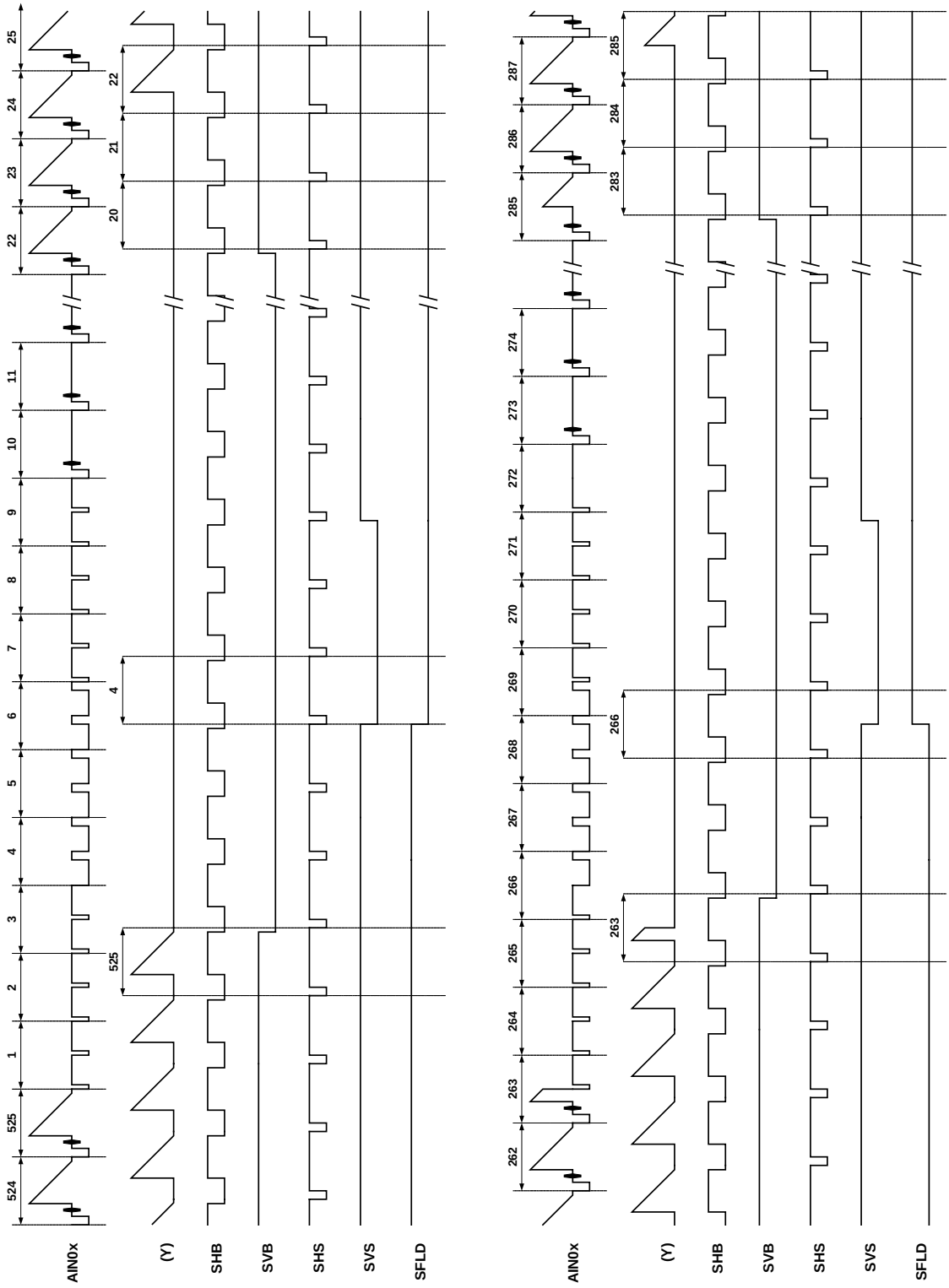


Figure 4.30 60Hz Vertical timing

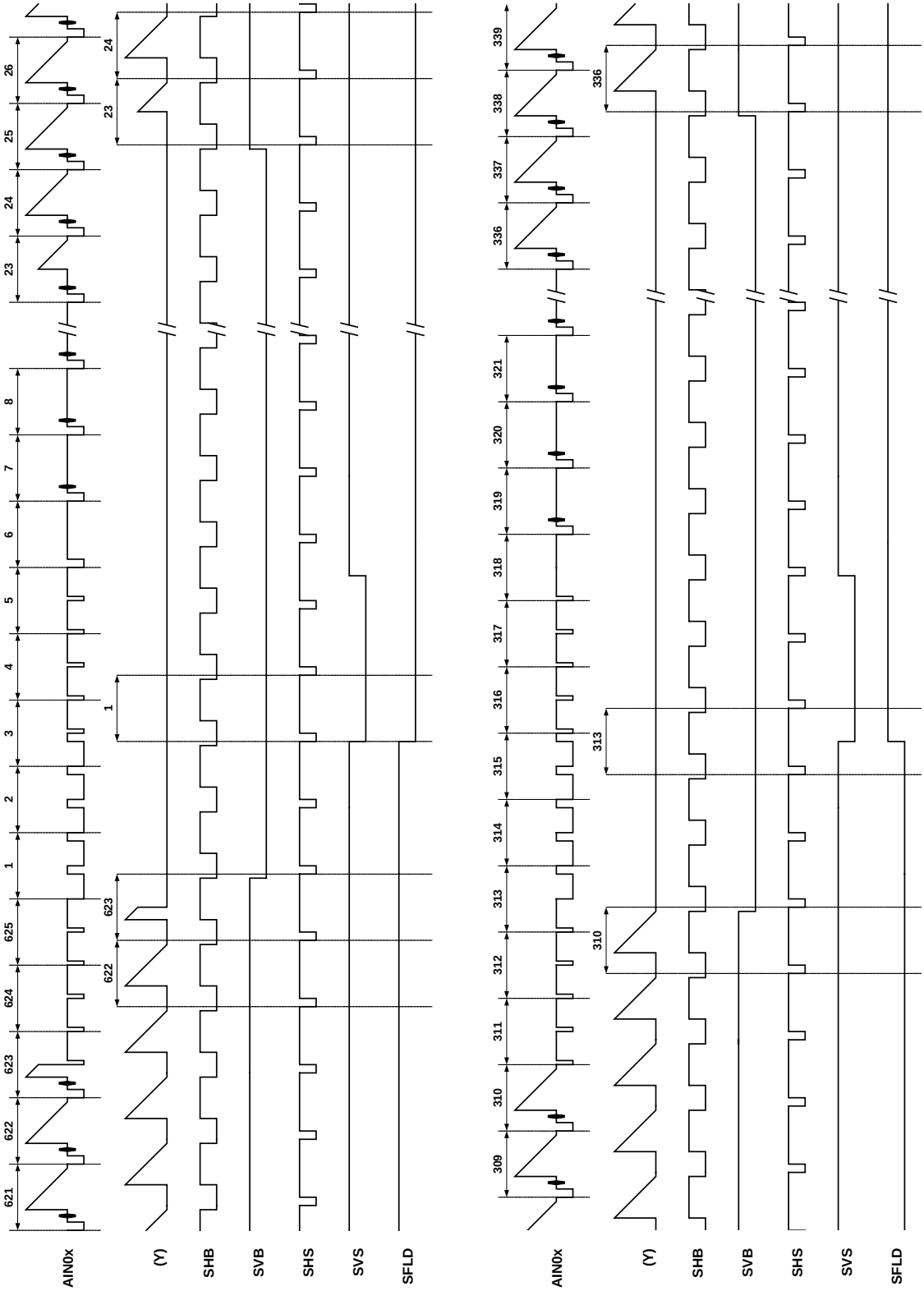


Figure 4.31 50Hz Vertical timing

4.15.3. SV Port Horizontal Timing

Figure 4.32 and Figure 4.33 indicate the SV port output video signal interface timings when the video port mode (register VPDEF_MODE) is ”0” or ”1”. Figure 4.34 and Figure 4.35 show the details in the neighborhood of SAV and EAV.

Note! The figures are for the 8-bit mode (**SVVDEF_S10B="0"**)

HSW=60

HDLY=122(fv=60Hz), HDLY=132(fv=50Hz)

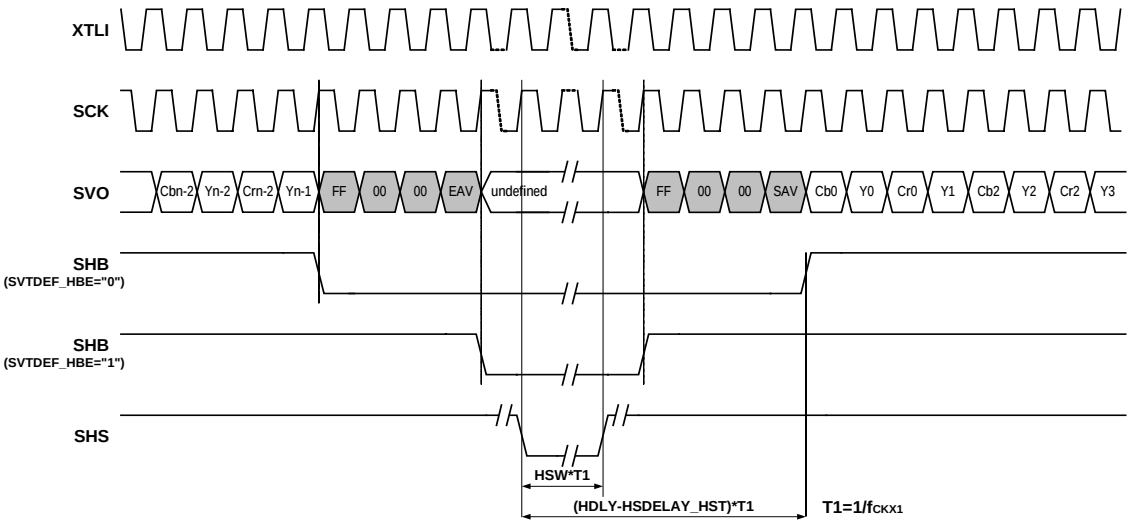


Figure 4.32 SV port Horizontal timing (SVTDEF_R656:1 /VPDEF_MODE:0 or1)

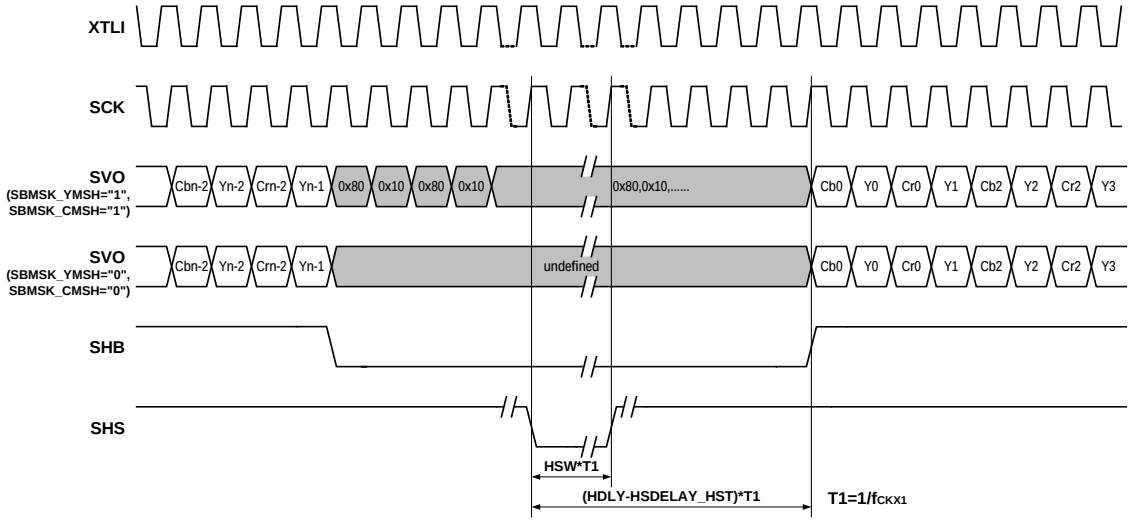


Figure 4.33 SV port Horizontal timing (SVTDEF_R656:0 /VPDEF_MODE:0 or1)

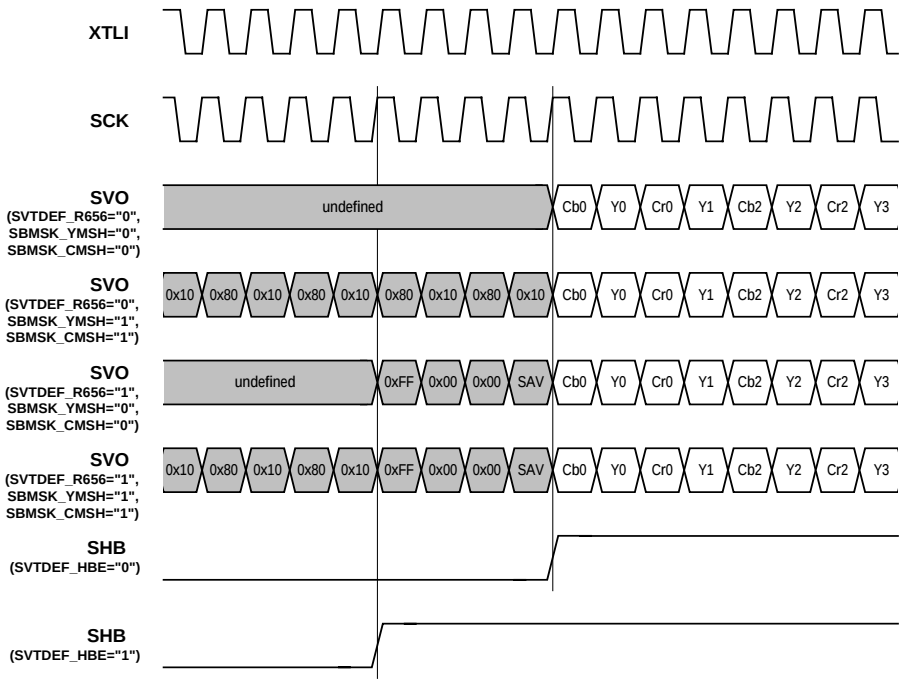


Figure 4.34 SV port SAV timing (VPDEF_MODE:0 or 1)

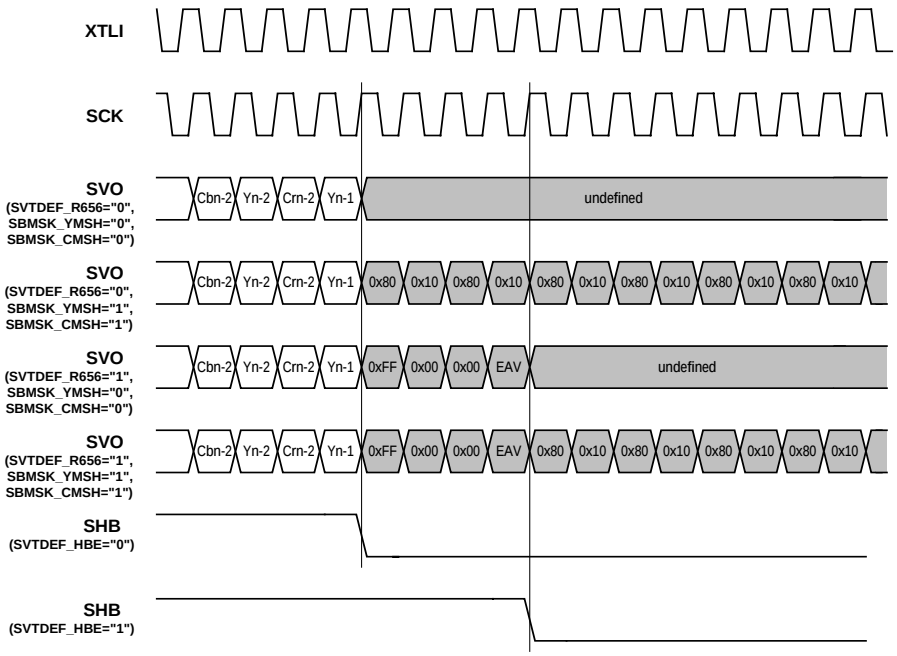


Figure 4.35 SV port EAV timing (VPDEF_MODE:0 or1)

The SV port output video signal interface timing of SAV in Figure 4.36 and of EAV in Figure 4.37 are shown respectively, when the video port mode (register VPDEF_MODE) is ”2”.

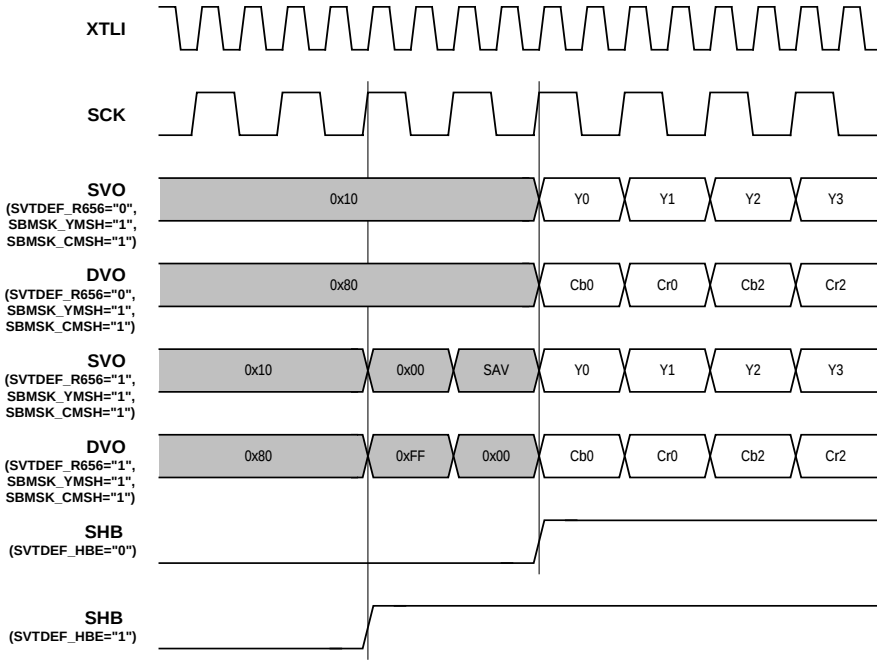


Figure 4.36 SV port SAV timing (VPDEF_MODE2)

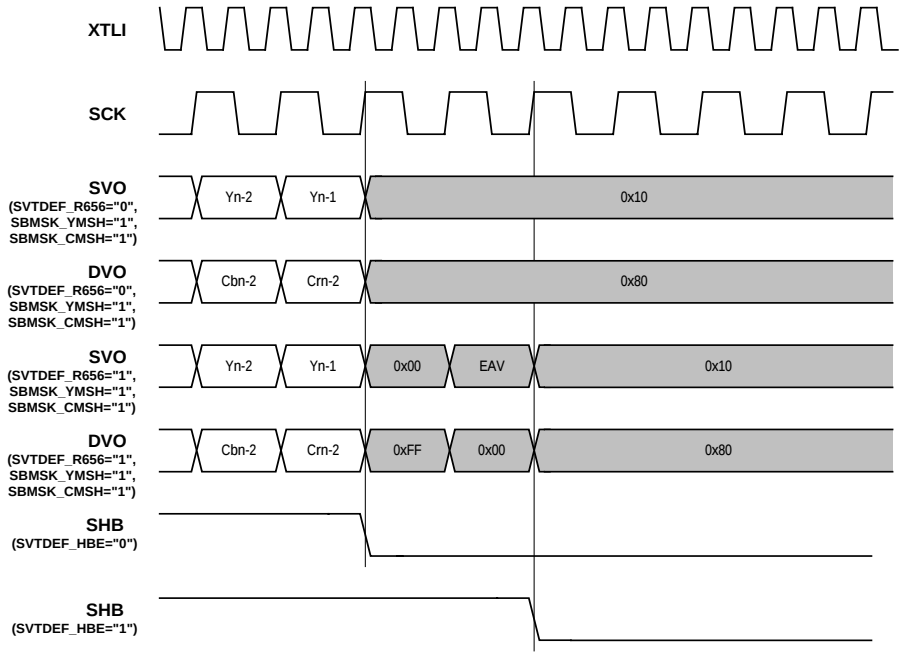


Figure 4.37 SV port EAV timing (VPDEF_MODE:2)

Figure 4.38 and Figure 4.39 indicate the interface timing of SV port Y/Cb/Cr output video signal SAV and EAV, respectively, when the video port mode (register VPDEF_MODE) is ” 4”.

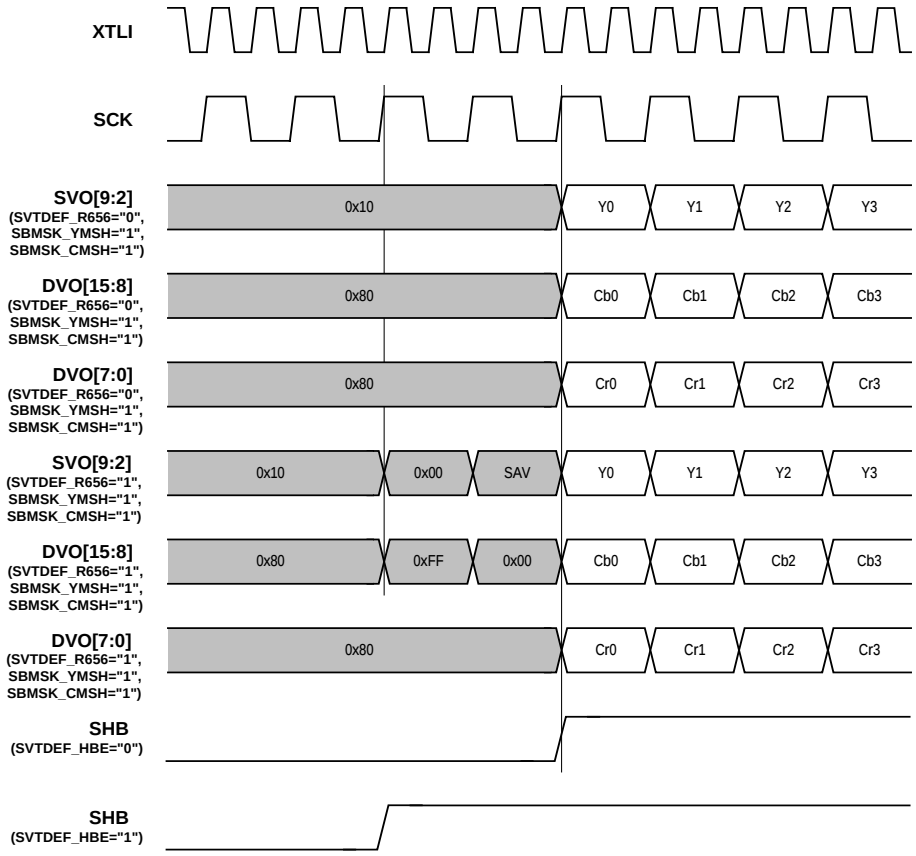


Figure 4.38 SV port SAV timing (VPDEF_MODE:4, SVVDEF_SOLV:0)

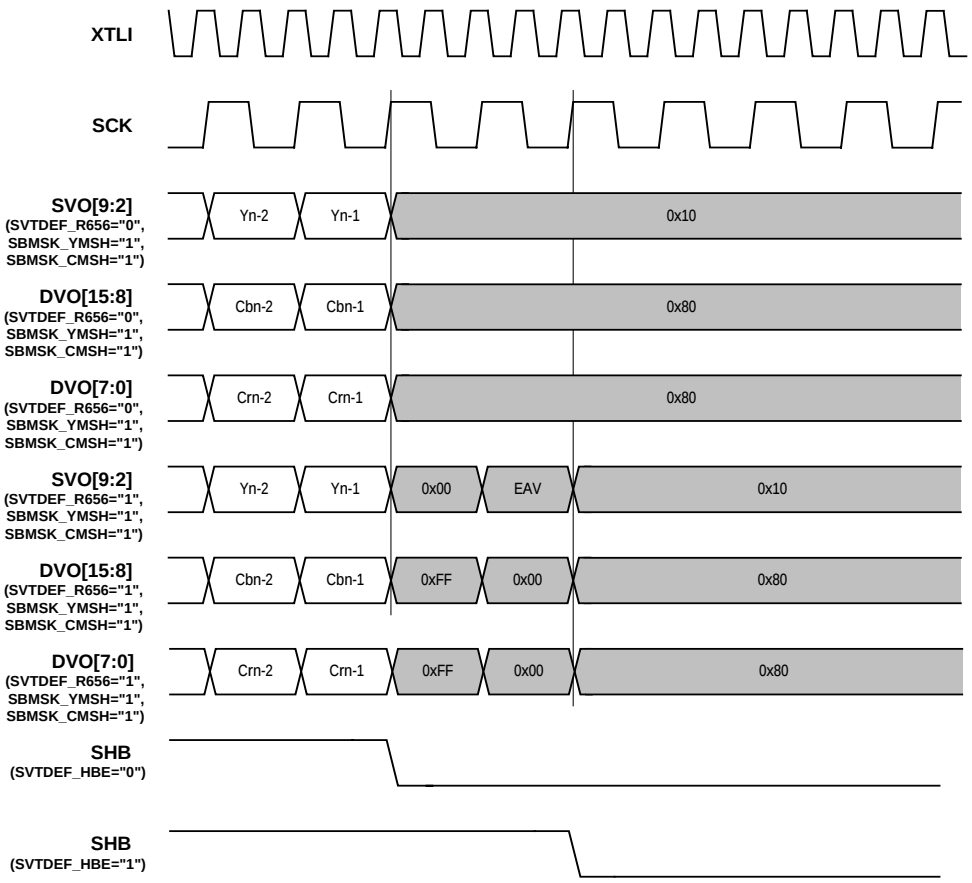


Figure 4.39 SV port EAV timing (VPDEF_MODE:4, SVVDEF_SOLV:0)

Figure 4.40 and Figure 4.41 indicate the SV port RGB output image-signal interface timing SAV and EAV, respectively, when the video port mode (register VPDEF_MODE) is ” 4”

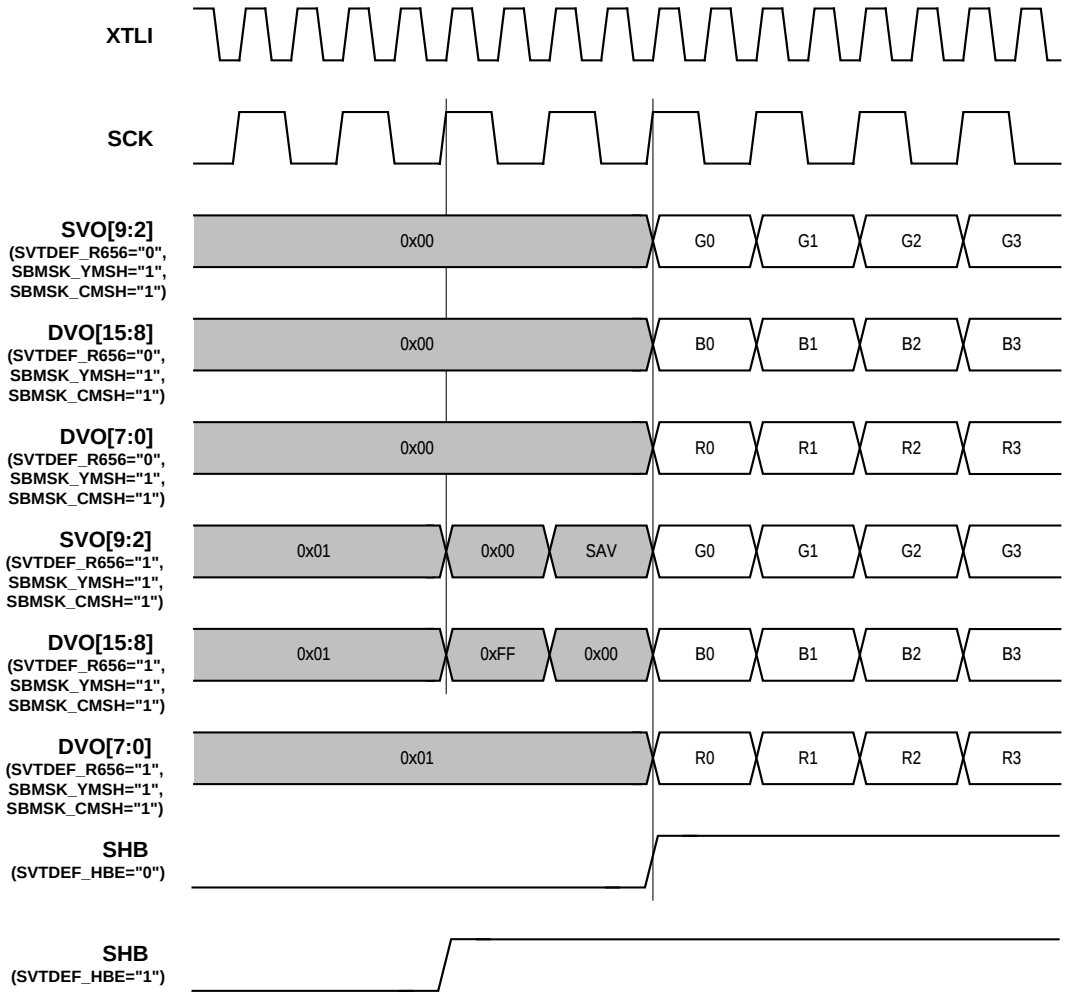


Figure 4.40 SV port SAV timing (VPDEF_MODE:4, SVVDEF_SOLV:2)

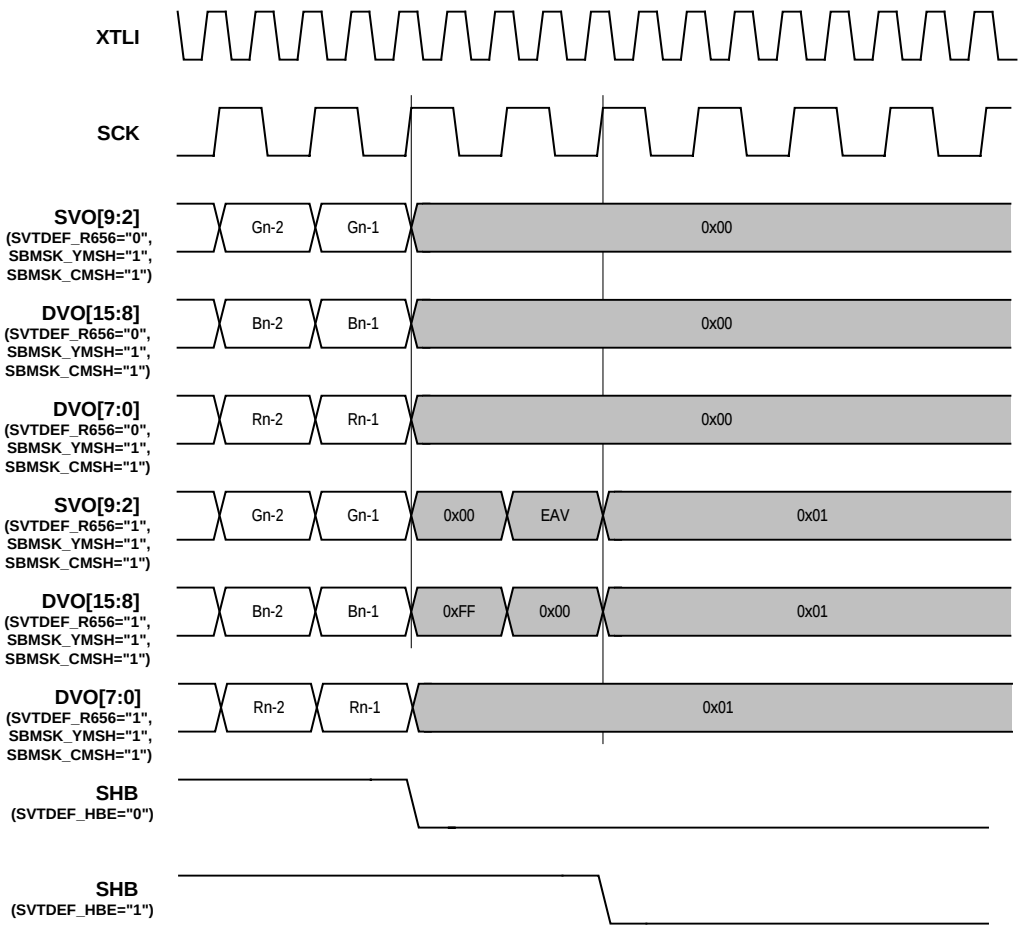


Figure 4.41 SV port EAV timing (VPDEF_MODE:4, SVVDEF_SOLV:2)

4.15.4. SV Port Control Signal Timing

Figure 4.42 indicates the timing relation among Hsync (SHS port), Vsync (SVS port) and the Field ID (SFLD port), and the timing between the Hblank (SHB port) and Vblank (SVB port), on the SV port.

The fixed delay from the first Hsync of odd field to the Vsync:

HVDLYO=0

The fixed delay from the first Hsync of even field to the Vsync:

HVDLYE=429(fv=60Hz), HVDLYE=432(fv=50Hz)

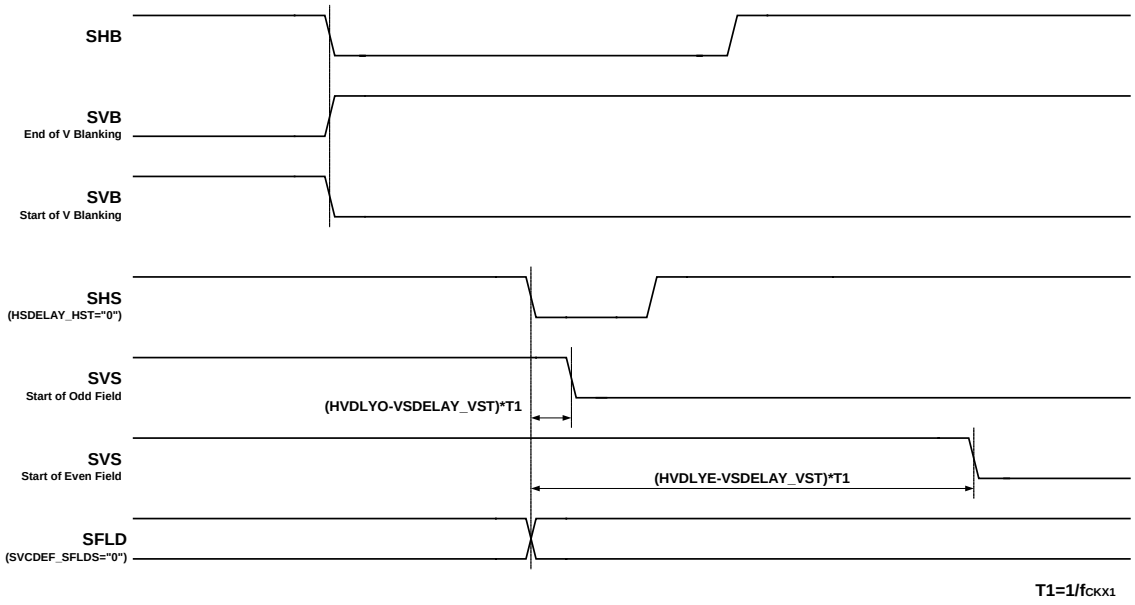


Figure 4.42 SV port H-V timing

In addition, Figure 4.43 shows the timing of the SCBF/SFLD ports.

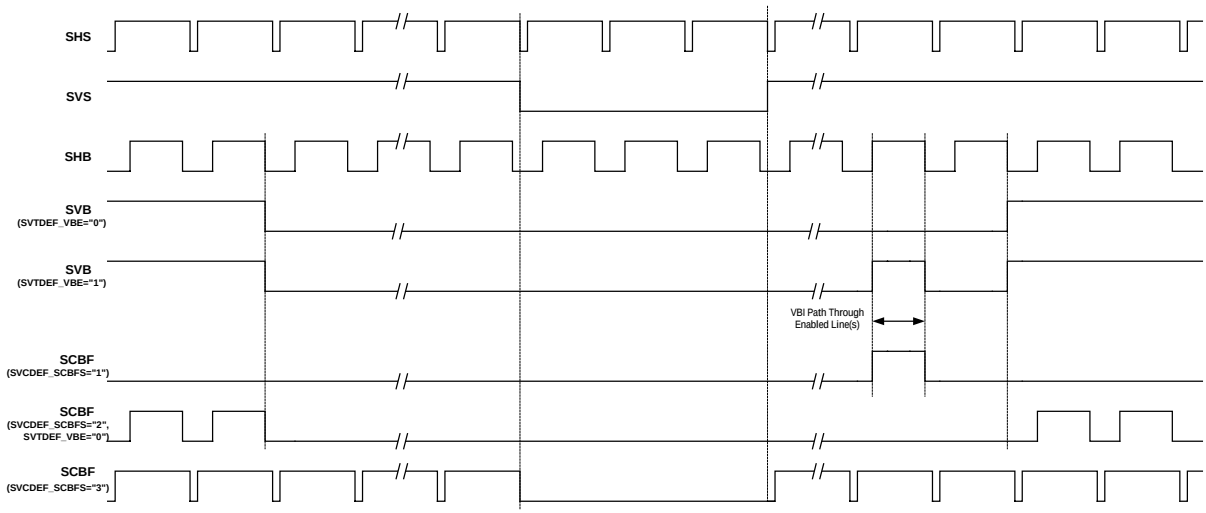


Figure 4.43 SV port SCBF/SFLD pin timing

4.15.5. DV port Horizontal Timing

The DV port output video signal interface timings shown in Figure 4.44 and Figure 4.45 for the case with video port mode (register VPDEF_MODE) set to ”0”, in Figure 4.46 and Figure 4.47 for the case with ”1”, and in Figure 4.48 and Figure 4.49 for the case with “3”. Figure 4.50 shows the timing of the Target Ready signal on the DV port.

Note:! DV Line outputs a data of an active video only.

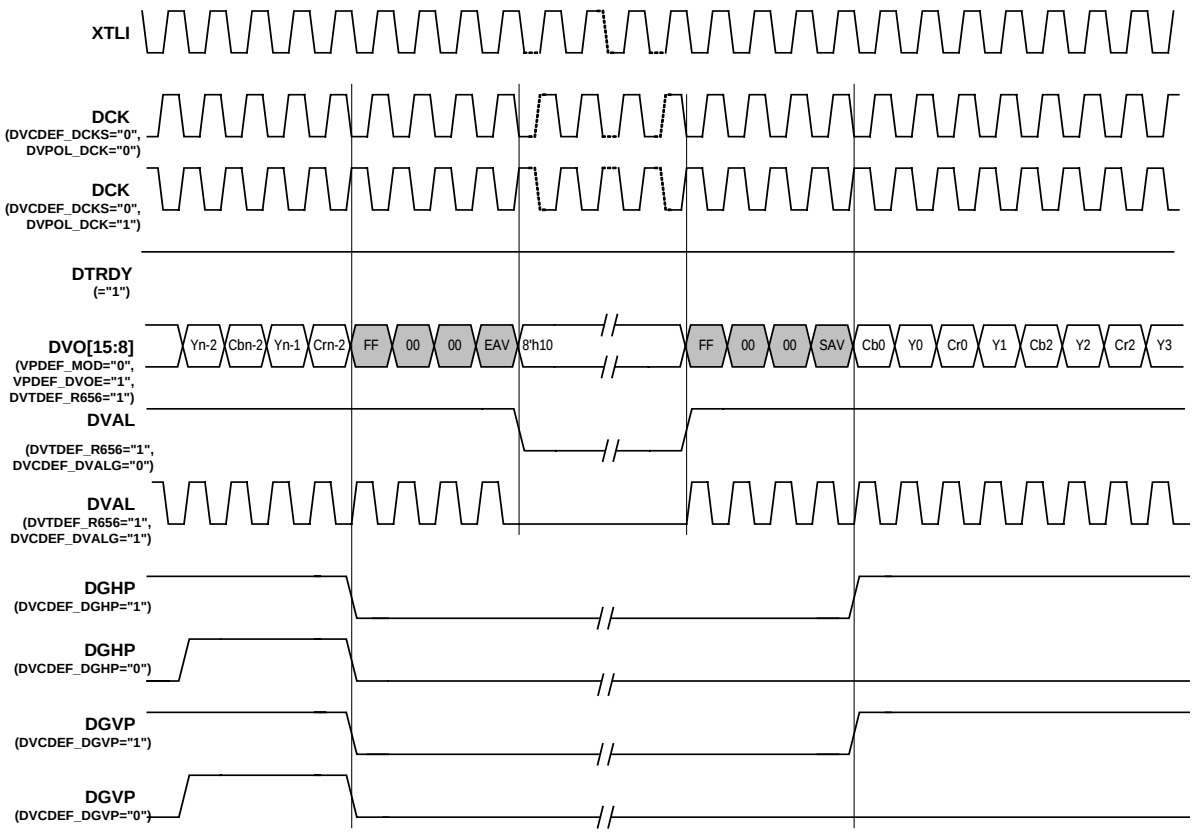


Figure 4.44 DV port Horizontal timing (DVTDEF_R656:1 /VPDEF_MODE:0)

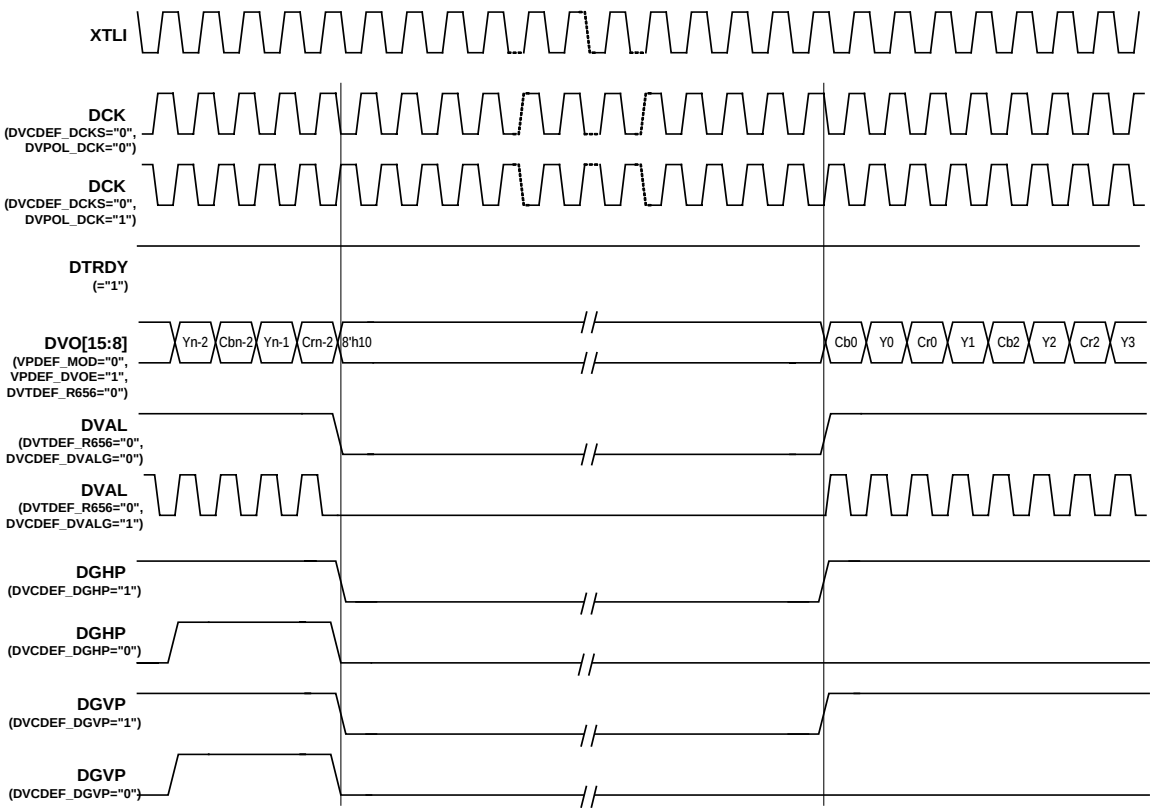


Figure 4.45 DV port Horizontal timing (DVTDEF_R656:0 /VPDEF_MODE:0)

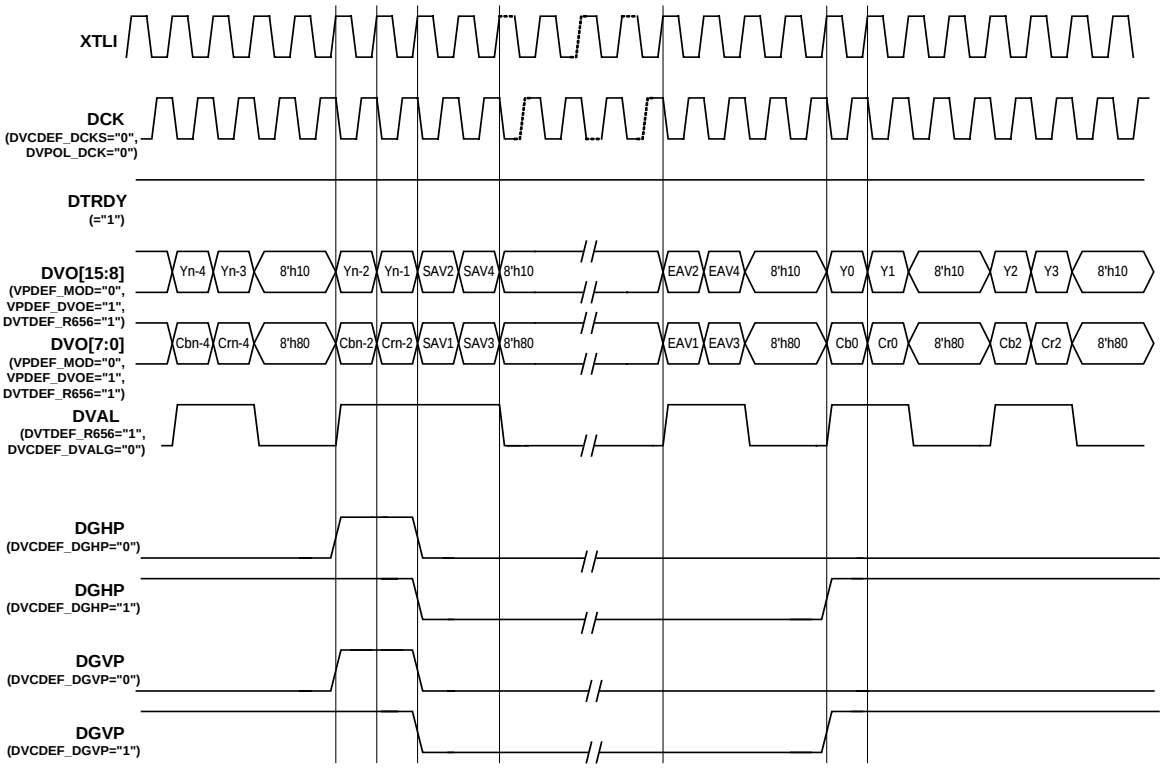


Figure 4.46 DV port Horizontal timing (DVTDEF_R656:1 /VPDEF_MODE:1)

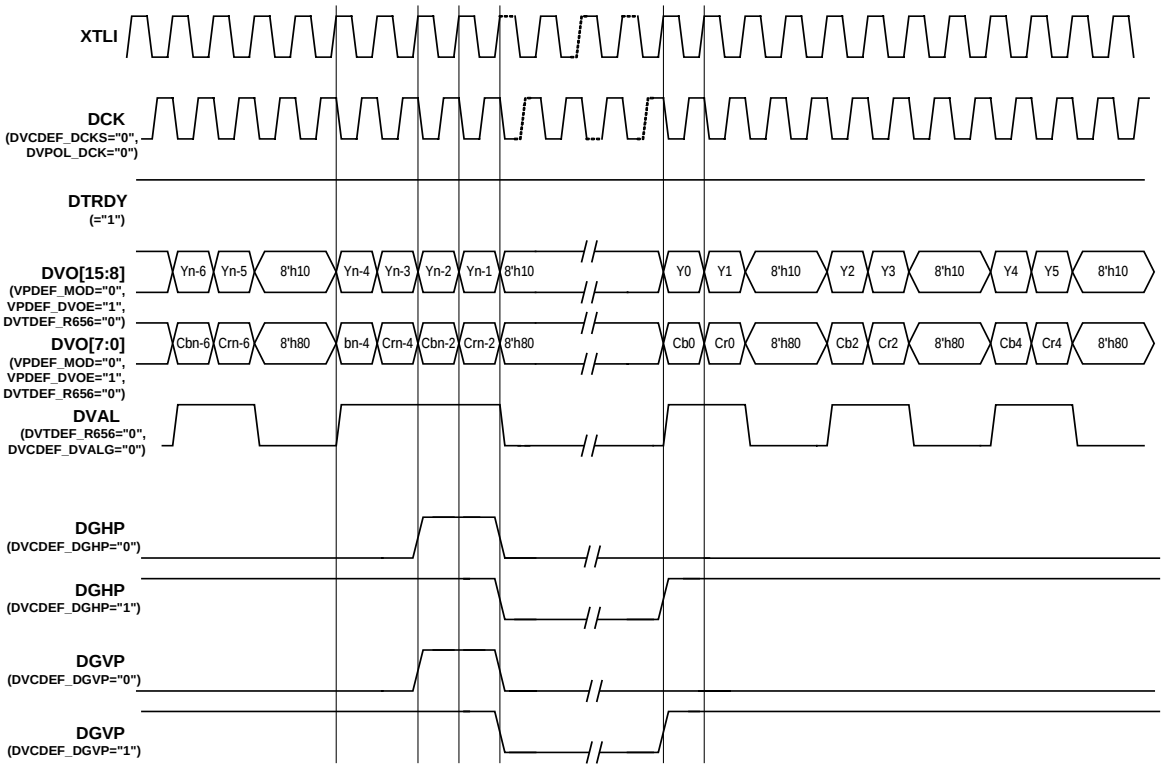


Figure 4.47 DV port Horizontal timing (DVTDEF_R656:0 /VPDEF_MODE:1)

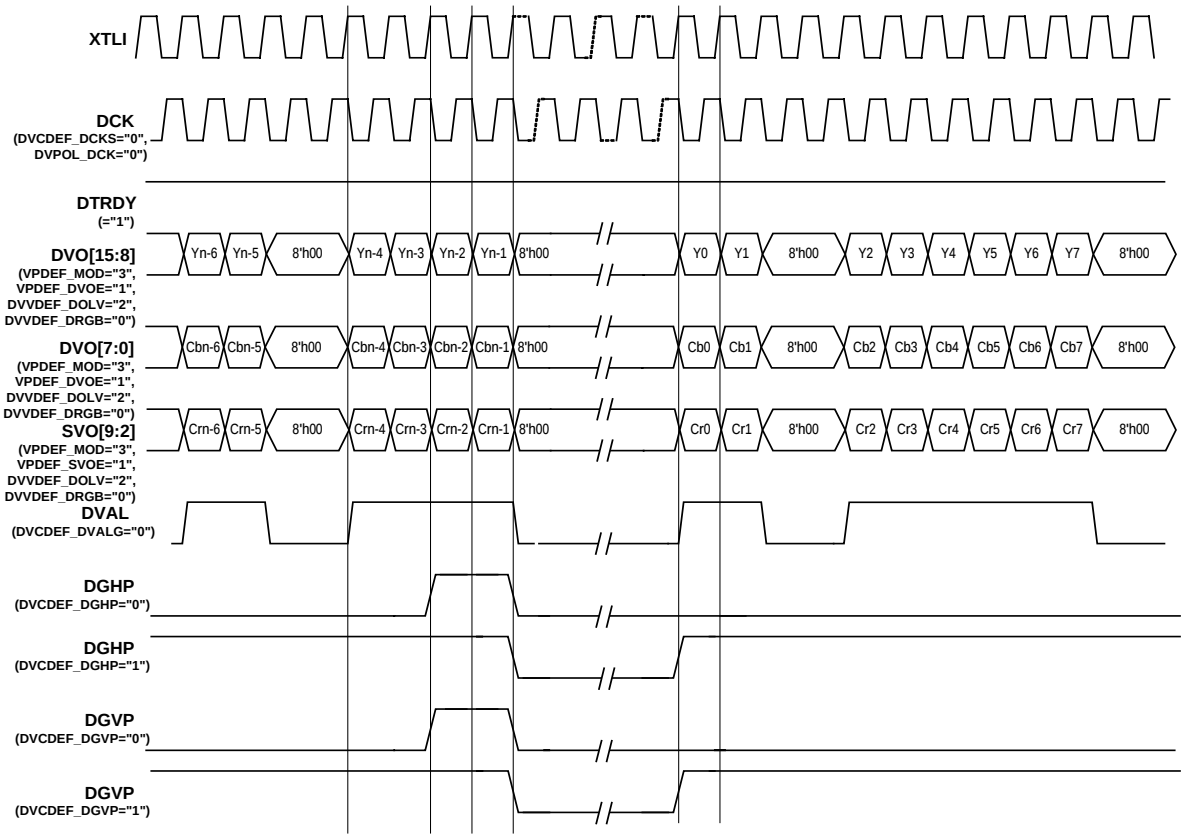


Figure 4.48 DV port Horizontal timing (DVTDEF_R656:0 /VPDEF_MODE:3 /DVVDEF_DOLV:0)

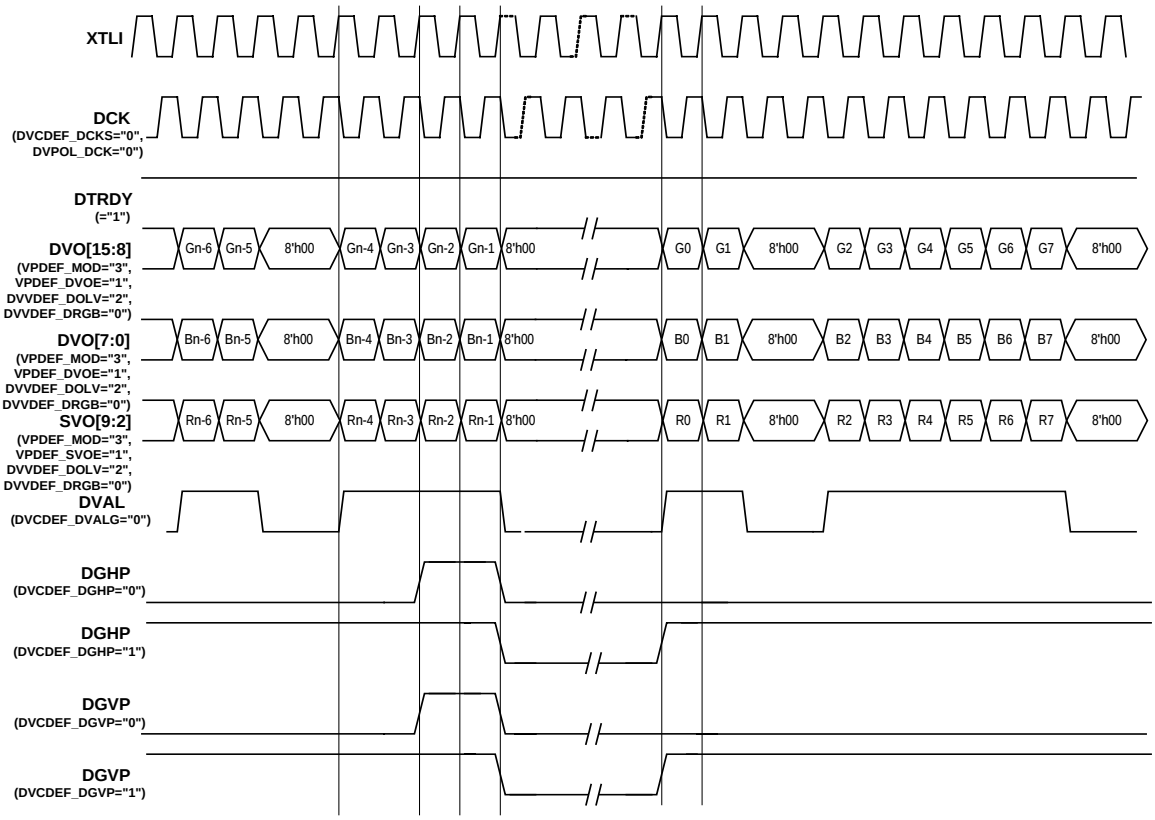


Figure 4.49 DV port Horizontal timing (DVTDEF_R656:0 /VPDEF_MODE:3 /DVVDEF_DOLV:2)

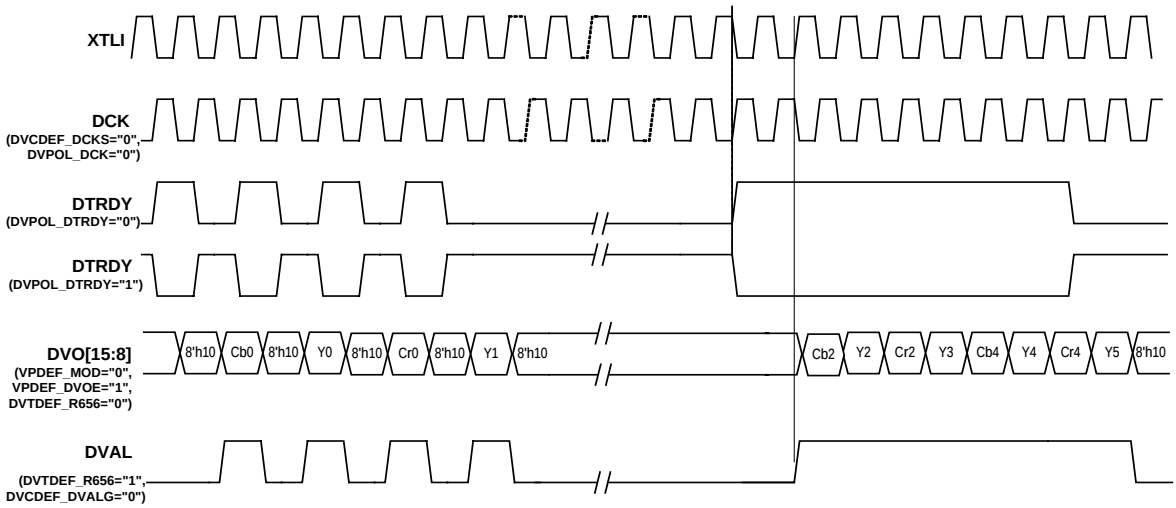


Figure 4.50 DV port Target Ready signal

4.16. Color Killer Feature

4.16.1. Color Killer Factors

The color killer works under the logical OR condition of the following two factors:

1: BL (Burst Level) Color killer

Color killer that works when the color-burst level goes lower than the preset level.

(Presetting level using registers CKILLS_ALEV and CKILLS_RLEV)

2: VS (Video Standard) Color killer

Color killer that works when input video signal not found among the configured video standards. However, this is not applicable if the automatic video standard automatic switching mode set to “Manual”.

(For the video standard setting, please refer to the register ATVM_VSTD)

4.16.2. Color Killing

Color killer factors taking place, either of the followings works depending on register setting at CKILLS_MOD:

- Bypassing YC separation circuit.

-Chrominance signal forced off.

4.17. Video Standard Detection/Automatic Switching Circuit

The XV750C is able to detect the following input video systems of the input vide signals, and automatically switches over to the detected system.

- NTSC-Jpn, NTSC-M
- NTSC-4.43
- PAL-B, D, G, H, I, PAL-N
- PAL-M
- PAL-CombinationN
- PAL-60
- SECAM

Since judgment is not automatic on the setup mode, the distinction between NTSC-M and NTSC-Japan in the above (1), PAL-B, D, G, H, I and PAL-N in the above (3) is determined by specifying whether the setup exists in the register MNVM_MOD [7:5]. For PAL-M in the above (4), setup is usually on, but off also can be configured. The video mode judgment result can be confirmed by the register VMJDG_.

4.17.1. Video Standard Automatic Switching Mode

The following 4 operation modes are selectable by the register settings on ATVM_.

Manual:

By setting color sub-carrier frequency (Fsc Mode), color modulation (Color Mode) and scan (Scan Mode), on the register MNVM_MOD, video mode can be forcedly configured.

Single Auto:

A single video mode can be specified. Detecting video mode other than the specified, color killer is going to be activated. In addition, synchronization (scan mode) will follow the detected mode.

Group Auto:

Multiple video modes can be specified, and switch able among the specified modes. However, scan (scan mode) will follow the detected mode even in the case not specified.

Full Auto:

On each mode of color sub-carrier frequency (Fsc Mode), color modulation (Color Mode) and scan (Scan Mode), operates in accordance to the detected result.

When component signal is applied, only the scan mode (fv: 60Hz/50Hz) can be automatically switched (except manual setting.)

For the register setting values, please refer to Table 4.13.

Table 4.13 Settings for video mode automatic switching

	FULL Auto		GROUP Auto		SINGLE Auto		Manual	
Video System	**ATVM**	**MNVM_ MDD**	**ATVM**	**MNVM_ MDD**	**ATVM**	**MNVM_ MDD**	**ATVM**	**MNVM_ MDD**
NTSC-(Jpn),M	“1xxx xxxx”	“x xxxx”	“0xxx xxx1”	“x xxxx”	“0000 0001”	“x xxxx”	“0000 0000”	“0 0000”
NTSC-4.43	“1xxx xxxx”	“x xxxx”	“0x1x xxxx”	“x xxxx”	“0010 0000”	“x xxxx”	“0000 0000”	“0 1000”
PAL-B,D,G,H,I,N	“1xxx xxxx”	“x xxxx”	“0xxx xx1x”	“x xxxx”	“0000 0010”	“x xxxx”	“0000 0000”	“0 1011”
PAL-M	“1xxx xxxx”	“x xxxx”	“0xxx 1xxx”	“x xxxx”	“0000 1000”	“x xxxx”	“0000 0000”	“0 0000”
PAL-CombiN	“1xxx xxxx”	“x xxxx”	“0xx1 xxxx”	“x xxxx”	“0001 0000”	“x xxxx”	“0000 0000”	“1 0010”
PAL-60	“1xxx xxxx”	“x xxxx”	“01xx xxxx”	“x xxxx”	“0100 0000”	“x xxxx”	“0000 0000”	“0 1010”
SECAM	“1xxx xxxx”	“x xxxx”	“0xxx x1xx”	“x xxxx”	“0000 0100”	“x xxxx”	“0000 0000”	“0 0111”

x: Don't care

4.18. VBI Path-through Data Output

Settings on the registers VBPLS0_ and VBPLS1_, avail 27MHz sampling data of the specified line (For specifying the line, please refer to “5 Interface Registers” on page 78) as output at the image data output SV port or DV port. Please refer to the relevant register VBIDEF_.

For the output port and register settings of the timing signal ”VBI Term” indicate VBI data under output, please refer to “4.15.1 Timing Output Pins” on page.49. In addition, by setting the register SVTDEFVBE, SVB (vertical blanking signal in the SV Line) can be activated during the VBI Path-through output interval. For more detail please see Figure 4.43

Note! Please be careful if VBI Path-through being specified, VBI data extraction shall not avail.

4.19. VBI Data Extraction Circuit

With this circuit, data extraction during the vertical blanking-interval (closed caption, CGMS and WSS.) becomes available. The extracted data can be read at register via a VBI FIFO. Table 4.14 indicates the reference standards of the supported systems.

Table 4.14 The reference standards for VBI data extraction

Expression	System	Line	Org.	Doc. NO.	Doc. Title
Closed Caption	525/60	21/284	EIA	EIA-608	EIA Standard / Recommended Practice for Line 21 Data Service
CGMS(CGMS-A)	525/60	20/283	IEC	IEC61880	International Standard / Video systems (525/60) – Video and accompanied data using the vertical blanking interval – Analogue interface
WSS	625/50	23	ITU	ITU-R BT.1119	Recommendation ITU-R BT.1119 / Wide – Screen Signaling For Broadcasting

Using GPIO status output mode, it is also possible to give receiving CGMS or wide screen information output to the GPIO port. As to the DPIO port, please refer to ” 4.21 GPIO port” on page 73. For setting Closed Caption, CGMS and WSS detection, please refer to register VBELS_.

Note! In case specifying VBI Path-through, please be careful as VBI data cannot be extracted.

4.19.1. Read-out Using VBI FIFO

The XV750C is provided with a FIFO for the VBI extracted data output via host interface registers. The FIFO is 16 stages deep. Using the register VBFDEF_, writing mode etc. into VBI FIFO can be specified.

When reading data from VBI FIFO, first read register FSTS_VBNE , “1” there means there are data in the VBI FIFO, please read the concerned data and information by reading the register VBINF_ VBRD_. For the details of the registers, please refer to "5 Interface Registers" on page 78.

4.20. Interrupt

Detecting Interrupt event, the XV750C produces output interrupt signal at the IRQ_N port.

Relevant registers: FIRQ_ (FIFO related interrupt event)

MIRQ_ (Other miscellaneous interrupt event)

FIMSK_ (FIFO related interrupt masking event)

MIMSK_ (Other miscellaneous interrupt masking event)

4.20.1. Interrupt Events

Interrupt events are as listed below:

FIFO related interrupt:

- DV port FIFO becoming not empty
- DV port FIFO becoming almost empty
- DV port FIFO becoming almost full
- DV port FIFO becoming overflowed
- VBI FIFO becoming not empty
- VBI FIFO becoming almost empty
- VBI FIFO becoming almost full
- VBI FIFO becoming overflowed

Other miscellaneous interrupt

- Video Mode being changed
- Video input sync being detected
- Video input going out of synchronization
- Standard signal being detected
- Non-standard signal being detected
- Interlaced scanning being detected
- Non-Interlaced scanning being detected
- Copy control data being changed

4.20.2. Interrupt Masks

Each interrupt event described above can be independently masked. If any interrupt event taking places during interrupt being masked, no interrupt will happen but the situation will be held. In this case, when the interrupt masking released, the interrupt takes place. To allow the interrupt only after masking being removed, clear any interrupt event before releasing the concerned interrupt masking (by writing "1" into the corresponding bit in the register FIRQ_ and MIRQ_)

4.20.3. Interrupt Signal Timing

The timing of the interrupt request signal is shown here. Figure 4.51 represents the case where all the interrupt events are reset by the registers FIRQ_ and MIRQ_. Figure 4.52 shows the case where an unmasked interrupt event exists despite interrupt event has been reset by the register MIRQ_.

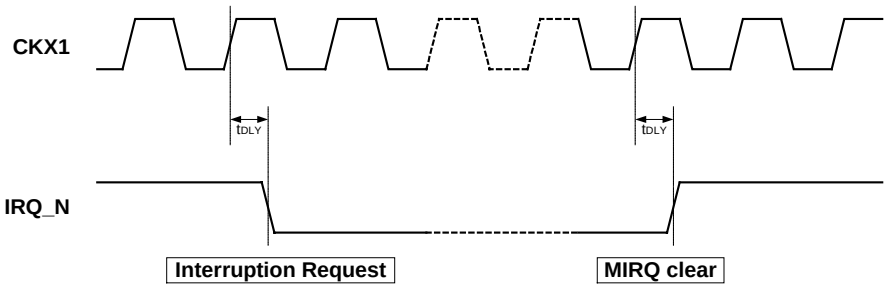


Figure 4.51 Interrupt signal timing (1)

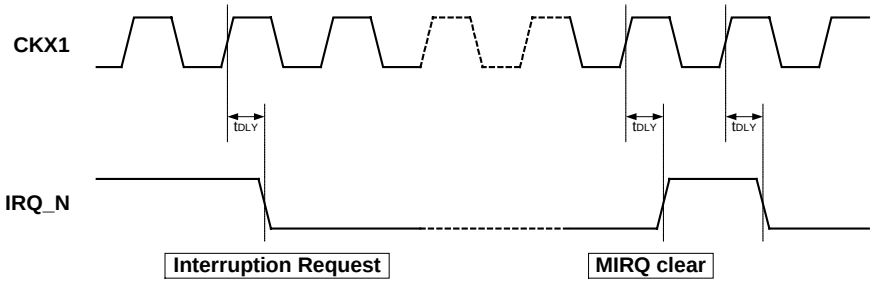


Figure 4.52 Interrupt signal timing (2)

4.21. GPIO Port

The XV750C has a 10-bits GPIO port. Register IO mode and Status Output mode can be selected for each of the two groups of upper 2 bits and lower 8 bits in the GPIO 10 bits. The upper two bits can be used also as the DV Line control timing output pins (DGP output mode).

GPIO lower 8 bits

Register IO mode:	Register GPMD_GPSOL=0
Status Output mode:	Register GPMD_GPSOL=1

GPIO upper 2 bits

Register IO mode:	Register GPMD_GPSOH=0
Status Output mode:	Register GPMD_GPSOH=1
DGP Output mode:	Register GPMD_GPSOH=2
CFR/CFS Output mode:	Register GPMD_GPSOH=3

4.21.1. Register IO Mode

By setting the register GPDIR_GPDIR, input/output can be specified for each bit. Actual read/write is performed through the register GPIOD_GPIOD. Please refer to “5.2 Register Details” on page.84 for the details.

4.21.2. Status Output Mode

Using registers GPMD_GPSSL and GPMD_GPSSH, the address of the internal status can be specified. Please refer to “5.2. Register Details” on page.84 for the details. Table 4.15 shows the registers that can be used for output. In this table, only the lower two bits of addresses from 0x02 to 0x05 can be used for output in the upper two bits of GPIO.

Table 4.15 Registers usable for GPIO Output

Address	Name	Read Write	MSB 7	6	5	4	3	2	1	LSB 0	Default
0x02	VMJDG Video Mode Judgement	R	CONF	rsv	SUPM	FSCM 1	FSCM 0	COLM 1	COLM 0	SCNM	
0x03	FSTS FIFO Status	R	VBFL	VBAF	VBAE	VBNE	DVFL	DVAF	DVAE	DVNE	
0x04	MSTS Misc. Status	R	NINT 1	NINT 0	NSTD	TBCE	CKON	BBON	SDET	FSCL	
0x05		R	rsv	AGAT 2	AGAT 1	AGAT 0	rsv	PJCON	VCXO 1	VCXO 0	
0x06	WSSTS Wide Screen Status	R	DETE	DETO	ASPE 1	ASPE 0	POS	FORM	ASPO 1	ASPO 0	
0x07	VBINF VBI FIFO Informations	R	VBERR	rsv	VBWN 1	VBWN 0	VBFLD	rsv	VBID 1	VBID 0	
0x08	VBRD VBI FIFO Read Data	R	VBRD 7	VBRD 6	VBRD 5	VBRD 4	VBRD 3	VBRD 2	VBRD 1	VBRD 0	
0xAB	CFSINF Color Field Seqence Information	R	rsv	rsv	rsv	rsv	CONF	CFSQ 2	CFSQ 1	CFSQ 0	

4.21.3. DGP2, 3 Signal Output

The upper two bits of GPIO can be used as the control timing output pins for the DV Line. Please refer to the registers DVGDEF_DGP2 and DVGDEF_DGP3 for the details.

4.21.4. CFR/CFS (Color Field Reset/Strobe) Signal Output

The upper two bits of GPIO can use GPIO lower 8 bits as CFR/CFS signal. This signal can also be fed to pins SCBF and SFLD.

4.22. I^2C Interface

The XV750C has an I^2C bus interface as the external host interface. It supports up to Fast-Mode.

Table 4.16 shows the slave addresses. By the setting of the IOAS pin, slave address can select two addresses.

Table 4.16 I^2C slave addresses

IOAS	A6	A5	A4	A3	A2	A1	A0	RW
Low	1	0	0	0	1	0	0	X
High	1	0	0	0	1	0	1	X

Figure 4.53 and Figure 4.54 show the write and read sequence timing respectively. In addition, the write and read timings when accessed continuously are shown in Figure 4.55 and Figure 4.56 respectively.

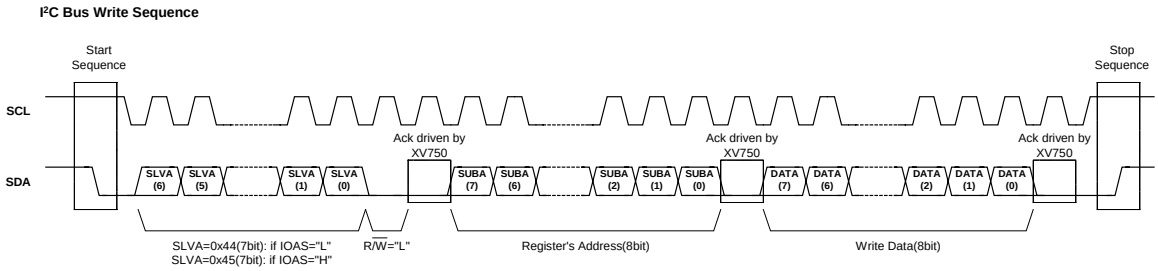


Figure 4.53 I²C Bus write sequence

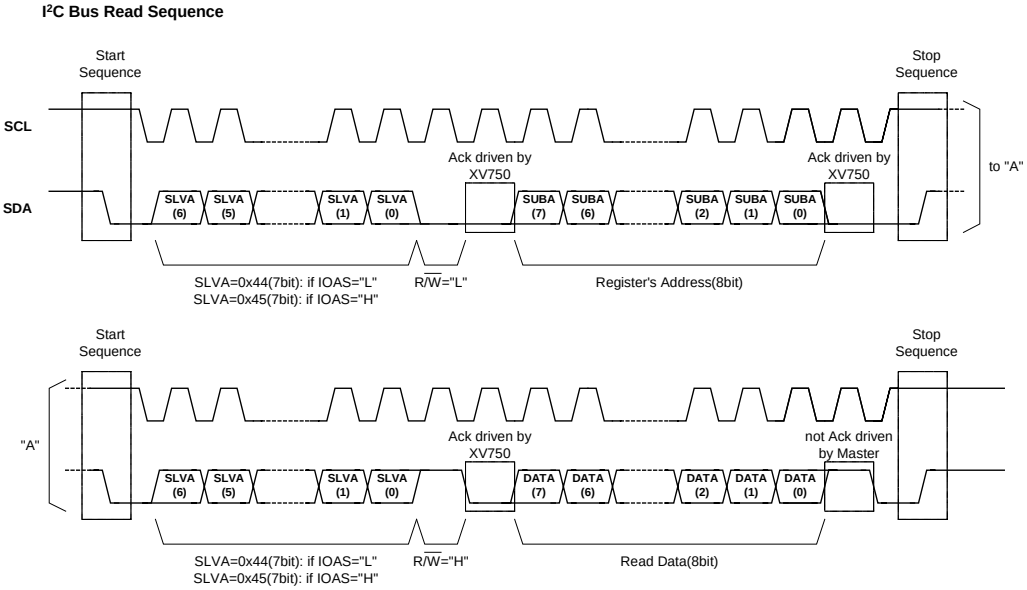


Figure 4.54 I²C Bus read sequence

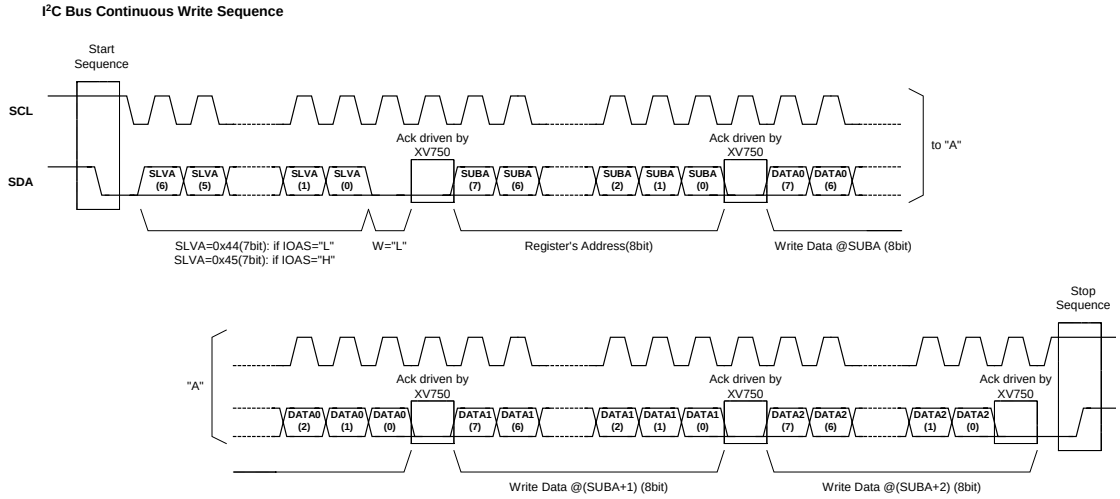


Figure 4.55 I²C Bus write sequence (continuous access)

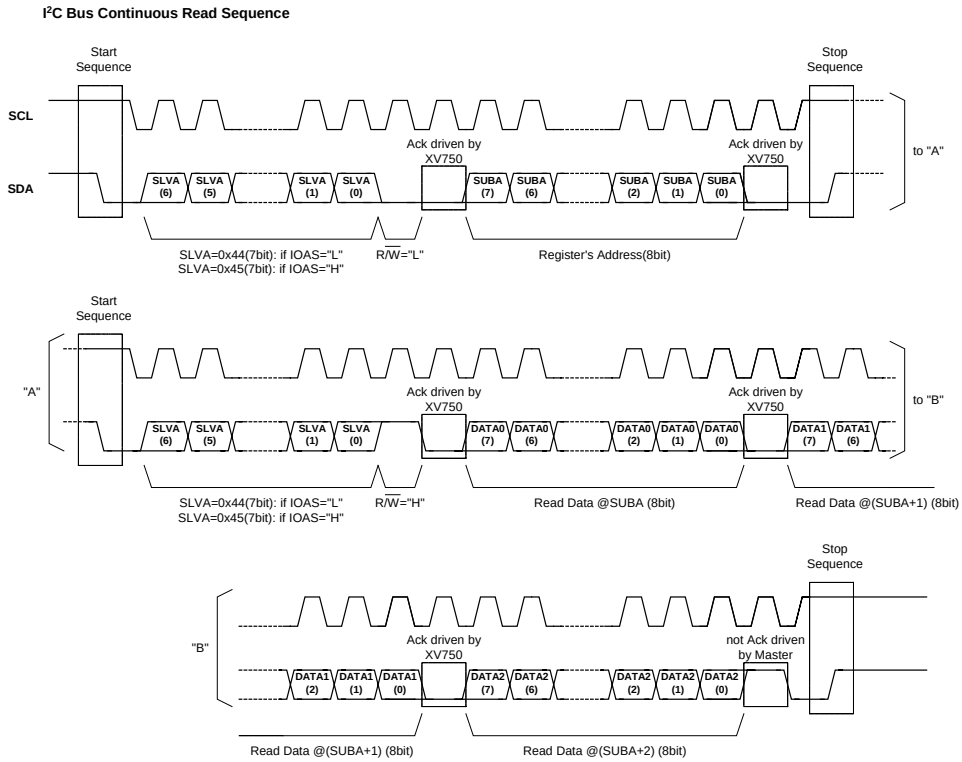


Figure 4.56 I²C Bus read sequence (continuous access)

4.23. Anti-Copy Protection

The XV750C is provided with a detection function based on "SPECIFICATION FOR DETECTION OF THE MACROVISION COPY PROTECTION PROCESS As Used On 525/60 and 625/50 DVD, STB and Pre-Recorded VHS Cassette Analog Video Outputs Revision 1.00". (Passed the Macrovision certification test) For more details, please refer to MacroVison™.

4.24. JTAG

The XV750C contains a JTAG circuit. For more details, please contact IIX Inc.

4.25. Test Pattern Generator

The XV750C can output color bar pattern, ramp pattern and raster pattern for testing. Each color level of the pattern output is as shown in the Table 4.17. The relative registers are TPGEN_MODE、TPGEN_PICS、TPGEN_AMPS

	White	Yellow	Cyan	Green	Magenta	Red	Blue	Black
NTSC 100%								
Y	235	210	170	145	106	81	41	16
Cb	128	16	166	584	202	90	240	128
Cr	128	146	16	34	222	240	110	128
NTSC 75%								
Y	180	162	131	112	84	65	35	16
Cb	128	44	156	72	184	100	212	128
Cr	128	142	44	58	198	212	114	128
PAL 100%								
Y	235	210	170	145	106	81	41	16
Cb	128	16	166	54	202	90	240	128
Cr	128	146	16	34	222	240	110	128
PAL 75%								
Y	235	162	131	112	84	65	35	16
Cb	128	44	156	72	184	100	212	128
Cr	128	142	44	58	198	212	114	128

Table 4.17 Color Level (8bits digital range)

5. Interface Registers

The XV750C has various interface registers to configure various flags, image adjustment, mode settings and parameter settings. The interface registers can be configured via the I^2C bus interface.

5.1. List of Registers

Table 5.1 shows the list of all registers. For the detailed explanation, please refer to “5.2 Register Details” on page.84.

Table 5.1 List of interface registers

Add-ress	Name	Read Write	MSB 7	6	5	4	3	2	1	LSB 0	De-fault
Flags and Status											
0x00	PRDC Product Code	R	PRDC 7	PRDC 6	PRDC 5	PRDC 4	PRDC 3	PRDC 2	PRDC 1	PRDC 0	
0x01		R	PRDC 15	PRDC 14	PRDC 13	PRDC 12	PRDC 11	PRDC 10	PRDC 9	PRDC 8	
0x02	VMJDG Video Mode Judgement	R	CONF	rsv	SUPM	FSCM 1	FSCM 0	COLM 1	COLM 0	SCNM	
0x03	FSTS FIFO Status	R	VBFL	VBAF	VBAE	VBNE	DVFL	DVAF	DVAE	DVNE	
0x04	MSTS Misc. Status	R	NINT 1	NINT 0	NSTD	TBCE	CKON	BBON	SDET	FSCL	
0x05		R	rsv	AGAT 2	AGAT 1	AGAT 0	rsv	PJCON	VCXO 1	VCXO 0	
0x06	WSSTS Wide Screen Status	R	DETE	DETO	ASPE 1	ASPE 0	POS	FORM	ASPO 1	ASPO 0	
0x07	VBINF VBI FIFO Informations	R	VBERR	rsv	VBWN 1	VBWN 0	VBFLD	rsv	VBID 1	VBID 0	
0x08	VBRD VBI FIFO Read Data	R	VBRD 7	VBRD 6	VBRD 5	VBRD 4	VBRD 3	VBRD 2	VBRD 1	VBRD 0	
0x09	DCCD Detected Copy Control Data	R	CSTYP	CSDET	AGCP	PSDET	rsv	rsv	DCCD 1	DCCD 0	
0x0A	FIRQ FIFO Interrupt Request	R/W	VBOV	VBAF	VBAE	VBNE	DVOV	DVAF	DVAE	DVNE	
0x0B	MIRQ Misc. Interrupt Request	R/W	DCCD	NINT	INT	NSTD	STD	NSDET	SDET	VMCLM	
0x0C	GPIOD General Purpose IO Read Write Data	W/R	GPIOD 7	GPIOD 6	GPIOD 5	GPIOD 4	GPIOD 3	GPIOD 2	GPIOD 1	GPIOD 0	
0x0D		W/R	rsv	rsv	rsv	rsv	rsv	rsv	GPIOD 9	GPIOD 8	
Picture Tuning											
0x10	CONT Contrast Trimmer	W/(R)	CONT 7	CONT 6	CONT 5	CONT 4	CONT 3	CONT 2	CONT 1	CONT 0	0x00
0x11	BRTT Brightness Trimmer	W/(R)	BRTT 6	BRTT 5	BRTT 4	BRTT 3	BRTT 2	BRTT 1	BRTT 0	rsv	0x00
0x12	APCOR Apeature Correction	W/(R)	CORG 1	CORG 0	rsv	WEIT 2	WEIT 1	WEIT 0	APBW 1	APBW 0	0x00
0x13	CLMK Color Level Trimmer	W/(R)	CHRMK 7	CHRMK 6	CHRMK 5	CHRMK 4	CHRMK 3	CHRMK 2	CHRMK 1	CHRMK 0	0x00
0x14		W/(R)	COLUM 7	COLUM 6	COLUM 5	COLUM 4	COLUM 3	COLUM 2	COLUM 1	COLUM 0	0x00
0x15		W/(R)	COLVM 7	COLVM 6	COLVM 5	COLVM 4	COLVM 3	COLVM 2	COLVM 1	COLVM 0	0x00

Add-ress	Name	Read Write	MSB 7	6	5	4	3	2	1	LSB 0	De-fault
0x16	HUET Hue Trimmer	W/(R)	HUET 1	HUET 0	rsv	UVOF 4	UVOF 3	UVOF 2	UVOF 1	UVOF 0	0x00
0x17		W/(R)	HUET 9	HUET 8	HUET 7	HUET 6	HUET 5	HUET 4	HUET 3	HUET 2	0x00
0x18	TRPFCHR TRAP Filter Characteristics	W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	CHRS 1	CHRS 0	0x02
0x19	BPFCHR Band Pass Filter Characteristics	W/(R)	rsv	rsv	rsv	rsv	rsv	CHRS 2	CHRS 1	CHRS 0	0x00
0x1A	BELCHR BELL Filter Characteristics	W/(R)	rsv	rsv	SHAP 1	SHAP 0	rsv	rsv	SIFT 1	SIFT 0	0x00
0x1B	DEMPCHR De-Emphasys Filter Characteristics	W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	CHRS 1	CHRS 0	0x00
0x1C	PROFLT Programmable Filter Parameter Setting	W/(R)	ADRS 7	ADRS 6	ADRS 5	ADRS 4	ADRS 3	ADRS 2	ADRS 1	ADRS 0	0x00
0x1D		W/(R)	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0	0x00
0x1E	VENHANC Virtical Enhancer	W/(R)	CORG 1	CORG 0	rsv	WEIT 2	WEIT 1	WEIT 0	rsv	ENB	0x00
Configuration											
0x20	AIMS Analog Input MUX Selection	W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	SELP 1	SELP 0	0x00
0x21	ATVM Automatic Video Mode Settings	W/(R)	FULL	VSTD 6	VSTD 5	VSTD 4	VSTD 3	VSTD 2	VSTD 1	VSTD 0	0x7F
0x22	MNVM Manual Video Mode Settings	W/(R)	MOD 7	MOD 6	MOD 5	MOD 4	MOD 3	MOD 2	MOD 1	MOD 0	0x80
0x23	COMBDEF Comb Filter Definition	W/(R)	Rsv	rsv	PAFS	PCOMB	rsv	ACMS	BPFS	COMS	0x14
0x24		W/(R)	P3HT 3	P3HT 2	P3HT 1	P3HT 0	P3LT 3	P3LT 2	P3LT 1	P3LT 0	0xCB
0x25	Reserved	rsv	rsv	rsv	rsv	rsv	rsv	rsv	rsv	rsv	
0x26	AGCDEF Automatic Gain Control Definitions	W/(R)	rsv	rsv	LMT	FRZ	rsv	MOD 2	MOD 1	MOD 0	0x22
0x27		W/(R)	AGMK 7	AGMK 6	AGMK 5	AGMK 4	AGMK 3	AGMK 2	AGMK 1	AGMK 0	0x00
0x28		W/(R)	rsv	rsv	rsv	rsv	rsv	AGTC 2	AGTC 1	AGTC 0	0x04
0x29		W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	HVSL 1	HVSL 0	0x02
0x2A	PAGCC Peak AGC Control	W/(R)	PAGM 7	PAGM 6	PAGM 5	PAGM 4	PAGM 3	PAGM 2	PAGM 1	PAGM 0	0x7F
0x2B		W/(R)	rsv	rsv	rsv	rsv	SETM	SETC 2	SETC 1	SETC 0	0x04
0x2C		W/(R)	REOFS 3	REOFS 2	REOFS 1	REOFS 0	rsv	RETC 2	RETC 1	RETC 0	0x84
0x2D	YGFXA Y Ch. Fixed Gain for Analog Amp.	W/(R)	rsv	rsv	rsv	rsv	rsv	FXGA 2	FXGA 1	FXGA 0	0x01
0x2E	LGFXD Luminance Fixed Gain for Digital AGC	W/(R)	FXGD 0	rsv	rsv	rsv	rsv	rsv	rsv	rsv	0x00
0x2F		W/(R)	FXGD 8	FXGD 7	FXGD 6	FXGD 5	FXGD 4	FXGD 3	FXGD 2	FXGD 1	0x80
0x30	ACCDEF Automatic Chrominance Gain Control Definitions	W/(R)	rsv	rsv	LMT	FRZ	rsv	rsv	MOD 1	MOD 0	0x23
0x31		W/(R)	ACMK 5	ACMK 4	ACMK 3	ACMK 2	ACMK 1	ACMK 0	rsv	rsv	0x00
0x32		W/(R)	rsv	rsv	rsv	rsv	rsv	ACTC 2	ACTC 1	ACTC 0	0x04
0x33	CGFXA C Ch. Fixed Gain for Analog Amp.	W/(R)	rsv	rsv	rsv	rsv	rsv	FXGA 2	FXGA 1	FXGA 0	0x01
0x34	PGFXA P Ch. Fixed Gain for Analog Amp.	W/(R)	rsv	rsv	rsv	rsv	rsv	FXGA 2	FXGA 1	FXGA 0	0x01

Address	Name	Read Write	MSB 7	6	5	4	3	2	1	LSB 0	Default
0x35	CHGFXD Chrominance Fixed Gain for Digital ACC	W/(R)	FXGD 0	rsv	rsv	rsv	rsv	rsv	rsv	rsv	0x00
0x36		W/(R)	FXGD 8	FXGD 7	FXGD 6	FXGD 5	FXGD 4	FXGD 3	FXGD 2	FXGD 1	0x80
0x37	UVGFXD U/V Fixed Gain for Digital ACC	W/(R)	FXGD 0	rsv	rsv	rsv	rsv	rsv	rsv	rsv	0x00
0x38		W/(R)	FXGD 8	FXGD 7	FXGD 6	FXGD 5	FXGD 4	FXGD 3	FXGD 2	FXGD 1	0x80
0x39	SBMSK SV Port Blanking Mask Settings	W/(R)	rsv	rsv	rsv	rsv	CMSV	CMSH	YMSV	YMSH	0x0F
0x3A	VBISLC VBI Slice Level Control	W/(R)	MOD	LEV 6	LEV 5	LEV 4	LEV 3	LEV 2	LEV 1	LEV 0	0x20
0x3B	PJCSW Pixel Jitter Canceller Switch	W/(R)	rsv	rsv	rsv	rsv	rsv	AUTO	CPJC	YPJC	0x07
0x3C	TBCDEF TBC Definitions	W/(R)	RLS 3	RLS 2	RLS 1	RLS 0	RLE 1	RLE 0	MOD	ENB	0x03
0x3D	VCXODEF VCXO Definitions	W/(R)	rsv	rsv	rsv	HCTLE	rsv	rsv	MOD 1	MOD 0	0x10
0x3E	BBDEF Blue-back Definitions	W/(R)	rsv	rsv	rsv	rsv	rsv	MOD 2	MOD 1	MOD 0	0x01
0x3F	VBIDEF VBI Definitions	W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	SVPTE	DVPTE	0x00
0x40	VBPLS0 VBI Path Through Line Selection #0	W/(R)	FIDSL	VBPSL 6	VBPSL 5	VBPSL 4	VBPSL 3	VBPSL 2	VBPSL 1	VBPSL 0	0x11
0x41		W/(R)	FIDEL	VBPEL 6	VBPEL 5	VBPEL 4	VBPEL 3	VBPEL 2	VBPEL 1	VBPEL 0	0x11
0x42	VBPLS1 VBI Path Through Line Selection #1	W/(R)	FIDSL	VBPSL 6	VBPSL 5	VBPSL 4	VBPSL 3	VBPSL 2	VBPSL 1	VBPSL 0	0x91
0x43		W/(R)	FIDEL	VBPEL 6	VBPEL 5	VBPEL 4	VBPEL 3	VBPEL 2	VBPEL 1	VBPEL 0	0x91
0x44	VBELS VBI Extractor Line Settings	W/(R)	CCELO 3	CCELO 2	CCELO 1	CCELO 0	CCSLO 3	CCSLO 2	CCSLO 1	CCSLO 0	0xBB
0x45		W/(R)	CCELE 3	CCELE 2	CCELE 1	CCELE 0	CCSLE 3	CCSLE 2	CCSLE 1	CCSLE 0	0xBB
0x46		W/(R)	CGELO 3	CGELO 2	CGELO 1	CGELO 0	CGSLO 3	CGSLO 2	CGSLO 1	CGSLO 0	0xAA
0x47		W/(R)	CGELE 3	CGELE 2	CGELE 1	CGELE 0	CGSLE 3	CGSLE 2	CGSLE 1	CGSLE 0	0xAA
0x48		W/(R)	WSELO 3	WSELO 2	WSELO 1	WSELO 0	WSSLO 3	WSSLO 2	WSSLO 1	WSSLO 0	0xCC
0x49		W/(R)	WSELE 3	WSELE 2	WSELE 1	WSELE 0	WSSLE 3	WSSLE 2	WSSLE 1	WSSLE 0	0xCC
0x4A	YCDELAY YC Delay	W/(R)	ODLC 2	ODLC 1	ODLC 0	rsv	ODLY 2	ODLY 1	ODLY 0	rsv	0x00
0x4B	HSDELAY HS Delay	W/(R)	HST 7	HST 6	HST 5	HST 4	HST 3	HST 2	HST 1	HST 0	0x00
0x4C	VSDELAY VS Delay	W/(R)	VST 7	VST 6	VST 5	VST 4	VST 3	VST 2	VST 1	VST 0	0x00
0x4D	ACTWINS Active Video Window Settings	W/(R)	WINL 3	WINL 2	WINL 1	WINL 0	rsv	rsv	rsv	rsv	0x00
0x4E		W/(R)	WINR 3	WINR 2	WINR 1	WINR 0	rsv	rsv	rsv	rsv	0x00
0x4F		W/(R)	WINT 3	WINT 2	WINT 1	WINT 0	rsv	rsv	rsv	rsv	0x00
0x50		W/(R)	WINB 3	WINB 2	WINB 1	WINB 0	rsv	rsv	rsv	rsv	0x00
0x51	SCROPDEF SV Port Cropping Definitions	W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	MOD 1	MOD 0	0x00
0x52	SCROPH SV Port Cropping H Settings	W/(R)	CRPHS 7	CRPHS 6	CRPHS 5	CRPHS 4	CRPHS 3	CRPHS 2	CRPHS 1	CRPHS 0	0x12
0x53		W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	rsv	CRPHS 8	0x00
0x54		W/(R)	CRPHA 7	CRPHA 6	CRPHA 5	CRPHA 4	CRPHA 3	CRPHA 2	CRPHA 1	CRPHA 0	0x68

Add-ress	Name	Read Write	MSB 7	6	5	4	3	2	1	LSB 0	De-fault
0x55		W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	rsv	CRPHA 8	0x01
0x56	SCROPV SV Port Cropping V Settings	W/(R)	CRPVS 7	CRPVS 6	CRPVS 5	CRPVS 4	CRPVS 3	CRPVS 2	CRPVS 1	CRPVS 0	0x06
0x57		W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	CRPVS 9	CRPVS 8	0x00
0x58		W/(R)	CRPVA 7	CRPVA 6	CRPVA 5	CRPVA 4	CRPVA 3	CRPVA 2	CRPVA 1	CRPVA 0	0xE6
0x59		W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	CRPVA 9	CRPVA 8	0x01
0x5A	DCROPH DV Port Cropping H Settings	W/(R)	CRPHS 7	CRPHS 6	CRPHS 5	CRPHS 4	CRPHS 3	CRPHS 2	CRPHS 1	CRPHS 0	0x12
0x5B		W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	rsv	CRPHS 8	0x00
0x5C		W/(R)	CRPHA 7	CRPHA 6	CRPHA 5	CRPHA 4	CRPHA 3	CRPHA 2	CRPHA 1	CRPHA 0	0x68
0x5D		W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	CRPHA 9	CRPHA 8	0x01
0x5E	DCROPV DV Port Cropping V Settings	W/(R)	CRPVS 7	CRPVS 6	CRPVS 5	CRPVS 4	CRPVS 3	CRPVS 2	CRPVS 1	CRPVS 0	0x0A
0x5F		W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	rsv	CRPVS 8	0x00
0x60		W/(R)	CRPVA 7	CRPVA 6	CRPVA 5	CRPVA 4	CRPVA 3	CRPVA 2	CRPVA 1	CRPVA 0	0xE0
0x61		W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	CRPVA 9	CRPVA 8	0x01
0x62	CKILLS Color Killer Settings	W/(R)	CKLE	MOD	rsv	RLEV 1	RLEV 0	ALEV 2	ALEV 1	ALEV 0	0x81
0x63	FHCTLS FH Control Setting	W/(R)	CODE 5	CODE 4	CODE 3	CODE 2	CODE 1	CODE 0	TBCE	rsv	0x00
0x64		W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	rsv	rsv	0x00
0x65		W/(R)	TBCT 6	TBCT 5	TBCT 4	TBCT 3	TBCT 2	TBCT 1	TBCT 0	rsv	0x00
0x66	HSYNC Hsync Setting	W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	rsv	TC	0x00
0x67	VSSFT Vsync Shift Setting	W/(R)	rsv	rsv	rsv	SFTL 4	SFTL 3	SFTL 2	SFTL 1	SFTL 0	0x00
Scaller Settings											
0x70	SCALM Scaller Mode	W/(R)	rsv	rsv	rsv	rsv	rsv	INTO	INTI	VFLTS	0x06
0x71	HPHS Horizontal Phase Settings	W/(R)	rsv	rsv	OFST 5	OFST 4	OFST 3	OFST 2	OFST 1	OFST 0	0x00
0x72	HFILT Horizontal Filter Setting	W/(R)	rsv	rsv	FILT 5	FILT 4	FILT 3	FILT 2	FILT 1	FILT 0	0x20
0x73	HSCAL Horizontal Scale Settings	W/(R)	SCAL 7	SCAL 6	SCAL 5	SCAL 4	SCAL 3	SCAL 2	SCAL 1	SCAL 0	0x00
0x74		W/(R)	SCAL 15	SCAL 14	SCAL 13	SCAL 12	SCAL 11	SCAL 10	SCAL 9	SCAL 8	0x80
0x75	VPHS Vertical Phase Settings	W/(R)	rsv	rsv	OFST 5	OFST 4	OFST 3	OFST 2	OFST 1	OFST 0	0x00
0x76	VFILT Vertical Filter Setting	W/(R)	rsv	rsv	VFILT 5	VFILT 4	VFILT 3	VFILT 2	VFILT 1	VFILT 0	0x20
0x77	VSCAL Vertical Scale Settings	W/(R)	VSCAL 7	VSCAL 6	VSCAL 5	VSCAL 4	VSCAL 3	VSCAL 2	VSCAL 1	VSCAL 0	0x00
0x78		W/(R)	VSCAL 15	VSCAL 14	VSCAL 13	VSCAL 12	VSCAL 11	VSCAL 10	VSCAL 9	VSCAL 8	0x40
System Configurations											
0x80	LPWCS Low Power Consumption Control Settings	W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	AUTO	PINE	0x03
0x81		W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	OFPWM	OFSCE	0x00
0x82		W/(R)	AFEC 7	AFEC 6	AFEC 5	AFEC 4	AFEC 3	AFEC 2	AFEC 1	AFEC 0	0x9F
0x83	AINDEF Analog Input Definitions	W/(R)	SEL3 1	SEL3 0	SEL2 1	SEL2 0	SEL1 1	SEL1 0	SEL0 1	SEL0 0	0x00

Address	Name	Read Write	MSB 7	6	5	4	3	2	1	LSB 0	Default
0x84	ICHX Input Channel Cross-Over	W/(R)	rsv	rsv	DPCH 1	DPCH 0	DCCH 1	DCCH 0	DYCH 1	DYCH 0	0x24
0x85	VSMPDEF Video Sampling Definitions	W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	SMPC	DCFB	0x00
0x86	ICMPNDEF Input Component Definitions	W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	LEV 1	LEV 0	0x00
0x87	Reserved	W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	rsv	rsv	
0x88	VPDEF Output Video Port Definitions	W/(R)	SVCOE	DVCOE	SVOE	DVOE	ADEM	MOD 2	MOD 1	MOD 0	0x00
0x89	SVVDEF SV Port Video Definitions	W/(R)	S10B	rsv	SOLM	SRGB 1	SRGB 0	rsv	SOLV 1	SOLV 0	0x80
0x8A	DVVDEF DV Port Video Definitions	W/(R)	OECV	rsv	DOLM	DRGB 1	DRGB 0	rsv	DOLV 1	DOLV 0	0x00
0x8B	SVTDEF SV Port Timing Definitions	W/(R)	rsv	rsv	rsv	rsv	rsv	VBE	HBE	R656	0x01
0x8C	DVTDEF DV Port Timing Definitions	W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	rsv	R656	0x01
0x8D	SVCDEF SV Port Control Signal Definitions	W/(R)	rsv	SFLDS 2	SFLDS 1	SFLDS 0	rsv	SCBFS 2	SCBFS 1	SCBFS 0	0x00
0x8E	DVCDEF DV Port Control Signal Definitions	W/(R)	rsv	DGVP	rsv	DGHP	rsv	rsv	DVALG	DCKS	0x01
0x8F	DVGDEF DV Port General Signal Definitions	W/(R)	OECV1	DGP1 2	DGP1 1	DGP1 0	OECV0	DGP0 2	DGP0 1	DGP0 0	0x21
0x90		W/(R)	OECV3	DGP3 2	DGP3 1	DGP3 0	OECV2	DGP2 2	DGP2 1	DGP2 0	0x00
0x91	SVPOL SV Port Polarities	W/(R)	SCK	rsv	SFLD	SCBF	SVB	SHB	SVS	SHS	0x00
0x92	DVPOL DV Port Polarities	W/(R)	DCK	rsv	DTRDY	DVAL	DGP1	DGP0	DGVP	DGHP	0x00
0x93	GPMD General Purpose IO Mode	W/(R)	GPSSH 1	GPSSH 0	GPSSL 2	GPSSL 1	GPSSL 0	GPSOH 1	GPSOH 0	GPSOL	0x00
0x94	GPDIR General Purpose IO pin Direction Settings	W/(R)	GPDIR 7	GPDIR 6	GPDIR 5	GPDIR 4	GPDIR 3	GPDIR 2	GPDIR 1	GPDIR 0	0x00
0x95		W/(R)	SOUT	SIN	rsv	rsv	rsv	rsv	GPDIR 9	GPDIR 8	0x00
0x96	FIMSK FIFO Interrupt Mask	W/(R)	VBOV	VBAF	VBAE	VBNE	DVOV	DVAF	DVAE	DVNE	0xFF
0x97	MIMSK Misc. Interrupt Mask	W/(R)	DCCD	NINT	INT	NSTD	STD	NSDET	SDET	VMCLM	0xFF
0x98	DVFLV DV Port FIFO Trigger Level	W/(R)	AFL 3	AFL 2	AFL 1	AFL 0	AEL 3	AEL 2	AEL 1	AEL 0	0x88
0x99	VBFLV VBI FIFO Trigger Level	W/(R)	rsv	AFL 2	AFL 1	AFL 0	rsv	AEL 2	AEL 1	AEL 0	0x22
0x9A	VBFDEF VBI FIFO Definitions	W/(R)	CGCRC	CCNULL	WSERR	CGERR	CCERR	WWSS	WCGMS	WCC	0x00
0x9B	PWMS PWM Settings	W/(R)	MOD	rsv	rsv	TC 4	TC 3	TC 2	TC 1	TC 0	0x80
0x9C	VCXOS VCXO Settings	W/(R)	VXOFS 7	VXOFS 6	VXOFS 5	VXOFS 4	VXOFS 3	VXOFS 2	VXOFS 1	VXOFS 0	0x00
0x9D		W/(R)	VXPOL	rsv	rsv	rsv	VXTC 3	VXTC 2	VXTC 1	VXTC 0	0x88
0x9E	CFRDEF Color Field Reset Signal Definitions	W/(R)	rsv	FLDP 2	FLDP 1	FLDP 0	rsv	rsv	FLDN 1	FLDN 0	0x73
0x9F		W/(R)	LINE 4	LINE 3	LINE 2	LINE 1	LINE 0	rsv	rsv	WID	0x01
0xA0	SYNCDEF Sync Detection Definitions	W/(R)	rsv	rsv	rsv	rsv	rsv	rsv	SYRT 1	SYRT 0	0x00
0xA1	PDLDEF Pedestal Level Detection Definitions	W/(R)	rsv	rsv	rsv	ADPT	MOD	TC 2	TC 1	TC 0	0x1C

Add-ress	Name	Read Write	MSB 7	6	5	4	3	2	1	LSB 0	De-fault
0xA2	TPGENS Test Pattern Generator Settings	W/(R)	AMPS 2	AMPS 1	AMPS 0	PICS 2	PICS 1	PICS 0	MODE 1	MODE 0	0x00
Information and Data											
0xA8	SNRMON Signal Noise Ratio Monitor	R	SLEV 7	SLEV 6	SLEV 5	SLEV 4	SLEV 3	SLEV 2	SLEV 1	SLEV 0	
0xA9		R	NLEV 7	NLEV 6	NLEV 5	NLEV 4	NLEV 3	NLEV 2	NLEV 1	NLEV 0	
0xAA	HLJINF H-Lock Judgement Information	R	LCKE 7	LCKE 6	LCKE 5	LCKE 4	LCKE 3	LCKE 2	LCKE 1	LCKE 0	
0xAB	CFSINF Color Field Seqence Information	R	rsv	rsv	rsv	rsv	CONF	CFSQ 2	CFSQ 1	CFSQ 0	
0xAC	VTRDET VTR Detection	R	rsv	rsv	rsv	rsv	rsv	WEAK	VTR 1	VTR 0	

5.2. Register Details

Here gives sample register explanation. (The register EXAMPLE_ is for explanatory purpose only and not existing.)

First, please see the list of registers' main ID and bit map. Main ID is a summary of a number of relevant registers, having an underscore "_" at the end of the alphanumerical letter.

EXAMPLE_[6]

0xFF

Name[7]							R/W[8]	
Example Register							Write/Read	
Address[9]	D7	D6	D5	D4	D3	D2	D1	D0[10]
0xFF	rsv	LEV 2	LEV 1	LEV 0	rsv	rsv	MOD 1	MOD 0

Next follows the table that describes registers included in the above main ID. Generally, a register representation has a sub-ID after the underscore.

Identification[11]	Bit Width[12]	Expression[13]	Default[14]
EXAMPLE_MOD	2	Binary	0x0
Description[15]			
This register specifies a mode.			
Value[16]	Operation or Status[16]		
0	Mode 0		
1	Mode 1		
Note[17]			

The next register table follows. In this example, since the sub-IDs included in the main ID of EXAMPLE_ being MOD and LEV, the tables for the registers EXAMPLE_MOD and EXAMPLE_LEV follow.

Identification	Bit Width	Expression	Default
EXAMPLE_LEV	3	2's Complement	0x1
Description			
This register sets the level…..			
Value	Operation or Status		
-4 to +3	The level goes down if the value turns to minus, goes up if it turns to plus, based on zero (0) as its center.		
Note			

[7] Main ID for the register.
[8] Name column of the main ID.
[9] Indicates the register's direction of access (read/write)
[10] Address of the register. 0x means the representation is in hexadecimal
[11] .Denotes each bit's meaning (sub ID) "rsv" represents the bit is reserved. Please note also that the addresses not described in "List of Registers" or "Register Details" are all reserved.
[12] Register ID. Sub ID follows main ID.
[13] Indicates the bit width of the register.
[14] Represents register notation (binary, 2's complement etc.).
[15] The default value of the register.
[16] The description on the register.
[17] The register values and its movement and/or description
[17] Other notes or special comments will be described here.

5.2.1. Flag and Status

PRDC_

0x00 – 0x01

Name							R/W	
Product Code							Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x00	PRDC 7	PRDC 6	PRDC 5	PRDC 4	PRDC 3	PRDC 2	PRDC 1	PRDC 0
0x01	PRDC 15	PRDC 14	PRDC 13	PRDC 12	PRDC 11	PRDC 10	PRDC 9	PRDC 8

Identification	Bit Width	Expression	Default
PRDC_PRDC	16	Binary	-
Description			
Denotes the product code.			
Value	Operation or Status		
0xBB84	Product code		

VMJDG_

0x02

Name							R/W	
Video Mode Judgment							Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x02	CONF	rsv	SUPM	FSCM 1	FSCM 0	COLM 1	COLM 0	SCNM

Identification	Bit Width	Expression	Default
VMJDG_SCNM	1	Binary	-
Description			
Displays the result of video mode judgment. (scan mode)			
Value	Operation or Status		
0	60(59.94)Hz, 525Line		
1	50Hz, 625Line		
Note			
Effective only when the register VMJDG_CONF='1'			

Identification	Bit Width	Expression	Default
VMJDG_COLM	2	Binary	-
Description			
Displays the result of video mode judgment. (color modulation)			
Value	Operation or Status		
0	NTSC		
1	PAL		
2	Reserved		
3	SECAM		
Note			
Effective only when the register VMJDG_CONF='1'			

Identification	Bit Width	Expression	Default
VMJDG_ FSCM	2	Binary	-
Description			

Indicates the result of video mode judgment. (FSC mode)	
Value	Operation or Status
0	3.579545MHz (NTSC-M, NTSC-Japan)
1	4.43361875MHz (PAL-B,D,G,H,I,N, PAL-60, NTSC-4.43)
2	3.57561149MHz (PAL-M)
3	3.58205625MHz (PAL-CombinationN)
Note	
Effective only when the register VMJDG_CONF='1'	

Identification	Bit Width	Expression	Default
VMJDG_SUPM	1	Binary	-
Description			
Indicates the setup mode actually working			
Value	Operation or Status		
0	Setup 0 (IRE)		
1	Setup 7.5 (IRE)		
Note			

Identification	Bit Width	Expression	Default
VMJDG_CONF	1	Binary	-
Description			
Indicates the result of video mode judgement effective and effective or not of the registers VMJDG_SCNM, VMJDG_COLM, VMJDG_FSCM.			
Value	Operation or Status		
0	Ineffective		
1	Effective		
Note			

FSTS_

0x03

Name							R/W	
FIFO Status							Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x03	VBFL	VBAF	VBAE	VBNE	DVFL	DVAF	DVAE	DVNE

Identification	Bit Width	Expression	Default
FSTS_DVNE	1	Binary	-
Description			
Indicates the status that the DV port FIFO is not empty			
Value	Operation or Status		
0	DV port FIFO is empty		
1	DV port FIFO is not empty (data exists in one or more stage)		
Note			

Identification	Bit Width	Expression	Default
FSTS_DVAE	1	Binary	-
Description			
Indicates the status that the DV port FIFO is almost empty			
Value	Operation or Status		

0	DV port FIFO is not almost empty
1	DV port FIFO is almost empty
Note	
The criterion is defined by the register DVFLV_AEL	

Identification	Bit Width	Expression	Default
FSTS_DVAF	1	Binary	-
Description			
Indicates the status that the DV port FIFO is almost full.			
Value	Operation or Status		
0	DV port FIFO is not almost full.		
1	DV port FIFO is almost full.		
Note			
The criterion is defined by the register DVFLVAFL.			

Identification	Bit Width	Expression	Default
FSTS_DVFL	1	Binary	-
Description			
Indicates the status that the DV port FIFO is full.			
Value	Operation or Status		
0	DV port FIFO is not full.		
1	DV port FIFO is full.		
Note			

Identification	Bit Width	Expression	Default
FSTS_VBNE	1	Binary	-
Description			
Indicates the status that the VBI FIFO is not empty			
Value	Operation or Status		
0	VBI FIFO is empty.		
1	VBI FIFO is not empty (data exists in one or more stage.)		
Note			

Identification	Bit Width	Expression	Default
FSTS_VBAE	1	Binary	-
Description			
Indicates the status that the VBI FIFO is almost empty.			
Value	Operation or Status		
0	VBI FIFO is not almost empty.		
1	VBI FIFO is almost empty.		
Note			
The criterion is defined by the register VBFLV_AEL			

Identification	Bit Width	Expression	Default
FSTS_VBAF	1	Binary	-
Description			
Indicates the status that the VBI FIFO is almost full.			
Value	Operation or Status		
0	VBI FIFO is not almost full.		
1	VBI FIFO is almost full.		
Note			
The criterion is defined by the register VBFLV_AFL.			

Identification	Bit Width	Expression	Default
FSTS_VBFL	1	Binary	-
Description			
Indicates the status that the VBI FIFO is full.			
Value	Operation or Status		
0	VBI FIFO is not full.		
1	VBI FIFO is full.		
Note			

MSTS_

0x04 – 0x05

Name							R/W	
Misc. Status							Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x04	NINT 1	NINT 0	NSTD	TBCE	CKON	BBON	SDET	FSCL
0x05	rsv	AGAT 2	AGAT 1	AGAT 0	rsv	PJCON	VCXO 1	VCXO 0

Identification	Bit Width	Expression	Default
MSTS_FSCL	1	Binary	-
Description			
Indicates that internally generated color cub-carrier has locked-in with that of the input video signal.			
Value	Operation or Status		
0	Not locked-in		
1	Locked-in		
Note			
Not effective when the video mode is SECAM			

Identification	Bit Width	Expression	Default
MSTS_SDET	1	Binary	-
Description			
Indicates sync has detected in the input video signal.			
Value	Operation or Status		
0	Sync not detected		
1	Sync detected		
Note			

Identification	Bit Width	Expression	Default
MSTS_BBON	1	Binary	-
Description			
Indicates the blue-back is being displayed.			
Value	Operation or Status		
0	Blue-back is not being displayed.		
1	Blue-back is being displayed.		
Note			

Identification	Bit Width	Expression	Default
MSTS_CKON	1	Binary	-
Description			
Indicates that the color killer circuit is working.			
Value	Operation or Status		
0	Color killer is not working.		
1	Color killer is working.		
Note			

Identification	Bit Width	Expression	Default
MSTS_TBCE	1	Binary	-
Description			
Indicates that TBC error is occurring. (TBC memory overflow occurred)			
Value	Operation or Status		
0	TBC error not occurred.		
1	TBC error occurred.		
Note			

Identification	Bit Width	Expression	Default
MSTS_NSTD	1	Binary	-
Description			
Indicates that the input video signal is a non-standard signal.			
Value	Operation or Status		
0	Non-standard signal is not being received.		
1	Non-standard signal is being received.		
Note			
Here, non-standard means the signal whose number of lines deviates from the standard.			

Identification	Bit Width	Expression	Default
MSTS_NINT	2	Binary	-
Description			
Indicates that the input video signal is non-interlaced.			
Value	Operation or Status		
0	Non-interlaced signal is not received.		
1	Non-interlaced signal is not received.		
2	Non-interlaced signal is received (continuous odd field.)		
3	Non-interlaced signal is received (continuous even field.)		
Note			

Identification	Bit Width	Expression	Default
MSTS_VCXO	2	Binary	-
Description			
Indicates the status of VCXO operation.			
Value	Operation or Status		
0	Free run operation		
1	Burst lock VCXO operation		
2	H-lock (line-lock) VCXO operation		
3	Reserved		
Note			

Identification	Bit Width	Expression	Default
MSTS_PJCON	1	Binary	-
Description			
Indicates if PJC filter in operation or not.			
Value	Operation or Status		
0	PJC filter OFF		
1	PJC filter on		
Note			

Identification	Bit Width	Expression	Default
MSTS_AGAT	3	Binary	-
Description			
Indicates analog gain level currently set			
Value	Operation or Status		
0 - 7	Analog gain		
Note			
Effective only at the time analog AGC in operation			

WSSTS_

0x06

Name							R/W	
Wide Screen Status							Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x06	DETE	DETO	ASPE 1	ASPE 0	POS	FORM	ASPO 1	ASPO 0

Identification	Bit Width	Expression	Default
WSSTS_ASPO	2	Binary	-
Description			
Indicates the aspect ratio of odd-field.			
Value	Operation or Status		
0	4:3		
1	14:9		
2	16:9		
3	>16:9		
Note			
Above value is set when WSS is detected while receiving the PAL signal. While the NTSC signal is applied, the bits are set when CGMS is detected as follows: WSSTS_ASPO[0] : CGMS Word0 bit1 (Odd Field) WSSTS_ASPO[1] : CGMS Word0 bit2 (Odd Field) The values are only valid when the register WSSTS_DETO is '1' while either NTSC or PAL signal is being received.			

Identification	Bit Width	Expression	Default
WSSTS_FORM	1	Binary	-
Description			
Indicates the format of WSS.			
Value	Operation or Status		
0	Full		
1	Letter Box		
Note			

Above value is set when WSS is detected while receiving the PAL signal. Ineffective when receiving the NTSC signal. Effective only when the register WSSTS_DETO is '1'.

Identification	Bit Width	Expression	Default
WSSTS_POS	1	Binary	-
Description			
Indicates the position of WSS.			
Value	Operation or Status		
0	Center		
1	Top		
Note			
Above value is set when WSS is detected while receiving the PAL signal. Ineffective when receiving the NTSC signal. Effective only when the register WSSTS_DETO is '1'.			

Identification	Bit Width	Expression	Default
WSSTS_ASPE	2	Binary	-
Description			
Indicates the aspect ratio of even field			
Bit	Operation or Status		
0	CGMS Word0 bit1 (Even Field)		
1	CGMS Word0 bit2 (Even Field)		
Note			
Above value is set when CGMS is detected while receiving the NTSC signal. Ineffective when receiving the PAL signal. Effective only when the register WSSTS_DETE is '1'.			

Identification	Bit Width	Expression	Default
WSSTS_DETO	1	Binary	-
Description			
Indicates whether the odd-field information on WSSTS_ is effective or ineffective.			
Value	Operation or Status		
0	Ineffective		
1	Effective		
Note			

Identification	Bit Width	Expression	Default
WSSTS_DETE	1	Binary	-
Description			
Indicates that the even-field information on WSSTS_ is effective or ineffective.			
Value	Operation or Status		
0	Ineffective		
1	Effective		
Note			

VBINF_

0x07

Name							R/W	
VBI FIFO Information							Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0

0x07	VBERR	VBFNE	VBWN 1	VBWN 0	VBFLD	rsv	VBID 1	VBID 0

Identification	Bit Width	Expression	Default
VBINF_VBID	2	Binary	-
Description			
Indicates the kinds of the oldest data stored in the VBI FIFO.			
Value	Operation or Status		
0	Closed caption		
1	CGMS		
2	WSS		
3	Reserved		
Note			

Identification	Bit Width	Expression	Default
VBINF_VBFLD	1	Binary	-
Description			
Indicates the field of the oldest data stored in the VBI FIFO.			
Value	Operation or Status		
0	Odd-field		
1	Even-field		
Note			

Identification	Bit Width	Expression	Default
VBINF_VBWN	2	Binary	-
Description			
Indicates the word number of the oldest data stored in the VBI FIFO.			
Value	Operation or Status		
0	Word number = 0		
1	Word number = 1		
2	Word number = 2		
3	Reserved		
Note			
Please refer to Table 5.2 for the detail on the relation between the word number and the data.			

Identification	Bit Width	Expression	Default
VBINF_VBFNE	1	Binary	-
Description			
Indicates the existence of data stored in the VBI FIFO.			
Value	Operation or Status		
0	No data		
1	Some data		
Note			
Identification	Bit Width	Expression	Default
VBINF_VBERR	1	Binary	-
Description			
Indicates the existence of error in the oldest data stored in the VBI FIFO.			
Value	Operation or Status		
0	No error		
1	Some error		
Note			

VBRD_

0x08

Name							R/W	
VBI FIFO Read Data							Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x08	VBRD 7	VBRD 6	VBRD 5	VBRD 4	VBRD 3	VBRD 2	VBRD 1	VBRD 0

Identification	Bit Width	Expression	Default
VBRD_VBRD	8	Binary	-
Description			
Indicates the oldest data stored in the VBI FIFO.			
Value	Operation or Status		
0-255	VBI data (refer to Table 5.2.)		
Note			
The data will be de-queued from the VBI FIFO right after having read this register.			

Table 5.2 VBI FIFO register interface

Data Type	VBINF_								VBRD_							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Closed Caption, Odd Field, 1st word, No error	0	*	0	0	0		0	0	Character 1							
Closed Caption, Odd Field, 2st word, No error	0	*	0	1	0		0	0	Character 2							
Closed Caption, Even Field, 1st word, No error	0	*	0	0	1		0	0	Character 1							
Closed Caption, Even Field, 2st word, No error	0	*	0	1	1		0	0	Character 2							
Closed Caption, Odd Field, 1st word, With error	1	*	0	0	0		0	0	Character 1							
Closed Caption, Odd Field, 2st word, With error	1	*	0	1	0		0	0	Character 2							
Closed Caption, Even Field, 1st word, With error	1	*	0	0	1		0	0	Character 1							
Closed Caption, Even Field, 2st word, With error	1	*	0	1	1		0	0	Character 2							
CGMS-A, Odd Field, 1st word, No error	0	*	0	0	0		0	1	Word1							Word0
CGMS-A, Odd Field, 2nd word, No error	0	*	0	1	0		0	1	Word2							
CGMS-A, Odd Field, 3rd word, No error	0	*	1	0	0		0	1			CRC					
CGMS-A, Even Field, 1st word, No error	0	*	0	0	1		0	1	Word1							Word0
CGMS-A, Even Field, 2nd word, No error	0	*	0	1	1		0	1	Word2							
CGMS-A, Even Field, 3rd word, No error	0	*	1	0	1		0	1			CRC					
CGMS-A, Odd Field, 1st word, With error	1	*	0	0	0		0	1	Word1							Word0
CGMS-A, Odd Field, 2nd word, With error	1	*	0	1	0		0	1	Word2							
CGMS-A, Odd Field, 3rd word, With error	1	*	1	0	0		0	1			CRC					
CGMS-A, Even Field, 1st word, With error	1	*	0	0	1		0	1	Word1							Word0
CGMS-A, Even Field, 2nd word, With error	1	*	0	1	1		0	1	Word2							
CGMS-A, Even Field, 3rd word, With error	1	*	1	0	1		0	1			CRC					
WSS, Odd Field, 1st word, No error	0	*	0	0	0		1	0	Group2				Group1			
WSS, Odd Field, 2nd word, No error	0	*	0	1	0		1	0		Group4				Group3		
WSS, Even Field, 1st word, No error	0	*	0	0	1		1	0	Group2				Group1			
WSS, Even Field, 2nd word, No error	0	*	0	1	1		1	0		Group4				Group3		
WSS, Odd Field, 1st word, With error	1	*	0	0	0		1	0	Group2				Group1			
WSS, Odd Field, 2nd word, With error	1	*	0	1	0		1	0		Group4				Group3		
WSS, Even Field, 1st word, With error	1	*	0	0	1		1	0	Group2				Group1			
WSS, Even Field, 2nd word, With error	1	*	0	1	1		1	0		Group4				Group3		

DCCD_

0x09

Name							R/W	
Detected Copy Control Data							Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x09	CSTYP	CSDET	AGCP	PSDET	rsv	rsv	DCCD 1	DCCD 0
Note								
For details of copy control data, please refer to Macrovision.								

Identification	Bit Width	Expression	Default
DCCD_DCCD	2	Binary	-
Description			
Indicates copy control data			
Value	Operation or Status		
0	Copy control data=0		

1	Copy control data=1
2	Copy control data=2
3	Copy control data=3
Note	

Identification	Bit Width	Expression	Default
DCCD_PSDET	1	Binary	-
Description			
Individual indication of copy control data			
Value	Operation or Status		
0	Without any copy control data event		
1	With certain copy control data events		
Note			

Identification	Bit Width	Expression	Default
DCCD_AGCP	1	Binary	-
Description			
Individual indication of copy control data event			
Value	Operation or Status		
0	Without any copy control data event		
1	With certain copy control data events		
Note			

Identification	Bit Width	Expression	Default
DCCD_CSDET	1	Binary	-
Description			
Individual indication of copy control data event			
Value	Operation or Status		
0	Without any copy control data event		
1	With certain copy control data events		
Note			

Identification	Bit Width	Expression	Default
DCCD_CSTYP	1	Binary	-
Description			
Individual copy control data event			
Value	Operation or Status		
0	Without any copy control data event		
1	With certain copy control data events		
Note			

FIRQ_

0x0A

Name							R/W	
FIFO Interrupt Request							Read/Write(reset)	
Address	D7	D6	D5	D4	D3	D2	D1	D0

0x0A	VBOV	VBAF	VBAE	VBNE	DVOV	DVAF	DVAE	DVNE

Note

This register displays and resets the interrupt requests. To reset any interrupt request in this register, reset it before resetting the MIRQ_ register (Even when there is no need to reset the interrupt request in the MIRQ_ register, it must be effectively reset by writing a data 0x00.)

Identification	Bit Width	Expression	Default
FIRQ_DVNE	1	Binary	-

Description

DV port FIFO non-empty interrupt event.
This interrupt event occurs when the status of the DV port FIFO changed from “empty” to “non-empty” (data exists in one or more stage.)

Value	Operation or Status
0	The event has not occurred.
1	The event has occurred.

Note

Writing "1" into this bit will reset the interrupt request.

Identification	Bit Width	Expression	Default
FIRQ_DVAE	1	Binary	-

Description

DV port FIFO almost empty interrupt event.
This interrupt event occurs when the status of the DV port FIFO changed from “not almost empty” to “almost-empty”

Value	Operation or Status
0	The event has not occurred.
1	The event has occurred.

Note

Writing "1" into this bit will reset the interrupt request.
(The criterion on “almost” is specified by the register DVFLV_AEL)

Identification	Bit Width	Expression	Default
FIRQ_DVAF	1	Binary	-

Description

DV port FIFO almost full interrupt event.
This interrupt event occurs when the status of the DV port FIFO changed from “not almost full” to “almost full”.

Value	Operation or Status
0	The event has not occurred.
1	The event has occurred.

Note

Writing "1" into this bit will reset the interrupt request.
(The criterion on “almost” is specified by the register DVFLV_AFL)

Identification	Bit Width	Expression	Default
FIRQ_DVOV	1	Binary	-

Description

DV port FIFO Overflow interrupt event.
This interrupt event occurs when the status of the DV port FIFO changed from “not full” to “full”.

Value	Operation or Status
0	The event has not occurred.
1	The event has occurred.

Note

Writing "1" into this bit will reset the interrupt request.

Identification	Bit Width	Expression	Default
FIRQ_VBNE	1	Binary	-
Description			
VBI FIFO not empty interrupt event. This interrupt event occurs when the status of the VBI FIFO changed from “empty” to “non-empty” (data exists in one or more stage.)			
Value	Operation or Status		
0	The event has not occurred.		
1	The event has occurred.		
Note			
Writing "1" into this bit will reset the interrupt request.			

Identification	Bit Width	Expression	Default
FIRQ_VBAE	1	Binary	-
Description			
VBI FIFO almost empty interrupt event. This interrupt event occurs when the status of the VBI FIFO changed from “not almost empty” to “almost empty”.			
Value	Operation or Status		
0	The event has not occurred.		
1	The event has occurred.		
Note			
Writing "1" into this bit will reset the interrupt request. (The criterion on “almost” is specified by the regisgter VBFLV_AEL.)			

Identification	Bit Width	Expression	Default
FIRQ_VBAF	1	Binary	-
Description			
VBI FIFO almost full interrupt event. This interrupt event occurs when the status of the VBI FIFO changed from “not almost full” to “almost full”.			
Value	Operation or Status		
0	The event has not occurred.		
1	The event has occurred.		
Note			
Writing "1" into this bit will reset the interrupt request. (The criterion on “almost” is specified by the register VBFLV_AFL)			

Identification	Bit Width	Expression	Default
FIRQ_VBOV	1	Binary	-
Description			
VBI FIFO Overflow interrupt event. This interrupt event occurs when the status of the VBI FIFO changed from “not full” to “full”.			
Value	Operation or Status		
0	The event has not occurred.		
1	The event has occurred.		
Note			
Writing "1" into this bit will reset the interrupt request.			

MIRQ_

0x0B

Name							R/W	
Misc. Interrupt Request							Read/Write(reset)	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x0B	DCCD	NINT	INT	NSTD	STD	NSDET	SDET	VMCLM

Note

This register displays and resets the interrupt requests. To reset the interrupt request in this register, reset the interrupt request in the FIRQ_ register first before resetting this register (This rule does not apply if interrupt request in the FIRQ_ register needs not be reset.)

Identification	Bit Width	Expression	Default
MIRQ_VMCLM	1	Binary	-

Description

Video mode (video system) changed interrupt event.
This interrupt event occurs when the video mode changed.

Value	Operation or Status
0	The event has not occurred.
1	The event has occurred.

Note

Writing "1" into this bit will reset the interrupt request.

Identification	Bit Width	Expression	Default
MIRQ_SDET	1	Binary	-

Description

Sync detection interrupt event.
This interrupt event occurs when the status of sync detection changed from “not detected” to “detected”.

Value	Operation or Status
0	The event has not occurred.
1	The event has occurred.

Note

Writing "1" into this bit will reset the interrupt request.

Identification	Bit Width	Expression	Default
MIRQ_NSDET	1	Binary	-

Description

Out-of-sync interrupt event.
This interrupt event occurs when the status of sync detection changed from “detected” to “not detected”.

Value	Operation or Status
0	The event has not occurred.
1	The event has occurred.

Note

Writing "1" into this bit will reset the interrupt request.

Identification	Bit Width	Expression	Default
MIRQ_STD	1	Binary	-

Description

Standard signal detected interrupt event. This interrupt event occurs when the status of standard signal detection changed from “not detected” to “detected” in the input video signal.	
Value	Operation or Status
0	The event has not occurred.
1	The event has occurred.
Note	
Writing "1" into this bit will reset the interrupt request.	

Identification	Bit Width	Expression	Default
MIRQ_NSTD	1	Binary	-
Description			
Standard signal not detected interrupt event. This interrupt event occurs when the status of standard signal detection changed from “detected” to “not detected” in the input video signal.			
Value	Operation or Status		
0	The event has not occurred.		
1	The event has occurred.		
Note			
Writing "1" into this bit will reset the interrupt request.			

Identification	Bit Width	Expression	Default
MIRQ_INT	1	Binary	-
Description			
Non-interlaced scan not detected interrupt event. This interrupt event occurs when the status of non-interlaced signal changed from “detected” to “not detected” in the input video signal.			
Value	Operation or Status		
0	The event has not occurred.		
1	The event has occurred.		
Note			
Writing "1" into this bit will reset the interrupt request.			

Identification	Bit Width	Expression	Default
MIRQ_NINT	1	Binary	-
Description			
Interrupt event due change in copy control data. An interrupt caused by the change in copy control data.			
Value	Operation or Status		
0	Such interrupt event not taking place.		
1	Such interrupt event took place.		
Note			
Writing "1" into this bit will reset the interrupt event.			

Identification	Bit Width	Expression	Default
MIRQ_DCCD	1	Binary	-
Description			
Copy control data changed interrupt event This is the Interrupt taken place when copy control data has changed.			
Value	Operation or Status		
0	Such interrupt event not taking place.		
1	Such interrupt event took place.		
Note			
Writing "1" into this bit will reset the interrupt event.			

GPIOD_

0x0C – 0x0D

Name							R/W	
General Purpose IO Read Write Data							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x0C	GPIOD 7	GPIOD 6	GPIOD 5	GPIOD 4	GPIOD 3	GPIOD 2	GPIOD 1	GPIOD 0
0x0D	rsv	rsv	rsv	rsv	rsv	rsv	GPIOD 9	GPIOD 8

Identification	Bit Width	Expression	Default
GPIOD_GPIOD	10	Binary	0x000

Description

This register is accessed when GPIO is set to register IO mode. The register GPDIR_GPDIR specifies Read/Write direction for each bit.
Data written into the bits specified as Read are ignored.
Data read from the bits specified as Write will be the read-back data previously written in.
In addition, when the register GPDIR_SIN is "1", read the GPIO's lower 8 bits first before reading the lower 2 bits. Similarly, when the register GPDIR_SOUT is "1", write the GPIO's lower 8 bits first before writing the lower 2 bits.

Bit	Operation or Status
0	Read or write to GPIO0 pin.
1	Read or write to GPIO1 pin.
2	Read or write to GPIO2 pin.
3	Read or write to GPIO3 pin.
4	Read or write to GPIO4 pin.
5	Read or write to GPIO5 pin.
6	Read or write to GPIO6 pin.
7	Read or write to GPIO7 pin.
8	Read or write to GPIO8 pin.
9	Read or write to GPIO9 pin.

Note

The register IO mode settings should be as follows:
For the lower 8 bits of the GPIO pins: GPMD_GPSOL='0'
For the upper 2 bits of the GPIO pins: GPMD_GPSOH='0'

5.2.2. Picture Tuning

CONT_

0x10

Name							R/W	
Contrast Trimmer							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x10	CONT 7	CONT 6	CONT 5	CONT 4	CONT 3	CONT 2	CONT 1	CONT 0

Identification	Bit Width	Expression	Default
CONT_CONT	8	2's complement	0x00
Description			
This register is used to adjust contrast.			
Value	Operation or Status		
-128 to +127	Enter a larger number for stronger contrast, and a smaller number for weaker contrast, with zero (0) at its center.		
Note			

BRTT_

0x11

Name							R/W	
Brightness Trimmer							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x11	BRTT 6	BRTT 5	BRTT 4	BRTT 3	BRTT 2	BRTT 1	BRTT 0	rsv

Identification	Bit Width	Expression	Default
BRTT_BRTT	7	2's complement	0x00
Description			
This register is used to adjust brightness.			
Value	Operation or Status		
-64 to +63	Enter a larger number for stronger brightness, and a smaller number for weaker brightness, with zero (0) at its center.		
Note			

APCOR_

0x12

Name							R/W	
Aperture Correction							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x12	CORG 1	CORG 0	rsv	WEIT 2	WEIT 1	WEIT 0	APBW 1	APBW 0

Identification	Bit Width	Expression	Default

APCOR_APBW	2	Binary	0x0
Description			
This register is used to choose the frequency response of aperture correction. As for the frequency characteristics, please refer to Figure 4.19.			
Value	Operation or Status		
0	Reserved		
1	Refer to the frequency characteristics		
2	Refer to the frequency characteristics		
3	Refer to the frequency characteristics		
Note			

Identification	Bit Width	Expression	Default
APCOR_WEIT	3	Binary	0x0
Description			
This register is used to choose the strength (weight) of enhancement.			
Value	Operation or Status		
0 to 7	The larger the setting, the stronger the aperture correction.		
Note			

Identification	Bit Width	Expression	Default
APCOR_CORG	2	Binary	0x0
Description			
This register chooses the way the coring works in order to suppress the noisiness caused by aperture correction. For the coring characteristics, please refer to the Figure 4.20.			
Value	Operation or Status		
0	Coring is OFF		
1	4-bit		
2	5-bit		
3	6-bit		
Note			
Figure 4.20 shows the coring characteristics on the correction components.			

CLMK_

0x13 – 0x15

Name							R/W	
Color Level Trimmer							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x13	CHRMK 7	CHRMK 6	CHRMK 5	CHRMK 4	CHRMK 3	CHRMK 2	CHRMK 1	CHRMK 0
0x14	COLUM 7	COLUM 6	COLUM 5	COLUM 4	COLUM 3	COLUM 2	COLUM 1	COLUM 0
0x15	COLVM 7	COLVM 6	COLVM 5	COLVM 4	COLVM 3	COLVM 2	COLVM 1	COLVM 0

Identification	Bit Width	Expression	Default
CLMK_CHRMK	8	2's complement	0x00
Description			
This register is used to adjust the gain of the chroma components in video signal. For the input other than component or SECAM signal, the color density is adjustable, however, use of CLMK_COLUM and CLMK_COLVM is recommended.			
Value	Operation or Status		

-128 to 127	The larger the setting, the stronger the gain, the smaller the setting the weaker the gain, with zero (0) as its center.
Note	
This register should be set to zero (0) when decoding SECAM. When applying component signal, this register becomes disabled.	

Identification	Bit Width	Expression	Default
CLMK_COLUM	8	2's complement	0x00
Description			
This register is used to adjust U gain after chroma decoding. This register can be used for color density adjustment together with the register CLMK_COLVM.			
Value	Operation or Status		
-128 to 127	The larger the setting, the stronger the gain, the smaller the setting the weaker the gain, with zero (0) as its center.		
Note			
When component signal being applied, the gain center is 64.			

Identification	Bit Width	Expression	Default
CLMK_COLVM	8	2's complement	0x00
Description			
This register adjusts V gain after chroma decoding. This register can be used for color density adjustment together with the register CLMK_COLUM.			
Value	Operation or Status		
-128 to 127	The larger the setting, the stronger the gain, the smaller the setting the weaker the gain, with zero (0) as its center.		
Note			
When component signal being applied, the gain center is 64.			

HUET_

0x16 – 0x17

Name							R/W	
Hue Trimmer							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x16	HUET 1	HUET 0	rsv	UVOF 4	UVOF 3	UVOF 2	UVOF 1	UVOF 0
0x17	HUET 9	HUET 8	HUET 7	HUET 6	HUET 5	HUET 4	HUET 3	HUET 2

Identification	Bit Width	Expression	Default
HUET_UVOF	5	Binary	0x00
Description			
This register is used to give offset to the phase variance between UV decoding axes (standard 90 degree.) Offset between zero (0) and approx. 31 degree can be specified.			
Value	Operation or Status		
0 to 31	Offset amount = HUET_UVOF* approx. 1 degree		
Note			

Identification	Bit Width	Expression	Default
HUET_HUET	10	2's complement	0x000
Description			

This register gives offset to the color sub-carrier phase and the decoding axes. Hue trimming can be applied between -180 degree and +179.6 degree, with zero (0) at its center.	
Value	Operation or Status
-512 to 511	Amount of hue trimming ＝HUET_HUET*360/1024 degree
Note	
The hue trimming is furnished for use when decoding the video signals of NTSC color modulation (color_mode=0.) Usually, hue trimming is impossible for color modulation based on PAL or SECAM in principle; however, the XV750C can emulate hue trimming when using PAL color modulation (color_mode=1.) In case of SECAM, any value in this register will be neglected.	

TRPFCHR_

0x18

Name							R/W	
TRAP Filter Characteristics							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x18	rsv	rsv	rsv	rsv	rsv	rsv	CHRS 1	CHRS 0

Identification	Bit Width	Expression	Default
TRPFCHR_CHRS	2	Binary	0x2
Description			
This register selects the frequency characteristics of the trap filter used for Y/C separation. Refer to Figure 4.13, Figure 4.14 and Figure 4.15 for the frequency characteristics.			
Value	Operation or Status		
0	Refer to the frequency characteristics		
1	Refer to the frequency characteristics		
2	Refer to the frequency characteristics		
3	Refer to the frequency characteristics		
Note			

BPFCHR_

0x19

Name							R/W	
Band Pass Filter Characteristics							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x19	rsv	rsv	rsv	rsv	rsv	CHRS 2	CHRS 1	CHRS 0

Identification	Bit Width	Expression	Default
BPFCHR_CHRS	3	Binary	0x0
Description			
This register chooses the frequency characteristics of the band-pass filter used for Y/C separation. Refer to Figure4.11 and Figure 4.12 for the frequency characteristics.			
Value	Operation or Status		
0	Refer to the frequency characteristics		
1	Refer to the frequency characteristics		

2	Refer to the frequency characteristics
3	Refer to the frequency characteristics
4	Refer to the frequency characteristics
5	Refer to the frequency characteristics
6	Refer to the frequency characteristics
7	Refer to the frequency characteristics
Note	

BELCHR_

0x1A

Name							R/W	
BELL Filter Characteristics							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x1A	rsv	rsv	SHAP 1	SHAP 0	rsv	rsv	SIFT 1	SIFT 0

Identification	Bit Width	Expression	Default
BELCHR_SIFT	2	Binary	0x0
Description			
This register chooses the frequency characteristics (shift) of the bell filter used in SECAM decoding circuit.			
Value	Operation or Status		
0	Recommended characteristic		
1	Reserved		
2	Reserved		
3	Reserved		
Note			
Please use at the default value.			

Identification	Bit Width	Expression	Default
BELCHR_SHAP	2	Binary	0x0
Description			
This register is used to choose the frequency characteristics (shape) of the bell filter used in SECAM decoding circuit.			
Value	Operation or Status		
0	Recommended characteristic		
1	Reserved		
2	Reserved		
3	Reserved		
Note			
Please use at the default value.			

DEMPCHR_

0x1B

Name							R/W	
De-Emphasis Filter Characteristics							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x1B	rsv	rsv	rsv	rsv	rsv	rsv	CHRS 1	CHRS 0

Identification	Bit Width	Expression	Default
DEMPCHR_CHRS	2	Binary	0x0
Description			
This register chooses the frequency characteristics of the de-emphasis filter used in SECAM decoding circuit.			
Value	Operation or Status		
0	Recommended characteristic		
1	Reserved		
2	Reserved		
3	Reserved		
Note			
Please use at the default value.			

PROFLT_

0x1C – 0x1D

Name							R/W	
Programmable Filter Parameter Setting							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x1C	ADRS 7	ADRS 6	ADRS 5	ADRS 4	ADRS 3	ADRS 2	ADRS 1	ADRS 0
0x1D	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0

Identification	Bit Width	Expression	Default
PROFLT_ADRS	8	Binary	0x00
Description			
This register specifies the address of the data register for the programmable filter.			
Value	Operation or Status		
0 to 255	Register's address for the programmable filter (See Table 4.6)		
Note			
Before writing any data into this register, a register's address of the programmable fileter must be specified to the register PROFLT_DATA.			

Identification	Bit Width	Expression	Default
PROFLT_DATA	8	Binary	0x00
Description			
This register specifies the data for the register of the programmable filter.			
Value	Operation or Status		
0 to 255	Programmable filter data. (Please refer to the Table 4.6)		
Note			
Before writing any data into this register, a register's address of the programmable fileter must be specified to the register PROFLT_ADRS.			

VENHANC_

0x1E

Name							R/W	
Virtical Enhancer							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0

0x12	CORG 1	CORG 0	rsv	WEIT 2	WEIT 1	WEIT 0	rsv	ENB

Identification	Bit Width	Expression	Default
VENHANC_ENB	1	Binary	0x0
Description			
This register selects ON/OFF of the vertical aperture correction.			
Value	Operation or Status		
0	OFF		
1	ON		
Note			

Identification	Bit Width	Expression	Default
VENHANC_WEIT	3	Binary	0x0
Description			
This register specifies the degree (weight) of vertical aperture correction.			
Value	Operation or Status		
0 to 7	The larger the set number, the stronger the aperture correction applies.		
Note			

Identification	Bit Width	Expression	Default
VENHANC_CORG	2	Binary	0x0
Description			
This register selects the coring function to surpress the noise in aperture correction. As for the coring characteristics, please refer to Figure 4.20.			
Value	Operation or Status		
0	Coring OFF		
1	4 bits		
2	5 bits		
3	6 bits		
Note			
Figure 4.20 shows the coring characteristics for the correction element.			

5.2.3. Configuration

AIMS_

0x20

Name							R/W	
Analog Input MUX Selection							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x20	rsv	rsv	rsv	rsv	rsv	rsv	SELP 1	SELP 0

Identification	Bit Width	Expression	Default
AIMS_SELP	2	Binary	0x0
Description			
This register selects analog input line. The value corresponds to "m" in "AINnm" that denotes the analog video signal input pins.			
Value	Operation or Status		
0	Select AINn0 pin		
1	Select AINn1 pin		
2	Select AINn2 pin		
3	Select AINn3 pin		
Note			

ATVM_

0x21

Name							R/W	
Automatic Video Mode Settings							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x21	FULL	VSTD 6	VSTD 5	VSTD 4	VSTD 3	VSTD 2	VSTD 1	VSTD 0

Identification	Bit Width	Expression	Default
ATVM_VSTD	7	Binary	0x7F
Description			
This register specifies the video standard to be switched automatically according to the video standard (video system) of the input video signal. Automatic switching can be specified independently by setting "1" to the bit that corresponds to the video system. For example, to make only PAL-B, D, G, H, I, N and SECAM automatic, set the register ATVM_VSTD to "0x06". Please refer to "4.17 Video Standard Detection/Automatic Switching Circuit " on page 68 for the detail.			
Bit	Operation or Status		
0	NTSC-M, NTSC-Japan		
1	PAL-B,D,G,H.I,N		
2	SECAM		
3	PAL-M		
4	PAL-CombinationN		
5	NTSC-4.43		
6	PAL-60		
Note			
To set the video system manually using the register MNVM_MOD[4:0] , please set the registers ATVM_VSTD=0x00, ATVM_FULL='0'.			

Identification	Bit Width	Expression	Default
ATVM_FULL	1	Binary	0x0
Description			
This register specifies automatic switching for all the video standards, instead of setting one by one using the register ATVM_VSTD.			
Value	Operation or Status		
0	Register ATVM_VSTD is effective.		
1	Fully automatic (registers ATVM_VSTD and MNVM_MOD are ineffective)		
Note			

MNVM_

0x22

Name							R/W	
Manual Video Mode Settings							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x22	MOD 7	MOD 6	MOD 5	MOD 4	MOD 3	MOD 2	MOD 1	MOD 0
Note								
The register MNVM_MOD[4:0] is effective only when the registers are set as follow: ATVM_VSTD=0x00 and ATVM_FULL='0'. When the register MNVM_MOD[4:0] is effective, the VS color killer (refer to "4.16.16 Color Killer Event" on page 68) will not function, regardless of the result of video system judgment.								

Identification	Bit Width	Expression	Default
MNVM_MOD[0]	1	Binary	0x0
Description			
This register specifies the scan mode of the video standard manually.			
Value	Operation or Status		
0	59.94Hz/525Line		
1	50Hz/625Line		
Note			

Identification	Bit Width	Expression	Default
MNVM_MOD[2:1]	2	Binary	0x0
Description			
This register specifies the color mode (color modulation mode) of the video standard manually.			
Value	Operation or Status		
0	NTSC		
1	PAL		
2	Reserved		
3	SECAM		
Note			
This register is ineffective when component signal is being input.			

Identification	Bit Width	Expression	Default
MNVM_MOD[4:3]	2	Binary	0x0
Description			

This register specifies the Fsc mode (color sub-carrier frequency) of the video standard manually.	
Value	Operation or Status
0	3.579545MHz
1	4.4361875MHz
2	3.57561149MHz
3	3.58205625MHz
Note	
This register is ineffective when component signal is being input.	

Identification	Bit Width	Expression	Default
MNVM_MOD[5]	1	Binary	0x0
Description			
This register specifies the set-up mode (for NTSC-M and NTSC-Japan) of the video standard. NTSC-M: 1 NTSC-Japan: 0			
Value	Operation or Status		
0	None		
1	7.5IRE		
Note			
This register is effective whenever the decoding video system is NTSC-M or NTSC-Japan, regardless of automatic/manual setting of the video standard. Please note that this register becomes ineffective when component signal being fed.			

Identification	Bit Width	Expression	Default
MNVM_MOD[6]	1	Binary	0x0
Description			
This register specifies the setup mode (for PAL-B, D, G, H, I, N) of the video standard manually. Normally, set as follows: PAL-B, D, G, H, I: 0 PAL-N: 1			
Value	Operation or Status		
0	None		
1	7.5%		
Note			
This register is effective whenever the decoding video system is PAL-B, D, G, H, I or PAL-N, regardless of automatic/manual setting of the video standard. Please note that this register becomes ineffective when component signal being fed.			

Identification	Bit Width	Expression	Default
MNVM_MOD[7]	1	Binary	0x1
Description			
This register specifies the setup mode (for PAL-M) of the video standard manually. Usually, please set the register at the default value.			
Value	Operation or Status		
0	None		
1	7.5%		
Note			
This register is effective when the decoding video system is PAL-M. Please note that this register becomes ineffective when component signal being fed.			

COMBDEF_

0x23 - 0x24

Name							R/W	
Comb Filter Definition							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x23	rsv	rsv	PAFS	PCOMB	rsv	ACMS	BPFS	COMS
0x24	P3HT 3	P3HT 2	P3HT 1	P3HT 0	P3LT 3	P3LT 2	P3LT 1	P3LT 0

Identification	Bit Width	Expression	Default
COMBDEF_COMS	1	Binary	0x0
Description			
This register selects the comb filter operation in the Y/C separation circuit. Usually, please use at the default value.			
Value	Operation or Status		
0	Adaptive comb filter		
1	Fixed comb filter		
Note			
Please refer to the Table 4.5.			

Identification	Bit Width	Expression	Default
COMBDEF_BPFS	1	Binary	0x0
Description			
This register selects the band-pass filter for comb filter operation in the Y/C separation circuit. Usually, please use at the default value.			
Value	Operation or Status		
0	BPF dedicated for comb filter operation		
1	BPF for chrominance signals		
Note			

Identification	Bit Width	Expression	Default
COMBDEF_ACMS	1	Binary	0x1
Description			
This register chooses a Y/C separation filter to use, when a video signal is input that is judged to have no color burst correlation, when the adaptive comb filter is used in Y/C separation circuit.			
Value	Operation or Status		
0	Trap band-pass filter		
1	Fixed comb filter		
Note			

Identification	Bit Width	Expression	Default
COMBDEF_PCOMB	1	Binary	0x1
Description			
This register is to choose the post-comb filter for PAL. Usually, please use at the default value.			
Value	Operation or Status		
0	Not to use		
1	Use		
Note			
This register becomes effective only for the PAL video signal input.			

Identification	Bit Width	Expression	Default

COMBDEF_PAFS	1	Binary	0x0
Description			
This register is to choose the type of adaptive filter for PAL			
Value	Operation or Status		
0	Adaptive 5-line comb filter		
1	Adaptive 3-line hybrid filter		
Note			
This register becomes not effective unless in PAL mode. Please refer to Table 4.5.			

Identification	Bit Width	Expression	Default
COMBDEF_P3LT	4	Binary	0xB
Description			
For PAL 3 lines comb (hybrid) filter image adjustment			
Value	Operation or Status		
0 to 0xF	Higher trimmer		
Note			

Identification	Bit Width	Expression	Default
COMBDEF_P3HT	4	Binary	0xC
Description			
[illegible] lines comb (hybrid) filter image adjustment			
Value	Operation or Status		
0 to 0xF	Lower trimmer		
Note			

AGCDEF_

0x26 – 0x29

Name							R/W	
Automatic Gain Control Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x26	rsv	rsv	LMT	FRZ	rsv	rsv	MOD 1	MOD 0
0x27	AGMK 7	AGMK 6	AGMK 5	AGMK 4	AGMK 3	AGMK 2	AGMK 1	AGMK 0
0x28	rsv	rsv	rsv	rsv	rsv	AGTC 2	AGTC 1	AGTC 0
0x29	rsv	rsv	rsv	rsv	rsv	rsv	HVSL 1	HVSL 0

Identification	Bit Width	Expression	Default
AGCDEF_MOD	2	Binary	0x2
Description			
This is the register to set the AGC operation mode.			
Value	Operation or Status		
0	Fixed gain (gain value set to the register)		
1	Digital AGC operation (Analog gain fixed to the value set to the register)		
2	Analog and digital AGC operation (max input level 120%)		
3	Analog and digital AGC operation (max input level 200%)		
Note			

Identification	Bit Width	Expression	Default
AGCDEF_FRZ	1	Binary	0x0
Description			
This is the register to freeze the AGC operation.			
Value	Operation or Status		
0	AGC is active.		
1	AGC is freeze.		
Note			
This register is ineffective when the AGC operation is in fixed-gain mode (register AGCDEF_MOD='0')			

Identification	Bit Width	Expression	Default
AGCDEF_LMT	1	Binary	0x1
Description			
This is the register to apply a limiter to AGC operation.			
Value	Operation or Status		
0	Limiter OFF		
1	Limiter ON		
Note			
This register is ineffective when the AGC operation is in fixed-gain mode (register AGCDEF_MOD='0'.)			

Identification	Bit Width	Expression	Default
AGCDEF_AGMK	8	2's complement	0x00
Description			
This is the register to set the AGC reference level. Usually, use the default value.			
Value	Operation or Status		
-128 to +127	The reference level goes down if the value turns to minus, goes up if it turns to plus, based on zero (0) as its center.		
Note			
This register is ineffective when the AGC operation is in fixed-gain mode (register AGCDEF_MOD='0')			

Identification	Bit Width	Expression	Default
AGCDEF_AGTC	3	Binary	0x5
Description			
This is the register to set the AGC time constant. Usually, use the default value.			
Value	Operation or Status		
0 to 7	The time constant is maximum at zero (0) and minimum at 7.		
Note			
This register is ineffective when the AGC operation is in fixed-gain mode (register AGCDEF_MOD='0')			

Identification	Bit Width	Expression	Default
AGCDEF_HVSL	2	Binary	0x2
Description			
This register is to set the HV reduction mode for AGC.			
Value	Operation or Status		
0	Standard		
1	HV reduction mode		
2,3	Automatic		
Note			
This register is ineffective when the AGC operation is in fixed-gain mode (register AGCDEF_MOD='0')			

PAGCC_

0x2A – 0x2C

Name							R/W	
Peak AGC Control							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x2A	PAGM 7	PAGM 6	PAGM 5	PAGM 4	PAGM 3	PAGM 2	PAGM 1	PAGM 0
0x2B	rsv	rsv	rsv	rsv	SETM	SETC 2	SETC 1	SETC 0
0x2C	REOFS 3	REOFS 2	REOFS 1	REOFS 0	rsv	RETC 2	RETC 1	RETC 0

Identification	Bit Width	Expression	Default
PAGCC_PAGM	8	2's complement	0x7F
Description			
This register is to specify the threshold level for the peak AGC. Usually, use the default value.			
Value	Operation or Status		
-128 to 127	If shifting to negative direction, peak AGC threshold level comes down working for better peak AGC efficiency. Vice versa, if shifting to the positive direction, threshold level going up making peak AGC less effective.		
Note			

Identification	Bit Width	Expression	Default
PAGCC_SETC	3	Binary	0x4
Description			
This register specifies set-up time constant for the peak AGC. Usually, please use at the default value.			
Value	Operation or Status		
0 to 7	0 for the maximum time constant, 7 for the minimum.		
Note			

Identification	Bit Width	Expression	Default
PAGCC_SETM	1	Binary	0x0
Description			
This register specifies set-up time constant mode for the peak AGC. Usually, please use at the default value.			
Value	Operation or Status		
0	The register PAGCC_SETC becomes effective as Peak AGC set-up time constant.		
1	Irrelevant to the value in the register PAGCC_SETC, this register sets the Peak AGC set-up time constant automatically.		
Note			

Identification	Bit Width	Expression	Default
PAGCC_RETC	3	Binary	0x4
Description			

This register is to specify the release time constant for the peak AGC. Usually, use at the default value.	
Value	Operation or Status
0 to 7	0 for the maximum time constant and 7 for the minimum
Note	

Identification	Bit Width	Expression	Default
PAGCC_REOFS	4	2's complement	0x8
Description			
This register is to specify the release level offset for the peak AGC. Usually, use the default value.			
Value	Operation or Status		
-8 to +7	The release level is given by the following equation: Release Level = PAGCC_PAGM - 16 + (PAGCC_REOFS*2)		
Note			

YGFXA_

0x2D

Name							R/W	
Y Ch. Fixed Gain for Analog Amp.							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x2D	rsv	rsv	rsv	rsv	rsv	FXGA 2	FXGA 1	FXGA 0

Identification	Bit Width	Expression	Default
YGFXA_FXGA	3	Binary	0x1
Description			
This register is to set the value of the fixed gain for the Y-channel programmable gain amplifier in the analog front end (VAFE.)			
Value	Operation or Status		
0 to 7	Gain = 20log((YGFXA_FXGA + 1) * 0.8) [dB]		
Note			
This register is effective only when AGCDEF_MOD='0' or '1'.			

LGFXD_

0x2E – 0x2F

Name							R/W	
Luminance Fixed Gain for Digital AGC							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x2E	FXGD 0	rsv	rsv	rsv	rsv	rsv	rsv	rsv
0x2F	FXGD 8	FXGD 7	FXGD 6	FXGD 5	FXGD 4	FXGD 3	FXGD 2	FXGD 1

Identification	Bit Width	Expression	Default
LGFXD_FXGD	9	Binary	0x100
Description			
This register sets the digital gain value of the AGC circuit.			

Value	Operation or Status
0 to 511	Gain = 20log(LGFXD_FXGD/128) [dB]
Note	
This register is effective only when the register AGCDEF_MOD='0'.	

ACCDEF_

0x30 – 0x32

Name							R/W	
Automatic Chrominance Gain Control Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x30	rsv	rsv	LMT	FRZ	rsv	rsv	MOD 1	MOD 0
0x31	ACMK 5	ACMK 4	ACMK 3	ACMK 2	ACMK 1	ACMK 0	rsv	rsv
0x32	rsv	rsv	rsv	rsv	rsv	AGTC 2	AGTC 1	AGTC 0

Identification	Bit Width	Expression	Default
ACCDEF_MOD	2	Binary	0x3
Description			
This register sets the ACC operation mode.			
Value	Operation or Status		
0	Fixed gain (gain can be set using a register)		
1	Digital ACC operation (Analog gain is fixed: gain can be set using a register)		
2	Reserved		
3	ACC operation for both analog and digital.		
Note			
The digital ACC operation includes the U/V gain control when component signal is input. However, since the U/V gain control depends on the AGC control of the luminance side, the AGC operation mode must be in the digital AGC operation as well. Please refer to "Figure 5.1 ".			

Identification	Bit Width	Expression	Default
ACCDEF_FRZ	1	Binary	0x0
Description			
This is the register to freeze the ACC operation.			
Value	Operation or Status		
0	ACC is active.		
1	ACC is freeze.		
Note			
This register is ineffective when the ACC operation is in the fixed-gain mode (register ACCDEF_MOD=0.)			

Identification	Bit Width	Expression	Default
ACCDEF_LMT	1	Binary	0x1
Description			
This is the register to apply a limiter for ACC operation.			
Value	Operation or Status		
0	Limiter OFF		
1	Limiter ON		
Note			
This register is ineffective when the ACC operation is in the fixed-gain mode (register ACCDEF_MOD=0.)			

Identification	Bit Width	Expression	Default
ACCDEF_ACMK	6	2's complement	0x00
Description			
This is the register to set the ACC reference level. Usually, use the default value.			
Value	Operation or Status		
-32 to +31	The reference level goes down if the value turns to minus, goes up if it turns to plus, based on zero (0) as its center.		
Note			
This register is ineffective when the ACC operation is in the fixed-gain mode (register ACCDEF_MOD=0.)			

Identification	Bit Width	Expression	Default
ACCDEF_ACTC	3	Binary	0x4
Description			
This is the register to set the ACC time constant. Usually, use the default value.			
Value	Operation or Status		
0 to 7	The time constant is maximum at zero (0) and minimum at 7.		
Note			
This register is ineffective when the ACC operation is in the fixed-gain mode (register ACCDEF_MOD=0.)			

CGFXA_

0x33

Name							R/W	
C Ch. Fixed Gain for Analog Amp.							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x33	rsv	rsv	rsv	rsv	rsv	FXGA 2	FXGA 1	FXGA 0

Identification	Bit Width	Expression	Default
CGFXA_FXGA	3	Binary	0x1
Description			
This is the register to set the fixed-gain value of the C-channel programmable-gain amp in the analog front end (VAFE.)			
Value	Operation or Status		
0 to 7	Gain = 20log((CGFXA_FXGA + 1) * 0.8) [dB]		
Note			
Effective when the register AGCDEF_MOD='0' or '1'. Please refer to "Figure 5.1 ".			

PGFXA_

0x34

Name							R/W	
P Ch. Fixed Gain for Analog Amp.							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x34	rsv	rsv	rsv	rsv	rsv	FXGA 2	FXGA 1	FXGA 0

Identification	Bit Width	Expression	Default
PGFXA_FXGA	3	Binary	0x1
Description			

This is the register to set the fixed-gain value of the P-channel programmable-gain amp in the analog front end (VAFE.)	
Value	Operation or Status
0 to 7	Gain = 20log((CGFXA_FXGA + 1) * 0.8) [dB]
Note	
Effective when the register AGCDEF_MOD='0' or '1'. Please refer to "Figure 5.1 ".	

CHGFXD_

0x35 – 0x36

Name							R/W	
Chrominance Gain Fixed for Digital ACC							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x35	FXGD 0	rsv	rsv	rsv	rsv	rsv	rsv	rsv
0x36	FXGD 8	FXGD 7	FXGD 6	FXGD 5	FXGD 4	FXGD 3	FXGD 2	FXGD 1

Identification	Bit Width	Expression	Default
CHGFXD_FXGD	9	Binary	0x100
Description			
This is the register to set the value of the chrominance fixed-gain in the digital ACC circuit.			
Value	Operation or Status		
0 to 511	Gain = 20log(CHGFXD_FXGD/64)[dB]		
Note			
Effective when the register ACCDEF_MOD='0'.			

UVGFXD_

0x37 – 0x38

Name							R/W	
U/V Gain Fixed for Digital ACC							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x37	FXGD 0	rsv	rsv	rsv	rsv	rsv	rsv	rsv
0x38	FXGD 8	FXGD 7	FXGD 6	FXGD 5	FXGD 4	FXGD 3	FXGD 2	FXGD 1

Identification	Bit Width	Expression	Default
UVGFXD_FXGD	9	Binary	0x100
Description			
This is the register to set the value of the U/V fixed-gain in digital ACC circuit.			
Value	Operation or Status		
0 to 511	Gain = 20log(UVGFXD_FXGD/512)[dB]		
Note			
Effective only when the register ACCDEF_MOD='0' and component signal is fed			

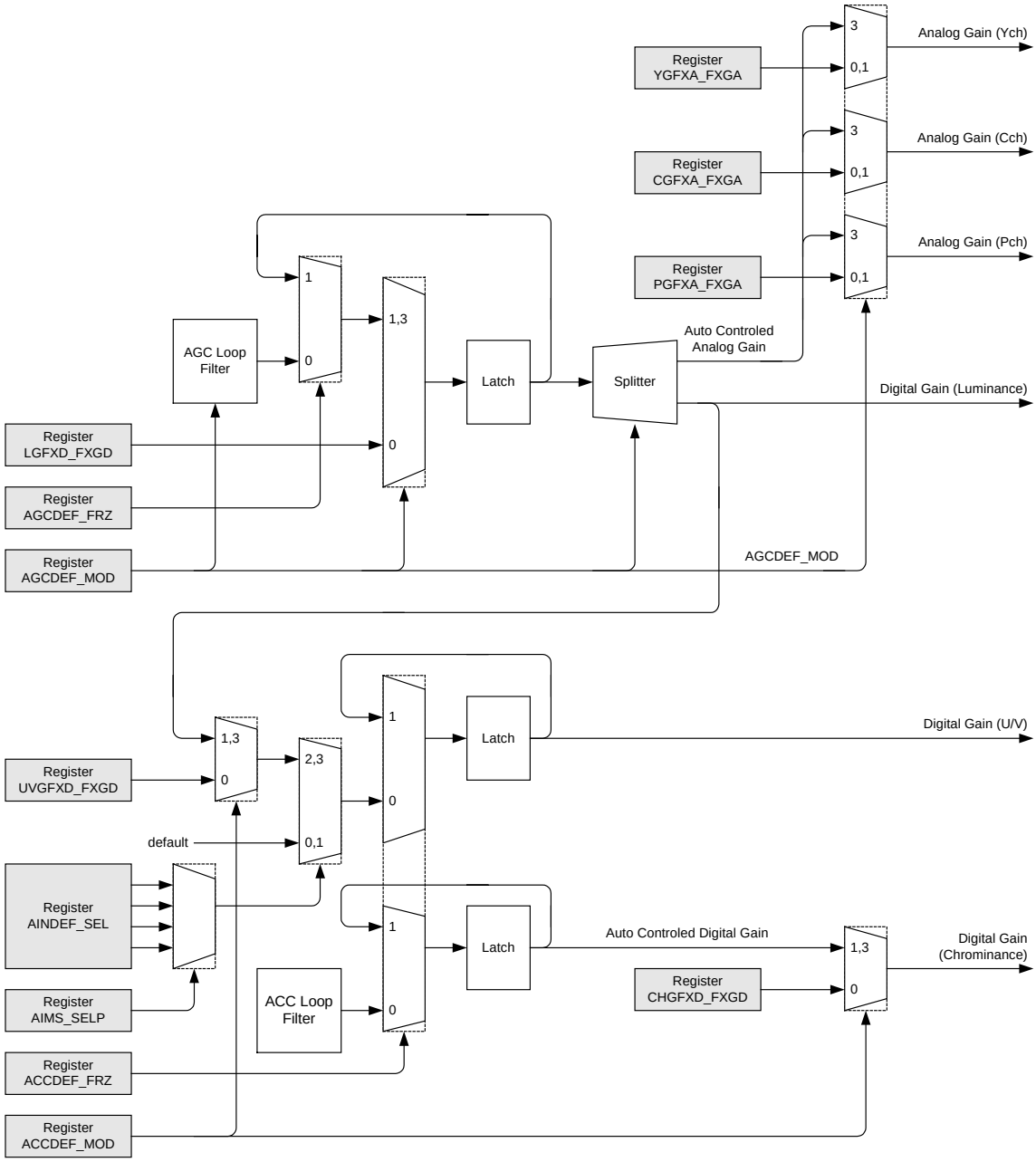


Figure 5.1 Functional diagram for gain control

SBMSK_

0x39

Name							R/W	
SV Port Blanking Mask Settings							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x39	rsv	rsv	rsv	rsv	CMSV	CMSH	YMSV	YMSH

Identification	Bit Width	Expression	Default
SBMSK_YMSH	1	Binary	0x1
Description			
This is the register to mask the luminance data output during the horizontal blanking-interval in the SV Line. The mask values are as follows: 0x10 (on 8bit-output) 0x040(on 10bit-output)			
Value	Operation or Status		
0	Do not mask		
1	Mask		
Note			

Identification	Bit Width	Expression	Default
SBMSK_YMSV	1	Binary	0x1
Description			
This is the register to mask the luminance data output during the vertical blanking-interval in the SV Line. The mask values are as follows: 0x10 (on 8bit-output) 0x040(on 10bit-output)			
Value	Operation or Status		
0	Do not mask		
1	Mask		
Note			

Identification	Bit Width	Expression	Default
SBMSK_CMSH	1	Binary	0x1
Description			
This is the register to mask the chrominance data output during the horizontal blanking-interval in the SV Line. The mask values are as follows: 0x80 (on 8bit-output) 0x200(on 10bit-output)			
Value	Operation or Status		
0	Do not mask		
1	Mask		
Note			

Identification	Bit Width	Expression	Default
SBMSK_CMSV	1	Binary	0x1
Description			
This is the register to mask the chrominance data output during the vertical blanking-interval in the SV Line. The mask values are as follows: 0x80 (on 8bit-output) 0x200(on 10bit-output)			
Value	Operation or Status		

0	Do not mask
1	Mask
Note	

VBISLC_

0x3A

Name							R/W	
VBI Slice Level Control							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x3A	MOD	LEV 6	LEV 5	LEV 4	LEV 3	LEV 2	LEV 1	LEV 0

Identification	Bit Width	Expression	Default
VBISLC_LEV	7	Binary	0x20
Description			
This register sets the slice level at the VBI slice level manual mode.			
Bit	Operation or Status		
0 to 127	Slice Level = VBISLC_LEV * 200/219 IRE (Pedestal Level = 0 IRE)		
Note			

Identification	Bit Width	Expression	Default
VBISLC_LEV	1	Binary	0x0
Description			
This register sets the control mode of the VBI slice level.			
Value	Operation or Status		
0	Automatic mode		
1	Manual mode		
Note			

PJCSW_

0x3B

Name							R/W	
Pixel Jitter Canceller Switch							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x3B	rsv	rsv	rsv	rsv	rsv	AUTO	CPJC	YPJC

Identification	Bit Width	Expression	Default
PJCSW_YPJC	1	Binary	0x1
Description			
This register turns on or off the PJC(Pixel Jitter Canceller) on luminance side.			
Value	Operation or Status		
0	Off		
1	On		
Note			
Ineffective when the register PJCSW_AUTO='1'.			

Identification	Bit Width	Expression	Default
PJCSW_CPJC	1	Binary	0x1
Description			
This is the register to turn on/off the Pixel Jitter Canceller (PJC) on chrominance side.			
Value	Operation or Status		
0	Off		
1	On		
Note			
Ineffective when the register PJCSW_AUTO='1'.			

Identification	Bit Width	Expression	Default
PJCSW_AUTO	1	Binary	0x1
Description			
This register sets either manual or automatic control of the PJC(Pixel Jitter Canceller) on/off control.			
Value	Operation or Status		
0	Manual PJC mode		
1	Automatic PJC mode		
Note			
In the automatic PJC mode, the next conditions will decide either PJC works or not. ·in case phase locked in VCXO operation：PJC off ·In case not pahse locked in VCXO operation：PJC on ·In the free-running mode:　PJC on			

TBCDEF_

0x3C

Name							R/W	
TBC Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x3C	RLS 3	RLS 2	RLS 1	RLS 0	RLE 1	RLE 0	MOD	ENB

Identification	Bit Width	Expression	Default
TBCDEF_ENB	1	Binary	0x1
Description			
Register to specify Line TBC(Time Base Corrector) on/off			
Value	Operation or Status		
0	Off		
1	On		
Note			

Identification	Bit Width	Expression	Default
TBCDEF_MOD	1	Binary	0x1
Description			
Register to set the Line TBC(Time Base Corrector) mode			
Value	Operation or Status		
0	Mode 0		
1	Mode 1		
Note			
For each mode's explanation, please refer to "4.8 TBC" on page 27.			

Identification	Bit Width	Expression	Default
TBCDEF_RLE	2	Binary	0x0
Description			
Register to specify the resetting line (on the ending side of the field) of Line TBC (Time Base Corrector).			
Value	Operation or Status		
0 to 3	From +0 to +3 lines of the standard line		
Note			

Identification	Bit Width	Expression	Default
TBCDEF_RLS	4	2's complement	0x0
Description			
Register to specify the resetting line (at the starting side of the field) of the Line TBC (Time Base Corrector).			
Value	Operation or Status		
-8 to +7	From -8 to +7 lines of the standard line		
Note			

VCXODEF_

0x3D

Name							R/W	
VCXO Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x3D	rsv	rsv	rsv	HCTLE	rsv	rsv	MOD 1	MOD 0

Identification	Bit Width	Expression	Default
VCXODEF_MOD	2	Binary	0x0
Description			
This register to specify the clock mode (free-running/VCXO) and VCXO modes. For details, please refer to "4.1.3 VCXO Control" on page 7.			
Value	Operation or Status		
0	Free-running		
1	Burst-locked VCXO		
2	Line-licked VCXO		
3	Automatic selection VCXO		
Note			

Identification	Bit Width	Expression	Default
VCXODEF_HCTLE	1	Binary	0x1
Description			
This is the register to turn the feature on/off to locate the horizontal sync sampling at an appropriate position automatically in the burst-locked VCXO mode. Usually, use this feature turned on.			
Value	Operation or Status		
0	Off		
1	On		
Note			

BBDEF_

0x3E

Name							R/W	
Blue-back Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x3E	rsv	rsv	rsv	rsv	rsv	MOD 2	MOD 1	MOD 0

Identification	Bit Width	Expression	Default
BBDEF_MOD	2	Binary	0x1

Description

This register selects the blue-back self-running sync mode of the XV750C. As for the blue-back self-running sync, please refer to "4.14.1 Self-running Sync" on page 48. As to the modes described in "Operation or Status" below, please refer to Table 5.3.

Value	Operation or Status
0	Blue-back self-running sync off
1	Blue-back self-running sync mode 0
2	Blue-back self-running sync mode 1
3	Forced Blue-back self-running sync
4 to 6	Not to be used since those are not yet specified
7	Forced self-running sync without blue-back output

Note

Set blue-back self-running sync OFF, the video input goes through at the same sync output with blue-back self-running sync mode ‘0’. With the forced self-running sync (without blue-back output) ON, the video input goes through at the same sync output with forced blue-back self-running sync.

Table 5.3 Blue-back self-running mode

Self-running mode BBDEF_MOD[2:0]		Sync from input video signal undetectable		Sync from input video signal detectable		
		Manual (Note 1)	Other than manual	Manual (Note 1)		Other than manual
		-	-	Different input v frequency than set to MNVM_MOD	Same input v frequency with set to MNVM_MOD	-
Self-running mode 0 (without blue-back)	0,4,5	△1	△2	×	○	○
Self-running mode 0 (with blue-back)	1	▲1	▲2	×	○	○
Self-running mode 1 (with blue-back)	2	▲1	▲2	▲1	○	○
Forced self-running (with blue-back)	3	▲1	▲2	▲1	▲1	▲3
Automatic mode 1 (without blue-back)	6	△1	△2	△1	○	○
Forced self-running (without blue-back)	7	△1	△2	△1	△1	△3

Note1:Manual here means the following settings in the video standard automatic switching registers.0x21: ATVM_FUL=0 and ATVM_VSTD[6:0]=0

Legend	Sync	Video image
△1	Self-running sync output in the scan mode frequency set in 0x22:MNVN_MOD	Video through
△2	Self-running sync output in the scan mode frequency detected proximately (60Hz immediately after resetting)	Video through
△3	Self-running sync output in the scan mode frequency currently detected	Video through
X	Sync output pulling into the scan mode frequency set in 0x22: MNVN_MOD (Note 2)	Video through
○	Sync output locked into the input video signal sync	Video through
▲1	Self-running sync output in the scan mode frequency set in 0x22:MNVN_MOD	blue-back output
▲2	Self-running sync output in the scan mode frequency detected proximately (60Hz immediately after resetting)	blue-back output
▲3	Self-running sync output in the scan mode frequency currently detected	blue-back output

Note2:Sync output in this case, shall be given in imperfect frequency because input sync signal might not be pulled in fully.

VBIDEF_

0x3F

Name							R/W	
VBI Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x3F	rsv	rsv	rsv	rsv	rsv	rsv	SVPTE	DVPTE

Identification	Bit Width	Expression	Default
VBIDEF_DVPTE	1	Binary	0x0
Description			

This is the register to turn the VBI Pass-through data output feature on/off in the DV Line.	
Value	Operation or Status
0	Off
1	On
Note	

Identification	Bit Width	Expression	Default
VBIDEF_SVPTE	1	Binary	0x0
Description			
This is the register to turn the VBI Pass-through data output feature on/off in the SV Line.			
Value	Operation or Status		
0	Off		
1	On		
Note			

VBPLS0_

0x40 – 0x41

Name							R/W	
VBI Path-through Line Selection #0							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x40	FIDSL	VBPSL 6	VBPSL 5	VBPSL 4	VBPSL 3	VBPSL 2	VBPSL 1	VBPSL 0
0x41	FIDEL	VBPEL 6	VBPEL 5	VBPEL 4	VBPEL 3	VBPEL 2	VBPEL 1	VBPEL 0

Identification	Bit Width	Expression	Default
VBPLS0_VBPSL	7	Binary	0x11
Description			
This represents the register #0 that indicates the starting line of VBI Pass-through. It indicates the relative line number in the field designated by the register VBPLS0_FIDSL. Table 5.4 shows the correspondence with the absolute line numbers.			
Value	Operation or Status		
0 to 127	Relative starting-line number		
Note			

Identification	Bit Width	Expression	Default
VBPLS0_FIDSL	1	Binary	0x0
Description			
This register specifies the field ID for the VBI Pass-through starting-line number designated by the register VBPLS0_VBPSL.			
Value	Operation or Status		
0	Field 0 (odd field)		
1	Field 1 (even field)		
Note			

Identification	Bit Width	Expression	Default
VBPLS0_VBPEL	7	Binary	0x11
Description			

This represents the register #0 that indicates the ending line of VBI Pass-through. It indicates the relative line number in the field designated by VBPLS0_ FIDEL. Table 5.4 shows the correspondence with the absolute line numbers.	
Value	Operation or Status
0 to 127	Relative starting-line number
Note	

Identification	Bit Width	Expression	Default
VBPLS0_FIDEL	1	Binary	0x0
Description			
This register specifies the field ID of the VBI Pass-through ending-line number designated by the register VBPLS0_VBPEL.			
Value	Operation or Status		
0	Field 0 (odd field)		
1	Field 1 (even field)		
Note			

VBPLS1_

0x42 – 0x43

Name							R/W	
VBI Path-through Line Selection #1							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x42	FIDSL	VBPSL 6	VBPSL 5	VBPSL 4	VBPSL 3	VBPSL 2	VBPSL 1	VBPSL 0
0x43	FIDEL	VBPEL 6	VBPEL 5	VBPEL 4	VBPEL 3	VBPEL 2	VBPEL 1	VBPEL 0

Identification	Bit Width	Expression	Default
VBPLS1_VBPSL	7	Binary	0x11
Description			
This represents the register #1 that specifies the starting line of VBI Pass-through. It indicates the relative line number in the field designated by the register VBPLS0_FIDSL. Table 5.4 shows the correspondence with the absolute line numbers.			
Value	Operation or Status		
0 to 127	Relative starting-line number		
Note			

Identification	Bit Width	Expression	Default
VBPLS1_FIDSL	1	Binary	0x1
Description			
This register specifies the field ID of the VBI Pass-through starting-line number designated by the register VBPLS1_VBPSL.			
Value	Operation or Status		
0	Field 0 (odd field)		
1	Field 1 (even field)		
Note			

Identification	Bit Width	Expression	Default
VBPLS1_VBPEL	7	Binary	0x11

Description	
This represents the register #1 that specifies the ending line of VBI Pass-through. It indicates the relative line number in the field designated by the register VBPLS0_ FIDEL. Table 5.4 shows the correspondence with the absolute line numbers.	
Value	Operation or Status
0 to 127	Relative starting-line number
Note	

Identification	Bit Width	Expression	Default
VBPLS1_FIDEL	1	Binary	0x1
Description			
This register specifies the field ID of the VBI Pass-through ending-line number designated by the register VBPLS1_VBPEL.			
Value	Operation or Status		
0	Field 0 (even field)		
1	Field 1 (even field)		
Note			

Table 5.4 VBI Pass-through line number correspondence

Register's Name	Register Value	Line Number
VBPLS0_VBPSL (VBPLS0_FIDSL="0")	0x00	4 Line (NTSC) / 1 Line (PAL)
	0x01	5 Line (NTSC) / 2 Line (PAL)
	0x02	6 Line (NTSC) / 3 Line (PAL)
VBPLS0_VBPEL (VBPLS0_FIDEL="0")	⋮	⋮
	0x10	20 Line (NTSC) / 17 Line (PAL)
VBPLS1_VBPSL (VBPLS1_FIDSL="0")	0x11	21 Line (NTSC) / 18 Line (PAL)
	0x12	22 Line (NTSC) / 19 Line (PAL)
VBPLS1_VBPEL (VBPLS1_FIDEL="0")	⋮	⋮
	0x3E	66 Line (NTSC) / 63 Line (PAL)
	0x3F	67 Line (NTSC) / 64 Line (PAL)
VBPLS0_VBPSL (VBPLS0_FIDSL="1")	0x00	267 Line (NTSC) / 314 Line (PAL)
	0x01	268 Line (NTSC) / 315 Line (PAL)
	0x02	269 Line (NTSC) / 316 Line (PAL)
VBPLS0_VBPEL (VBPLS0_FIDEL="1")	⋮	⋮
	0x10	283 Line (NTSC) / 330 Line (PAL)
VBPLS1_VBPSL (VBPLS1_FIDSL="1")	0x11	284 Line (NTSC) /331Line (PAL)
	0x12	285 Line (NTSC) / 332 Line (PAL)
VBPLS1_VBPEL (VBPLS1_FIDEL="1")	⋮	⋮
	0x3E	329 Line (NTSC) / 376 Line (PAL)
	0x3F	330 Line (NTSC) / 377Line (PAL)

VBELS_

0x44 – 0x49

Name							R/W	
VBI Extractor Line Settings							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x44	CCELO 3	CCELO 2	CCELO 1	CCELO 0	CCSLO 3	CCSLO 2	CCSLO 1	CCSLO 0
0x45	CCELE 3	CCELE 2	CCELE 1	CCELE 0	CCSLE 3	CCSLE 2	CCSLE 1	CCSLE 0
0x46	CGELO 3	CGELO 2	CGELO 1	CGELO 0	CGSLO 3	CGSLO 2	CGSLO 1	CGSLO 0
0x47	CGELE 3	CGELE 2	CGELE 1	CGELE 0	CGSLE 3	CGSLE 2	CGSLE 1	CGSLE 0
0x48	WSELO 3	WSELO 2	WSELO 1	WSELO 0	WSSLO 3	WSSLO 2	WSSLO 1	WSSLO 0
0x49	WSELE 3	WSELE 2	WSELE 1	WSELE 0	WSSLE 3	WSSLE 2	WSSLE 1	WSSLE 0

Identification	Bit Width	Expression	Default
VBELS_CCSLO	4	Binary	0xB
Description			
This register specifies the relative starting-line number for extracting the closed caption data in the VBI data extraction (odd field.) Table 5.5 shows the correspondence between the relative and absolute line numbers.			
Value	Operation or Status		
0 to 15	Relative starting-line number		
Note			

Identification	Bit Width	Expression	Default
VBELS_CCELO	4	Binary	0xB
Description			
This register specifies the relative ending-line number for extracting the closed caption data in the VBI data extraction (odd field.) Table 5.5 shows the correspondence between the relative and absolute line numbers.			
Value	Operation or Status		
0 to 15	Relative ending-line number		
Note			

Identification	Bit Width	Expression	Default
VBELS_CCSLE	4	Binary	0xB
Description			
This register specifies the relative starting-line number for extracting the closed caption data in the VBI data extraction (even field.) Table 5.5 shows the correspondence between the relative and absolute line numbers.			
Value	Operation or Status		
0 to 15	Relative starting-line number		
Note			

Identification	Bit Width	Expression	Default

VBELS_CCELE	4	Binary	0xB
Description			
This register specifies the relative ending-line number for extracting the closed caption data in the VBI data extraction (even field.) Table 5.5 shows the correspondence between the relative and absolute line numbers.			
Value	Operation or Status		
0 to 15	Relative ending-line number		
Note			

Identification	Bit Width	Expression	Default
VBELS_CGSLO	4	Binary	0xA
Description			
This register specifies the relative starting-line number for extracting CGMS in the VBI data extraction (odd field.) Table 5.5 shows the correspondence between the relative and absolute line numbers.			
Value	Operation or Status		
0 to 15	Relative starting-line number		
Note			

Identification	Bit Width	Expression	Default
VBELS_CGELO	4	Binary	0xA
Description			
This register specifies the relative ending-line number for extracting CGMS in the VBI data extraction (odd field.) Table 5.5 shows the correspondence between the relative and absolute line numbers.			
Value	Operation or Status		
0 to 15	Relative ending-line number		
Note			

Identification	Bit Width	Expression	Default
VBELS_CGSLE	4	Binary	0xA
Description			
This register specifies the relative starting-line number for extracting CGMS in the VBI data extraction (even field.) Table 5.5 shows the correspondence between the relative and absolute line numbers.			
Value	Operation or Status		
0 to 15	Relative starting-line number		
Note			

Identification	Bit Width	Expression	Default
VBELS_CGELE	4	Binary	0xA
Description			
This register specifies the relative ending-line number for extracting CGMS in the VBI data extraction (even field.) Table 5.5 shows the correspondence between the relative and absolute line numbers.			
Value	Operation or Status		
0 to 15	Relative ending-line number		
Note			

Identification	Bit Width	Expression	Default
VBELS_WSSLO	4	Binary	0xC

Description	
This register specifies the relative starting-line number for extracting WSS in the VBI data extraction (odd field.) Table 5.5 shows the correspondence between the relative and absolute line numbers.	
Value	Operation or Status
0 to 15	Relative starting-line number
Note	

Identification	Bit Width	Expression	Default
VBELS_WSELO	4	Binary	0xC
Description			
This register specifies the relative ending-line number for extracting WSS in the VBI data extraction (odd field.) Table 5.5 shows the correspondence between the relative and absolute line numbers.			
Value	Operation or Status		
0 to 15	Relative ending-line number		
Note			

Identification	Bit Width	Expression	Default
VBELS_WSSLE	4	Binary	0xC
Description			
This register specifies the relative starting-line number for extracting WSS in the VBI data extraction (even field.) Table 5.5 shows the correspondence between the relative and absolute line numbers.			
Value	Operation or Status		
0 to 15	Relative starting-line number		
Note			

Identification	Bit Width	Expression	Default
VBELS_WSELE	4	Binary	0xC
Description			
This register specifies the relative ending-line number for extracting WSS in the VBI data extraction (even field.) Table 5.5 shows the correspondence between the relative and absolute line numbers.			
Value	Operation or Status		
0 to 15	Relative ending-line number		
Note			

Table 5.5 VBI data extraction line number correspondence

Register's Name	Register Value	Line Number
VBELS_CCSLO VBELS_CGSLO VBELS_WSSLO VBELS_CCELO VBELS_CGELO VBELS_WSELO (Odd Field)	0x0	10 Line (NTSC) / 11 Line (PAL)
	0x1	11 Line (NTSC) / 12 Line (PAL)
	0x2	12 Line (NTSC) / 13 Line (PAL)
	0x3	13 Line (NTSC) / 14 Line (PAL)
	0x4	14 Line (NTSC) / 15 Line (PAL)
	0x5	15 Line (NTSC) / 16 Line (PAL)
	0x6	16 Line (NTSC) / 17 Line (PAL)
	0x7	17 Line (NTSC) / 18 Line (PAL)
	0x8	18 Line (NTSC) / 19 Line (PAL)
	0x9	19 Line (NTSC) / 20 Line (PAL)
	0xA	20 Line (NTSC) / 21 Line (PAL)
	0xB	21 Line (NTSC) / 22 Line (PAL)
	0xC	22 Line (NTSC) / 23 Line (PAL)
	0xD	23 Line (NTSC) / 24 Line (PAL)
	0xE	24 Line (NTSC) / 25 Line (PAL)
	0xF	25 Line (NTSC) / 26 Line (PAL)
VBELS_CCSLE VBELS_CGSLE VBELS_WSSLE VBELS_CCELE VBELS_CGELE VBELS_WSELE (Even Field)	0x0	273 Line (NTSC) / 324 Line (PAL)
	0x1	274 Line (NTSC) / 325 Line (PAL)
	0x2	275 Line (NTSC) / 326 Line (PAL)
	0x3	276 Line (NTSC) / 327 Line (PAL)
	0x4	277 Line (NTSC) / 328 Line (PAL)
	0x5	278 Line (NTSC) / 329Line (PAL)
	0x6	279 Line (NTSC) / 330 Line (PAL)
	0x7	280 Line (NTSC) / 331Line (PAL)
	0x8	281 Line (NTSC) / 332 Line (PAL)
	0x9	282 Line (NTSC) / 333 Line (PAL)
	0xA	283 Line (NTSC) / 334 Line (PAL)
	0xB	284 Line (NTSC) / 335 Line (PAL)
	0xC	285 Line (NTSC) / 336 Line (PAL)
	0xD	286 Line (NTSC) / 337 Line (PAL)
	0xE	287 Line (NTSC) / 338 Line (PAL)
	0xF	288 Line (NTSC) / 339 Line (PAL)

YCDELAY_

0x4A

Name							R/W	
YC Delay							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x4A	ODLC 2	ODLC 1	ODLC 0	rsv	ODLY 2	ODLY 1	ODLY 0	Rsv

Identification	Bit Width	Expression	Default
YCDELAY_ODLY	3	2's complement	0x0
Description			
This register is to adjust the Y data delay against the sync signal.			
Value	Operation or Status		
-4 to +3	Delay adjustment (in number of pixels)		
Note			

Identification	Bit Width	Expression	Default
YCDELAY_ODLC	3	2's complement	0x0
Description			
This register is to adjust the C data delay against the sync signal.			
Value	Operation or Status		
-4 to +3	Delay adjustment (in number of pixels)		
Note			

HSDELAY_

0x4B

Name							R/W	
HS Delay							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x4B	HST 7	HST 6	HST 5	HST 4	HST 3	HST 2	HST 1	HST 0

Identification	Bit Width	Expression	Default
HSDELAY_HST	8	2's complement	0x00
Description			
This register makes it possible to adjust the output timing for the horizontal sync signal SHS.			
Value	Operation or Status		
-128 to +127	Delay adjustment (in number of pixels)		
Note			

VSDELAY_

0x4C

Name							R/W	
VS Delay							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x4C	VST 7	VST 6	VST 5	VST 4	VST 3	VST 2	VST 1	VST 0

Identification	Bit Width	Expression	Default
VSDELAY_VST	8	2's complement	0x00
Description			
This register makes it possible to adjust the output timing for the vertical sync signal SVS.			
Value	Operation or Status		
-128 to +127	Delay adjustment (in number of pixels)		
Note			

ACTWINS_

0x4D – 0x50

Name							R/W	
Active Video Window Settings							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x4D	WINL 3	WINL 2	WINL 1	WINL 0	rsv	rsv	rsv	rsv
0x4E	WINR 3	WINR 2	WINR 1	WINR 0	rsv	rsv	rsv	rsv
0x4F	WINT 3	WINT 2	WINT 1	WINT 0	rsv	rsv	rsv	rsv
0x50	WINB 3	WINB 2	WINB 1	WINB 0	rsv	rsv	rsv	rsv

Identification	Bit Width	Expression	Default
ACTWINS_WINL	4	2's complement	0x0
Description			
This register makes it possible to adjust the window (left side) that represents an effective pixel interval.			
Value	Operation or Status		
-8 to +7	Adjustment of the effective pixels (in number of 2 pixels)		
Note			
Use the default value whenever an output in ITU-R BT.656 format is desirable.			

Identification	Bit Width	Expression	Default
ACTWINS_WINR	4	2's complement	0x0
Description			
This register makes it possible to adjust the window (right side) that represents an effective pixel interval.			
Value	Operation or Status		
-8 to +7	Adjustment of the effective pixels (in number of 2 pixels)		
Note			
Use the default value whenever an output in ITU-R BT.656 format is desirable.			

Identification	Bit Width	Expression	Default
ACTWINS_WINT	4	2's complement	0x0
Description			
This register makes it possible to adjust the window (upper side) that represents an effective pixel interval.			
Value	Operation or Status		
-8 to +7	Adjustment of the effective pixels (in number of pixels)		
Note			
Use the default value whenever an output in ITU-R BT.656 format is desirable.			

Identification	Bit Width	Expression	Default
ACTWINS_WINB	4	2's complement	0x0
Description			
This register makes it possible to adjust the window (lower side) that represents an effective pixel interval.			
Value	Operation or Status		
-8 to +7	Adjustment of the effective pixels (in number of pixels)		
Note			
Use the default value whenever an output in ITU-R BT.656 format is desirable.			

SCROPDEF_

0x51

Name							R/W	
SV Port Cropping Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x51	rsv	rsv	rsv	rsv	rsv	rsv	MOD 1	MOD 0

Identification	Bit Width	Expression	Default
SCROPDEF_MOD	2	Binary	0x0
Description			
This is the register to set the cropping feature for the SV Line. For the details on each mode, refer to "4.11Cropping" on page 41.			
Value	Operation or Status		
0	Cropping off		
1	Cropping mode		
2	Masking mode		
3	Reserved		
Note			
The cropping mode cannot be used when output is in ITU-R BT.656 format.			

SCROPH_

0x52 – 0x55

Name							R/W	
SV Port Cropping H Settings							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x52	CRPHS 7	CRPHS 6	CRPHS 5	CRPHS 4	CRPHS 3	CRPHS 2	CRPHS 1	CRPHS 0
0x53	rsv	rsv	rsv	rsv	rsv	rsv	rsv	CRPHS 8
0x54	CRPHA 7	CRPHA 6	CRPHA 5	CRPHA 4	CRPHA 3	CRPHA 2	CRPHA 1	CRPHA 0
0x55	rsv	rsv	rsv	rsv	rsv	rsv	rsv	CRPHA 8

Identification	Bit Width	Expression	Default
SCROPH_CRPHS	9	Binary	0x012
Description			
This register specifies the horizontal starting-position of the cropping area for the SV Line.			
Value	Operation or Status		
0 to 511	Horizontal starting-position (in number of bi-pixels): 0 to 1022 pixel		
Note			

Identification	Bit Width	Expression	Default
SCROPH_CRPHA	9	Binary	0x168
Description			
This register specifies the number of effective horizontal pixels in the cropping area for the SV Line.			
Value	Operation or Status		
0 to 511	Number of horizontal effective pixels (in number of bi-pixels): 0 to 1022 pixel		
Note			

SCROPV_

0x56 – 0x59

Name							R/W	
SV Port Cropping V Settings							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x56	CRPVS 7	CRPVS 6	CRPVS 5	CRPVS 4	CRPVS 3	CRPVS 2	CRPVS 1	CRPVS 0
0x57	rsv	rsv	rsv	rsv	rsv	rsv	CRPVS 9	CRPVS 8
0x58	CRPVA 7	CRPVA 6	CRPVA 5	CRPVA 4	CRPVA 3	CRPVA 2	CRPVA 1	CRPVA 0
0x59	rsv	rsv	rsv	rsv	rsv	rsv	CRPVA 9	CRPVA 8

Identification	Bit Width	Expression	Default
SCROPH_CRPVS	10	Binary	0x006
Description			
This register specifies the vertical starting-position of the cropping area for the SV Line.			
Value	Operation or Status		
0 to 1023	Vertical starting-position (in number of lines): 0 to 1023 line		
Note			

Identification	Bit Width	Expression	Default
SCROPH_CRPVA	10	Binary	0x1E6
Description			
This register specifies the number of effective vertical lines in the cropping area for the SV Line.			
Value	Operation or Status		
0 to 1023	Number of vertical effective lines (in number of lines): 0 to 1023 line		
Note			

DCROPH_

0x5A – 0x5D

Name							R/W	
DV Port Cropping H Settings							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x5A	CRPHS 7	CRPHS 6	CRPHS 5	CRPHS 4	CRPHS 3	CRPHS 2	CRPHS 1	CRPHS 0
0x5B	rsv	rsv	rsv	rsv	rsv	rsv	rsv	CRPHS 8
0x5C	CRPHA 7	CRPHA 6	CRPHA 5	CRPHA 4	CRPHA 3	CRPHA 2	CRPHA 1	CRPHA 0
0x5D	rsv	rsv	rsv	rsv	rsv	rsv	CRPHA 9	CRPHA 8

Identification	Bit Width	Expression	Default

DCROPH_CRPHS	9	Binary	0x012
Description			
This register specifies the horizontal starting-position of the cropping area for the DV Line.			
Value	Operation or Status		
0 to 511	Horizontal starting-position (in number of bi-pixels): 0 to 1022pixel		
Note			
There is certain restriction for setting this register. Refer to "4.10.4 Adjusting the Re-sampling Start Position" on page 38, for details.			

Identification	Bit Width	Expression	Default
DCROPH_CRPHA	10	Binary	0x168
Description			
This register specifies the number of effective horizontal pixels in the cropping area for the DV Line.			
Value	Operation or Status		
0 to 1023	Number of horizontal effective pixels (in number of bi-pixels): 0 to 2046 pixel		
Note			
There is certain restriction for setting this register. Refer to "4.10.5 Setting the Number of Output Pixels" on page 39, for details.			

DCROPV_

0x5E – 0x61

Name							R/W	
DV Port Cropping V Settings							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x5E	CRPVS7	CRPVS6	CRPVS5	CRPVS4	CRPVS3	CRPVS2	CRPVS1	CRPVS0
0x5F	rsv	Rsv	rsv	rsv	rsv	rsv	rsv	CRPVS8
0x60	CRPVA7	CRPVA6	CRPVA5	CRPVA4	CRPVA3	CRPVA2	CRPVA1	CRPVA0
0x61	rsv	Rsv	rsv	rsv	rsv	rsv	CRPVA9	CRPVA8

Identification	Bit Width	Expression	Default
DCROPH_CRPVS	9	Binary	0x00A
Description			
This register specifies the vertical starting-position of the cropping area for the DV Line.			
Value	Operation or Status		
0 to 511	Vertical starting-position (in number of bi-lines): 0 to 1023 line		
Note			
There is certain restriction for setting this register. Refer to "4.10.4 Adjusting the Re-sampling Start Position" on page 38, for details.			

Identification	Bit Width	Expression	Default
DCROPH_CRPVA	10	Binary	0x1E0
Description			

This register specifies the number of effective vertical lines in the cropping area for the DV Line.	
Value	Operation or Status
0 to 1023	Number of vertical effective lines (in number of lines): 0 to 1023 line
Note	
There is certain restriction for setting this register. Refer to "4.10.5 Setting the Number of Output Pixels" on page 39, for details.	

CKILLS_

0x62

Name							R/W	
Color Killer Settings							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x62	CKLE	MOD	Rsv	RLEV 1	RLEV 0	ALEV 2	ALEV 1	ALEV 0

Identification	Bit Width	Expression	Default
CKILLS_ALEV	3	Binary	0x1
Description			
This register is to specify the detection level of the BL color killing. The BL color killing works when the color burst level, theXV750C has detected, is lower than the one set in this register.			
Value	Operation or Status		
0	Approximately 2% of normal color burst level		
1	Approximately 3% of normal color burst level		
2	Approximately 4% of normal color burst level		
3	Approximately 6% of normal color burst level		
4	Approximately 7% of normal color burst level		
5	Approximately 9% of normal color burst level		
6	Approximately 11% of normal color burst level		
7	Approximately 16% of normal color burst level		
Note			
Applicable when input luminance signal level is at the standard level.			

Identification	Bit Width	Expression	Default
CKILLS_RLEV	2	Binary	0x0
Description			
This register is to specify the non-detection level of the BL color killing. The BL color killing turns off when the color burst level, theXV750C has detected, is higher than the one set in this register.			
Value	Operation or Status		
0	CKILLS_ALEV+ Approximately 2%		
1	CKILLS_ALEV+ Approximately 3%		
2	CKILLS_ALEV+ Approximately 4%		
3	CKILLS_ALEV+ Approximately 7%		
Note			

Identification	Bit Width	Expression	Default
CKILLS_MOD	1	Binary	0x0
Description			
This register is to choose the BL color killing modes.			
Value	Operation or Status		

0	Bypass YC separation
1	Output chrominance off
Note	

Identification	Bit Width	Expression	Default
CKILLS_CKLE	1	Binary	0x1
Description			
This register is to turn the BL color killing on and off.			
Value	Operation or Status		
0	Off		
1	On		
Note			

FHCTLS_

0x63 – 0x65

Name							R/W	
FH Control Setting							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x63	CODE 5	CODE 4	CODE 3	CODE 2	CODE 1	CODE 0	TBCE	rsv
0x64	rsv	rsv	Rsv	rsv	rsv	rsv	rsv	rsv
0x65	TBCT 6	TBCT 5	TBCT 4	TBCT 3	TBCT 2	TBCT 1	TBCT 0	rsv

Identification	Bit Width	Expression	Default
FHCTLS_TBCE	1	Binary	0x0
Description			
Register to switch on/off Fh automatic control feature in the line TBC circuit			
Value	Operation or Status		
0	Off		
1	On		
Note			
For Fh control function, please refer to "4.8.3 Fh Control" on page 31.			

Identification	Bit Width	Expression	Default
FHCTLS_CODE	6	Binary	0x0
Description			
Register to set synchronizing characteristics for various non standard signals			
Value	Operation or Status		
0	Standard setting		
1 - 63	Not yet defined		
Note			

Identification	Bit Width	Expression	Default
FHCTLS_TBCT	7	2's complement	0x00
Description			
Register to adjust Fh manually in the line TBC circuit.			
Value	Operation or Status		
-64 to +63	Number of pixels in 1H＝standard value＋FHCTLS_TBCT		

Note
Only effective when the register FHCTLS_TBCE is off = ‘0’.

HSYNC_

0x66

Name							R/W	
Hsync Setting							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x66	rsv	rsv	rsv	rsv	rsv	rsv	rsv	TC

Identification	Bit Width	Expression	Default
HSYNC_TC	1	Binary	0x00
Description			
This register sets the synchronizing characteristics of the XV750C for input signal’s horizontal sync.			
Value	Operation or Status		
0	Normal		
1	High speed		
Note			

VSSFT_

0x67

Name							R/W	
Vsync Shift Setting							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x67	rsv	rsv	rsv	SFTL 4	SFTL 3	SFTL 2	SFTL 1	SFTL 0

Identification	Bit Width	Expression	Default
VSSFT_SFTL	5	Binary	0x00
Description			
This register is used to shift the timing to output Vsync (SVS) by the line.			
Value	Operation or Status		
0 to 31	Output line＝standard line＋VSSFT_SFTL		
Note			

5.2.4. Scaler Settings

For the details of the register settings, please refer to”4.10 Scaling Engine” on page 35.

SCALM_

0x70

Name							R/W	
Scaler Mode							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x70	rsv	rsv	rsv	rsv	rsv	INTO	INTI	VFLTS

Identification	Bit Width	Expression	Default
SCALM_VFLTS	1	Binary	0x0
Description			
This register chooses a vertical filter.			
Value	Operation or Status		
0	Linear interpolation filter		
1	Low-pass filter		
Note			

Identification	Bit Width	Expression	Default
SCALM_INTI	1	Binary	0x1
Description			
This register specifies the scan that is input to the scaling engine.			
Value	Operation or Status		
0	Non-interlaced scan		
1	Interlaced scan		
Note			
Refer to "4.10 Scaling Engine" on page 35, for details.			

Identification	Bit Width	Expression	Default
SCALM_INTO	1	Binary	0x1
Description			
This register specifies the scan that is output from the scaling engine.			
Value	Operation or Status		
0	Non-interlaced scan		
1	Interlaced scan		
Note			
Refer to "4.10 Scaling Engine" on page 35, for details.			

HPHS_

0x71

Name							R/W	
Horizontal Phase Settings							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x71	rsv	rsv	OFST 5	OFST 4	OFST 3	OFST 2	OFST 1	OFST 0

Identification	Bit Width	Expression	Default
HPHS_OFST	6	Binary	0x00
Description			
This is the register to set the amount of horizontal phase offset.			
Value	Operation or Status		
0 to 63	Horizontal phase offset = HPHS_OFST/32 pixels		
Note			
Refer to "4.10 Scaling Engine" on page 35, for details.			

HFILT_

0x72

Name							R/W	
Horizontal Filter Setting							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x72	rsv	rsv	FILT 5	FILT 4	FILT 3	FILT 2	FILT 1	FILT 0

Identification	Bit Width	Expression	Default
HFILT_FILT	6	Binary	0x20
Description			
This is the register to set the horizontal low-pass filter.			
Value	Operation or Status		
2 to 32	Assignable values		
others	Non assignable values		
Note			
Refer to "4.10 Scaling Engine" on page 35, for details.			

HSCAL_

0x73 – 0x74

Name							R/W	
Horizontal Scale Settings							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x73	SCAL 7	SCAL 6	SCAL 5	SCAL 4	SCAL 3	SCAL 2	SCAL 1	SCAL 0
0x74	SCAL 15	SCAL 14	SCAL 13	SCAL 12	SCAL 11	SCAL 10	SCAL 9	SCAL 8

Identification	Bit Width	Expression	Default
HSCAL_SCAL	16	Binary	0x8000
Description			
This is the register to set the horizontal scaling factor.			
Value	Operation or Status		
0 to 65535	Please refer to "4.10.2 Horizontal Scaling" on page 36.		
Note			
There is certain restriction for setting this register. Refer to "4.10 Scaling Engine" on page 35, for details.			

VPHS_

0x75

Name							R/W	
Vertical Phase Settings							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x75	rsv	rsv	OFST 5	OFST 4	OFST 3	OFST 2	OFST 1	OFST 0

Identification	Bit Width	Expression	Default
VPHS_OFST	6	Binary	0x00
Description			
This is the register to set the amount of vertical phase offset.			
Value	Operation or Status		
0 to 63	Vertical phase offset = VPHS_OFST/32 lines		
Note			
Please refer to "4.10 Scaling Engine" on page 35, for details.			

VFILT_

0x76

Name							R/W	
Vertical Filter Setting							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x76	rsv	rsv	VFILT 5	VFILT 4	VFILT 3	VFILT 2	VFILT 1	VFILT 0

Identification	Bit Width	Expression	Default
VFILT_VFILT	6	Binary	0x20
Description			
This is the register to set the vertical low-pass filter.			
Value	Operation or Status		
8 to 32	Assignable value (SCALM_VFLTS=1)		
4,8,16,32	Assignable value (SCALM_VFLTS=0)		
others	Non assignable value		
Note			
Refer to "4.10 Scaling Engine" on page 35, for details.			

VSCAL_

0x77 – 0x78

Name							R/W	
Vertical Scale Settings							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x77	VSCAL 7	VSCAL 6	VSCAL 5	VSCAL 4	VSCAL 3	VSCAL 2	VSCAL 1	VSCAL 0
0x78	VSCAL 15	VSCAL 14	VSCAL 13	VSCAL 12	VSCAL 11	VSCAL 10	VSCAL 9	VSCAL 8

Identification	Bit Width	Expression	Default
VSCAL_VSCAL	16	Binary	0x4000

Description	
This is the register to set the horizontal scaling factor.	
Value	Operation or Status
0 to 65535	Please refer to "4.10.1 Vertical Scaling" on page 35.
Note	
There are restrictions for setting this register. Refer to "4.10 Scaling Engine" on page 35, for details.	

5.2.5. System Configurations

LPWCS_

0x80 – 0x82

Name							R/W	
Low Power Consumption Control Settings							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x80	rsv	rsv	rsv	rsv	rsv	rsv	AUTO	PINE
0x81	rsv	rsv	rsv	rsv	rsv	rsv	OF PWM	OF SCE
0x82	AFEC 7	AFEC 6	AFEC 5	AFEC 4	AFEC 3	AFEC 2	AFEC 1	AFEC 0

Identification	Bit Width	Expression	Default
LPWCS_PINE	1	Binary	0x1
Description			
This register sets the PWDN pin valid or invalid.			
Value	Operation or Status		
0	PWDN pin is invalid.		
1	PWDN pin is valid.		
Note			

Identification	Bit Width	Expression	Default
LPWCS_AUTO	1	Binary	0x1
Description			
This register sets the auto-power on/off control for the ADCs in VAFE. When the auto-power control is enabled, the unused ADCs are automatically powered down.			
Value	Operation or Status		
0	Auto-power control is off (LPWCS_AFEC[2:0] is effective)		
1	Auto-power control is on (LPWCS_AFEC[2:0] is ineffective)		
Note			

Identification	Bit Width	Expression	Default
LPWCS_OFSCE	1	Binary	0x0
Description			
This register conserves the power consumed by the memory used in the scaling engine. When the DV Line output is not in use, this value may be set to "1".			
Value	Operation or Status		
0	Normal mode		
1	Low-power mode		
Note			
This register should be "0" whenever the DV Line is used.			

Identification	Bit Width	Expression	Default
LPWCS_OFPWM	1	Binary	0x0
Description			
This register is used to disable the PWM output for the external VCXO. This register may be "1" when the VCXO pin is not in use.			
Value	Operation or Status		
0	Normal mode		
1	Low-power mode		
Note			

This register should be "0" whenever the VCXO pin is in use.

Identification	Bit Width	Expression	Default
LPWCS_AFEC	8	Binary	0x9F
Description			
This is the register to set the power control for VAFE (video analog front end.) Usually, use the default value.			

Bit	Operation or Status
0	On CH#0
1	On CH#1
2	On CH#2
3	On REF
4	On VCM
5	SWIB
6	BYPASS
7	On CLMPY
Note	

AINDEF_

0x83

Name							R/W	
Analog Input Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x83	SEL3 1	SEL3 0	SEL2 1	SEL2 0	SEL1 1	SEL1 0	SEL0 1	SEL0 0

Identification	Bit Width	Expression	Default
AINDEF_SELm	2	Binary	0x0
Description			
This register specifies the video signal applied to the analog input line number "m".			

Value	Operation or Status
0	Composite
1	S-video
2	Component (Video signal vs. sync ratio ＝7:3)
3	Component (Video signal vs. sync ratio ＝10:4)
Note	

ICHX_

0x84

Name							R/W	
Input Channel Cross-Over							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x84	Rsv	rsv	DPCH 1	DPCH 0	DCCH 1	DCCH 0	DYCH 1	DYCH 0

Identification	Bit Width	Expression	Default
ICHX_DYCH	2	Binary	0x0
Description			

This register specifies the analog input channel number connected to the digital Y channel.	
Value	Operation or Status
0	Analog channel #0
1	Analog channel #1 (not in use)
2	Analog channel #2 (not in use)
3	Reserved
Note	
ICHX_DYCH should always be ”0”.	

Identification	Bit Width	Expression	Default
ICHX_DCCH	2	Binary	0x1
Description			
This register specifies the analog input channel number connected to the digital C channel.			
Value	Operation or Status		
0	Analog channel #0 (not in use)		
1	Analog channel #1		
2	Analog channel #2		
3	Reserved		
Note			
Never set zero (0) in ICHX_DCCH.			

Identification	Bit Width	Expression	Default
ICHX_DPCH	2	Binary	0x2
Description			
This register specifies the analog input channel number connected to the digital P channel.			
Value	Operation or Status		
0	Analog channel #0 (not in use)		
1	Analog channel #1		
2	Analog channel #2		
3	Reserved		
Note			
Never set zero (0) in ICHX_DPCH.			

VSMPDEF_

0x85

Name							R/W	
Video Sampling Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x85	rsv	rsv	rsv	rsv	rsv	rsv	SMPC	DCFB

Identification	Bit Width	Expression	Default
VSMPDEF_DCFB	1	Binary	0x0
Description			
This register determines whether the decimation filter is used for down sampling the 27MHz clock to 13.5MHz or bypassed.			
Value	Operation or Status		
0	Decimation filter is used.		
1	Decimation filter is bypassed.		
Note			
Usually, please use at the default value.			

Identification	Bit Width	Expression	Default
VSMPDEF_SMPC	1	Binary	0x0
Description			
This register is used to set the sampling clock frequency.			
Value	Operation or Status		
0	27MHz		
1	13.5MHz		
Note			
Usually, please use at the default value.			

ICMPNDEF_

0x86

Name							R/W	
Input Component Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x86	rsv	rsv	rsv	rsv	rsv	rsv	LEV 1	LEV 0

Identification	Bit Width	Expression	Default
ICMPNDEF_LEV	2	Binary	0x0
Description			
This register defines the signal category in the component input mode.			
Value	Operation or Status		
0	YCbCr		
1	rsv		
2	rsv		
3	rsv		
Note			

VPDEF_

0x88

Name							R/W	
Output Video Port Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x88	SVCOE	DVCOE	SVOE	DVOE	rsv	MOD 2	MOD 1	MOD 0

Identification	Bit Width	Expression	Default
VPDEF_MOD	3	Binary	0x0
Description			
This register specifies the mode of the video output port. For details, refer to "4.13 Video Output " on page 42.			
Value	Operation or Status		
0	SYC, DYC		
1	SYC, DY, DC		
2	SY, SC		
3	DG/DY, DB/DCb, DR/DCr		
4	SG/SY, SB/SCb, SR/SCr		

Note

Identification	Bit Width	Expression	Default
VPDEF_DVOE	1	Binary	0x0
Description			
This register enables or disables the OE(Output Enable) pin for the signal output buffer of the video output port in the DV Line			
Value	Operation or Status		
0	OE pin is enabled (Hi-Z when OE="L", driven when OE="H")		
1	OE pin is disabled (always driven)		
Note			
This register controls the buffers for the pins that give the DV Line output signals rather than the DVO pins. For example, if the register VPDEF_MOD is '3', it also controls the buffers for the SVO pins.			

Identification	Bit Width	Expression	Default
VPDEF_SVOE	1	Binary	0x0
Description			
This register enables or disables the OE(Output Enable) pin for the signal output buffer of the video output port in the SV Line			
Value	Operation or Status		
0	OE pin is enabled (Hi-Z when OE="L", driven when OE="H")		
1	OE pin is disabled (always driven)		
Note			
This register controls the buffers for the pins that give the SV Line output signals rather than the SVO pins. For example, if the register VPDEF_MOD is '4', it also controls the buffers for the DVO pins.			

Identification	Bit Width	Expression	Default
VPDEF_DVCOE	1	Binary	0x0
Description			
This register specifies OE (Output Enable) control of DV line timing output buffer of the video output port.			
Value	Operation or Status		
0	OE pins effective (giving output with OE="L", Hi-Z and OE="H")		
1	OE pins ineffective (always giving output)		
Note			
This register controls terminal buffer to feed DV line timing signal instead of DVO pins. For instance, if the register VPDEF_MOD is '3' it also controls buffers for the SVO pins.			

Identification	Bit Width	Expression	Default
VPDEF_SVCOE	1	Binary	0x0
Description			
This register specifies OE (Output Enable) control of SV line timing output buffer of the video output port.			
Value	Operation or Status		
0	OE pins effective (giving output with OE="L", Hi-Z and OE="H")		
1	OE pins ineffective (always giving output)		
Note			
This register controls terminal buffer to feed SV line timing signal instead of SVO pins. For instance, if the register VPDEF_MOD is '4' it also controls buffers for the DVO pins.			

SVVDEF_

0x89

Name							R/W	
SV Port Video Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x89	S10B	rsv	SOLM	SRGB 1	SRGB 0	rsv	SOLV 1	SOLV 0

Identification	Bit Width	Expression	Default
SVVDEF_SOLV	2	Binary	0x0
Description			
This register specifies the color space for the data output signal of the SV Line.			
Value	Operation or Status		
0	YCbCr		
1	Reserved		
2	RGB		
3	Reserved		
Note			

Identification	Bit Width	Expression	Default
SVVDEF_SRGB	2	Binary	0x0
Description			
This register specifies the RGB mode for the data output signal of the SV Line.			
Value	Operation or Status		
0	0-255		
1	0-255 γ^{-1} correction		
2	16-235		
3	Reserved		
Note			
Only effective when the regiser SVVDEF_SOLV= ‘2’.			

Identification	Bit Width	Expression	Default
SVVDEF_SOLM	1	Binary	0x0
Description			
This register specifies the limiter for the data output signal of the SV Line.			
Value	Operation or Status		
0	Limiter is off		
1	Limiter is on (ITU-R BT.601level)		
Note			
Only effective when the register SVVDEF_SOLV= ‘0’.			

Identification	Bit Width	Expression	Default
SVVDEF_S10B	1	Binary	0x1
Description			
This register specifies the bit width for the data output signal of the SV Line.			
Value	Operation or Status		
0	8-bit		
1	10-bit		
Note			
This register will be disabled (fixed to 8-bit) when the register VPDEF_MOD= ‘3’ or ‘4’.			

DVVDEF_

0x8A

Name							R/W	
DV Port Video Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x8A	OECV	rsv	DOLM	DRGB 1	DRGB 0	rsv	DOLV 1	DOLV 0

Identification	Bit Width	Expression	Default
DVVDEF_DOLV	2	Binary	0x0
Description			
This register specifies the color space for the data output signal of the DV Line.			
Value	Operation or Status		
0	YCbCr		
1	Reserved		
2	RGB		
3	Reserved		
Note			

Identification	Bit Width	Expression	Default
DVVDEF_DRGB	2	Binary	0x0
Description			
This register specifies the RGB mode for the data output signal of the DV Line.			
Value	Operation or Status		
0	0-255		
1	0-255 γ^{-1} correction		
2	16-235		
3	Reserved		
Note			
Only effective when the register DVVDEF_DOLV= ‘2’.			

Identification	Bit Width	Expression	Default
DVVDEF_DOLM	1	Binary	0x0
Description			
This register specifies the limiter for the data output signal of the DV Line.			
Value	Operation or Status		
0	Limiter is off		
1	Limiter is on (ITU-R BT.601 level)		
Note			
Only effective when the regisiter DVVDEF_DOLV= ’0’.			

Identification	Bit Width	Expression	Default
DVVDEF_OECV	1	Binary	0x0
Description			
This register specifies whether the DVAL signal controls the output buffer for the DV Line's data signal.			
Value	Operation or Status		
0	Off (Always output mode)		
1	On (Output mode while the DVAL signal is asserted, otherwise Hi-Z)		
Note			
Only effective while the buffer is driven by the register VPDEF_DVOE. Otherwise, always Hi-Z.			

SVTDEF_

0x8B

Name							R/W	
SV Port Timing Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x8B	rsv	rsv	rsv	rsv	rsv	VBE	HBE	R656

Identification	Bit Width	Expression	Default
SVTDEF_R656	1	Binary	0x1
Description			
This register specifies the super positioning of the EAV and SAV codes defined in ITU-R BT.656 on the data output signal of the SV Line.			
Value	Operation or Status		
0	Off (no superposition)		
1	On (superposition)		
Note			

Identification	Bit Width	Expression	Default
SVTDEF_HBE	1	Binary	0x0
Description			
This register specifies the output mode for the control signal output, SHB (horizontal blanking signal) for the SV Line.			
Value	Operation or Status		
0	Normal mode		
1	Extended mode (The EAV and SAV output intervals are not treated as blanking period.)		
Note			

Identification	Bit Width	Expression	Default
SVTDEF_VBE	1	Binary	0x0
Description			
This register specifies the output mode for the control signal output, SVB (vertical blanking signal) for the SV Line.			
Value	Operation or Status		
0	Normal mode		
1	Extended mode (The VBI Path-through data output line is not treated as a blanking line)		
Note			

DVTDEF_

0x8C

Name							R/W	
DV Port Timing Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x8C	rsv	rsv	rsv	rsv	rsv	rsv	rsv	R656

Identification	Bit Width	Expression	Default
DVTDEF_R656	1	Binary	0x1
Description			
This register specifies the super positioning of the EAV and SAV codes defined in ITU-R BT.656 on the data output signal of the DV Line.			
Value	Operation or Status		
0	Off (no superposition)		
1	On (superposition)		
Note			

SVCDEF_

0x8D

Name							R/W	
SV Port Control Signal Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x8D	rsv	SFLDS 2	SFLDS 1	SFLDS 0	rsv	SCBFS 2	SCBFS 1	SCBFS 0

Identification	Bit Width	Expression	Default
SVCDEF_SCBFS	3	Binary	0x0
Description			
This register specifies the signals driven to the control signal-out pins in the SV Line.			
Value	Operation or Status		
0	Cb flag (Cb flag signal: Cb=”H” / Cr=”L”)		
1	VBI driving interval (VBI driving interval =”H”)		
2	Logical AND of SHB and SVB		
3	Logical AND of SHS and SVS		
4	SVS		
5	Reversing at every V sync		
6	CFR		
7	CFS		
Note			
The polarity can be reversed by the register SVPOL_SCBF.			

Identification	Bit Width	Expression	Default
SVCDEF_SFLDS	3	Binary	0x0
Description			
This register specifies the signal to output to the control signal-out pin SFLD for the SV Line.			
Value	Operation or Status		
0	Field ID (odd field =”L” / even field =”H”)		
1	VBI driving interval(VBI driving interval=”H”)		
2	Logical AND of SHB and SVB		
3	Logical AND of SHS and SVS		
4	SVS		
5	Reversing at every V sync		
6	CFR		
7	CFS		
Note			
The polarity can be reversed by the register SVPOL_SFLD.			

DVCDEF_

0x8E

Name							R/W	
DV Port Control Signal Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x8E	rsv	DGVP	rsv	DGHP	rsv	rsv	DVALG	DCKS

Identification	Bit Width	Expression	Default
DVCDEF_DCKS	1	Binary	0x1
Description			
This register specifies the direction of the control signal pin DCK for the DV Line.			
Value	Operation or Status		
0	DCK out		
1	DCK in		
Note			
The polarity can be reversed by the register DVPOL_DCK.			

Identification	Bit Width	Expression	Default
DVCDEF_DVALG	1	Binary	0x0
Description			
This register specifies the signal to output to the control signal-out pin DVAL for the DV Line.			
Value	Operation or Status		
0	Data out effective interval for the DV Line (Data Effective)(Data out effective interval =”H”)		
1	DCK & Data Effective		
Note			
The polarity can be reversed by the register DVPOL_DVAL.			

Identification	Bit Width	Expression	Default
DVCDEF_DGHP	1	Binary	0x0
Description			
This register specifies the signal to output to the control signal-out pin DGHP (horizontal general-purpose signal) for the DV Line.			
Value	Operation or Status		
0	Horizontal data ending flag (DHEND) (active Hi)		
1	Horizontal blanking (DHB) (Blanking interval = “L”)		
Note			
The polarity can be reversed by the register DVPOL_DGHP.			

Identification	Bit Width	Expression	Default
DVCDEF_DGVP	1	Binary	0x0
Description			
This register specifies the signal to output to the control signal-out pin DGVP (vertical general-purpose signal) for the DV Line.			
Value	Operation or Status		
0	Vertical data ending flag (DVEND) (active Hi)		
1	Vertical blanking (DVB) (Blanking interval = “L”)		
Note			
The polarity can be reversed by the register DVPOL_DGVP.			

DVGDEF_

0x8F – 0x90

Name							R/W	
DV Port General Signal Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x8F	OECV1	DGP12	DGP11	DGP10	OECV0	DGP02	DGP01	DGP00
0x90	OECV3	DGP32	DGP31	DGP30	OECV2	DGP22	DGP21	DGP20

Identification	Bit Width	Expression	Default
DVGDEF_DGP0	3	Binary	0x1
Description			
This register specifies the signal to output to the general-purpose signal pin DGP0 for the DV Line.			
Value	Operation or Status		
0	Horizontal blanking (DHB) (Blanking interval = “L”)		
1	Field ID (DFLD) (odd field =”L” / even field =”H”)		
2	Cb flag (DCBF) (Cb flag signal: Cb=”H” / Cr=”L”)		
3	VBI driving interval (DVBI) (VBI driving interval=”H”)		
4	DV port FIFO is not empty (DVNE) (active Hi)		
5	DV port FIFO is almost empty (DVAE) (active Hi)		
6	DV port FIFO is almost full (DVAF) (active Hi)		
7	DV port FIFO is full (DVFL) (active Hi)		
Note			
The polarity can be reversed by the register DVPOL_DGP0.			

Identification	Bit Width	Expression	Default
DVGDEF_OECV0	1	Binary	0x0
Description			
This register specifies how the DAVL controls the buffer for the general-purpose signal-out pin DGP0 for the DV Line.			
Value	Operation or Status		
0	Off (do not control the buffer ＝ always driven)		
1	On (driven while DVAL is active, otherwise Hi-Z)		
Note			

Identification	Bit Width	Expression	Default
DVGDEF_DGP1	3	Binary	0x2
Description			
This register specifies the signal to output to the general-purpose signal pin DGP1 for the DV Line.			
Value	Operation or Status		
0	Horizontal blanking (DHB)) (Blanking interval = “L”)		
1	Field ID(DFLD) (odd field =”L” / even field =”H”)		
2	Cb flag(DCBF) (Cb flag signal: Cb=”H” / Cr=”L”)		
3	ANC driving interval (DANC) (ANC driving interval =”H”)		
4	DV port FIFO is not empty (DVNE) (active Hi)		
5	DV port FIFO is almost empty (DVAE) (active Hi)		
6	DV port FIFO is almost full (DVAF) (active Hi)		
7	DV port FIFO is full (DVFL) (active Hi)		
Note			
The polarity can be reversed by the register DVPOL_DGP1.			

Identification	Bit Width	Expression	Default
DVGDEF_OECV1	1	Binary	0x0
Description			
This register specifies how DVAL controls the buffer for the general-purpose signal-out pin DGP1 for the DV Line.			
Value	Operation or Status		
0	Off (no buffer control ＝ always driven)		
1	On (driven while DVAL is active, otherwise Hi-Z)		
Note			

Identification	Bit Width	Expression	Default
DVGDEF_DGP2	3	Binary	0x0
Description			
This register specifies the signal to output to the general-purpose signal pin DGP2 (GPIO[8]) for the DV Line.			
Value	Operation or Status		
0	Horizontal blanking (DHB)) (Blanking interval = “L”)		
1	Field ID (DFLD) (odd field =”L” / even field =”H”)		
2	Cb flag (DCBF) (Cb flag signal: Cb=”H” / Cr=”L”)		
3	SAV or EAV output period (DSAVEAV) (SAV EAV output period =”H”)		
4	DV port FIFO is not empty (DVNE) (active Hi)		
5	DV port FIFO is almost empty (DVAE) (active Hi)		
6	DV port FIFO is almost full (DVAF) (active Hi)		
7	DV port FIFO is full (DVFL) (active Hi)		
Note			
To output DGP2 on pin GPIO[8], the register GPMD_GPSOH must be in DGP mode.			

Identification	Bit Width	Expression	Default
DVGDEF_OECV2	1	Binary	0x0
Description			
This register specifies how the DVAL controls the buffer for the general-purpose signal-out pin DGP2 (GPIO[8]) for the DV Line.			
Value	Operation or Status		
0	Off (no buffer control ＝ always driven)		
1	On (driven while DVAL is active, otherwise Hi-Z)		
Note			

Identification	Bit Width	Expression	Default
DVGDEF_DGP3	3	Binary	0x0
Description			
This register specifies the signal to output to the general-purpose signal pin DGP3(GPIO[9]) for the DV Line.			
Value	Operation or Status		
0	Horizontal blanking (DHB)) (Blanking interval = “L”)		
1	Field ID(DFLD) (odd field =”L” / even field =”H”)		
2	Cb flag(DCBF) (Cb flag signal: Cb=”H” / Cr=”L”)		
3	ANC driving interval (DANC) (ANC driving interval =”H”)		
4	DV port FIFO is not empty (DVNE) (active Hi)		
5	DV port FIFO is almost empty (DVAE) (active Hi)		
6	DV port FIFO is almost full (DVAF) (active Hi)		
7	DV port FIFO is full (DVFL) (active Hi)		
Note			
To output DGP3 on pin GPIO[9], the register GPMD_GPSOH must be in DGP mode.			

Identification	Bit Width	Expression	Default
DVGDEF_OECV3	1	Binary	0x0
Description			
This register specifies how DVAL controls the buffer for the general-purpose signal-out pin DGP3 (GPIO[9]) for the DV Line.			
Value	Operation or Status		
0	Off (no buffer control = always driven)		
1	On (driven while DVAL is active, otherwise Hi-Z)		
Note			

SVPOL_

0x91

Name							R/W	
SV Port Polarities							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x91	SCK	rsv	SFLD	SCBF	SVB	SHB	SVS	SHS

Identification	Bit Width	Expression	Default
SVPOL_SHS	1	Binary	0x0
Description			
This register specifies the polarity of the signal driven to the control signal pin SHS for the SV Line.			
Value	Operation or Status		
0	Normal (Horizontal sync signal: active LOW)		
1	Reverse		
Note			

Identification	Bit Width	Expression	Default
SVPOL_SVS	1	Binary	0x0
Description			
This register specifies the polarity of the signal driven to the control signal pin SVS for the SV Line.			
Value	Operation or Status		
0	Normal (Vertical sync signal: active LOW)		
1	Reverse		
Note			

Identification	Bit Width	Expression	Default
SVPOL_SHB	1	Binary	0x0
Description			
This register specifies the polarity of the signal driven to the control signal pin SHB for the SV Line.			
Value	Operation or Status		
0	Normal (Horizontal blanking signal: active LOW)		
1	Reverse		
Note			

Identification	Bit Width	Expression	Default
SVPOL_SVB	1	Binary	0x0

Description	
This register specifies the polarity of the signal driven to the control signal pin SVB for the SV Line.	
Value	Operation or Status
0	Normal (Vertical blanking signal: active LOW)
1	Reverse
Note	

Identification	Bit Width	Expression	Default
SVPOL_SCBF	1	Binary	0x0
Description			
This register specifies the polarity of the signal driven to the control signal pin SCBF for the SV Line.			
Value	Operation or Status		
0	Normal		
1	Reverse		
Note			
Please refer to the description on the register SVCDEF_SCBFS for the normal polarity of the output signal.			

Identification	Bit Width	Expression	Default
SVPOL_SFLD	1	Binary	0x0
Description			
This register specifies the polarity of the signal driven to the control signal pin SFLD for the SV Line.			
Value	Operation or Status		
0	Normal		
1	Reverse		
Note			
Please refer to the description on the register SVCDEF_SFLDS for the normal polarity of the output signal.			

Identification	Bit Width	Expression	Default
SVPOL_SCK	1	Binary	0x0
Description			
This register specifies the polarity of the signal driven to the control signal pin SCK for the SV Line.			
Value	Operation or Status		
0	Normal		
1	Reverse		
Note			

DVPOL_

0x92

Name							R/W	
DV Port Polarities							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x92	DCK	rsv	DTRDY	DVAL	DGP1	DGP0	DGVP	DGHP

Identification	Bit Width	Expression	Default

DVPOL_DGHP	1	Binary	0x0
Description			
This register specifies the polarity of the signal given at the DV control signal pin DGHP.			
Value	Operation or Status		
0	Normal		
1	Reverse		
Note			
As to the normal polarity of the output signal, please refer to the register DVCDEF_DGHP.			

Identification	Bit Width	Expression	Default
DVPOL_DGVP	1	Binary	0x0
Description			
This register specifies the polarity of the signal given at the DV control signal pin DGVP.			
Value	Operation or Status		
0	Normal		
1	Reverse		
Note			
For the normal polarity of the output signal, please refer to the register DVCDEF_DGVP.			

Identification	Bit Width	Expression	Default
DVPOL_DGP0	1	Binary	0x0
Description			
This register specifies the polarity of the signal given at the DV control signal pin DGP0.			
Value	Operation or Status		
0	Normal		
1	Reverse		
Note			
For the normal polarity of the output signal, please refer to the register DVCDEF_DGP0.			

Identification	Bit Width	Expression	Default
DVPOL_DGP1	1	Binary	0x0
Description			
This register specifies the polarity of the signal given at the DV control signal pin DGP1.			
Value	Operation or Status		
0	Normal		
1	Reverse		
Note			
For the normal polarity of the output signal, please refer to the register DVCDEF_DGP1.			

Identification	Bit Width	Expression	Default
DVPOL_DVAL	1	Binary	0x0
Description			
This register specifies the polarity of the signal given at the DV control signal pin DVAL.			
Value	Operation or Status		
0	Normal		
1	Reverse		
Note			
For the normal polarity of the output signal, please refer to the register DVCDEF_DVALG.			

Identification	Bit Width	Expression	Default
DVPOL_DTRDY	1	Binary	0x0
Description			
This register specifies the polarity of the signal given at the DV control signal pin DTRDY.			
Value	Operation or Status		
0	Normal (target ready =”H”)		

1	Reverse
Note	

Identification	Bit Width	Expression	Default
DVPOL_DCK	1	Binary	0x0
Description			
This register specifies the polarity of the signal given at the DV control signal IO pin DCK.			
Value	Operation or Status		
0	Normal		
1	Reverse		
Note			

GPMD_

0x93

Name							R/W	
General Purpose IO Mode							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x93	GPSSH 1	GPSSH 0	GPSSL 2	GPSSL 1	GPSSL 0	GPSOH 1	GPSOH 0	GPSOL

Identification	Bit Width	Expression	Default
GPMD_GPSOL	1	Binary	0x0
Description			
This register specifies the operation mode of GPIO[7:0], the lower 8 bits of the GPIO pins.			
Value	Operation or Status		
0	Register IO mode		
1	Output mode of the internal status register		
Note			

Identification	Bit Width	Expression	Default
GPMD_GPSOH	2	Binary	0x0
Description			
This register specifies the operation mode of GPIO[9:8], the upper 2 bits of the GPIO pins.			
Value	Operation or Status		
0	Register IO mode		
1	Output mode of the internal status register		
2	DGP mode		
3	CFR/CFS mode		
Note			

Identification	Bit Width	Expression	Default
GPMD_GPSSL	3	Binary	0x0
Description			
This register specifies the address of the status register directed to GPIO[7:0], the lower 8 bits of the GPIO pins.			
Value	Operation or Status		
0 to 6	Register address = GPMD_GPSSL + 0x02		
7	Register address = 0xAB		

Note
Effective only when GPMD_GPSOL=1 (internal status register out mode.)

Identification	Bit Width	Expression	Default
GPMD_GPSSH	2	Binary	0x0
Description			
This register specifies the address of the status register directed to GPIO[9:8], the upper 2 bits of the GPIO pins.			
Value	Operation or Status		
0 to 3	Register address = GPMD_GPSSH + 0x02		
others	Reserved		
Note			
Effective only when GPMD_GPSOH=1 (internal status register out mode.) Only the lower 2 bits of the register will be output as the status.			

GPDIR_

0x94 – 0x95

Name							R/W	
General Purpose IO pin Direction Settings							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x94	GPDIR 7	GPDIR 6	GPDIR 5	GPDIR 4	GPDIR 3	GPDIR 2	GPDIR 1	GPDIR 0
0x95	SOUT	SIN	rsv	rsv	rsv	rsv	GPDIR 9	GPDIR 8

Identification	Bit Width	Expression	Default
GPDIR_GPDIR	10	Binary	0x000
Description			
The value of this register determines the input/output direction of the buffer when the GPIO pins are in the register IO mode. The each bit of the register GPDIR_GPDIR[9:0] corresponds to each pin for GPIO[9:0].			
Value	Operation or Status		
0	Input		
1	Output		
Note			

Identification	Bit Width	Expression	Default
GPDIR_SIN	1	Binary	0x0
Description			
This register is used to approximately synchronize the data input between the upper 2 bits and lower 8 bits, when the GPIO pins are in the register IO mode.			
Value	Operation or Status		
0	The input timing for the upper 2-bit is independent from the lower 8-bit.		
1	The input timing for the upper 2-bit is synchronized with the lower 8-bit.		
Note			
Refer to the description on the register GPIOD_.			

Identification	Bit Width	Expression	Default
GPDIR_SOUT	1	Binary	0x0
Description			
This register is used to approximately synchronize the data output between the upper 2 bits and lower 8 bits, when the GPIO pins are in the register IO mode.			

Value	Operation or Status
0	The output timing for the upper 2-bit is independent from the lower 8-bit.
1	The output timing for the upper 2-bit is synchronized with the lower 8-bit.
Note	
Refer to the description on the register GPIOD_.	

FIMSK_

0x96

Name							R/W	
FIFO Interrupt Mask							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x96	VBOV	VBAF	VBAE	VBNE	DVOV	DVAF	DVAE	DVNE

Identification	Bit Width	Expression	Default
FIMSK_DVNE	1	Binary	0x1
Description			
This register masks the "DV port FIFO not empty" interrupt event.			
Value	Operation or Status		
0	Unmasked		
1	Masked		
Note			
Refer to the description on register FIRQ_DVNE for the interrupt events.			

Identification	Bit Width	Expression	Default
FIMSK _DVAE	1	Binary	0x1
Description			
This register masks the "DV port FIFO almost empty" interrupt event.			
Value	Operation or Status		
0	Unmasked		
1	Masked		
Note			
Refer to the description on register FIRQ_DVAE for the interrupt events.			

Identification	Bit Width	Expression	Default
FIMSK _DVAF	1	Binary	0x1
Description			
This register masks the "DV port FIFO almost full" interrupt event.			
Value	Operation or Status		
0	Unmasked		
1	Masked		
Note			
Refer to the description on register FIRQ_DVAF for the interrupt events.			

Identification	Bit Width	Expression	Default
FIMSK _DVOV	1	Binary	0x1
Description			
This register masks the "DV port FIFO Overflow" interrupt event.			
Value	Operation or Status		
0	Unmasked		
1	Masked		

Note
Refer to the description on register FIRQ_DVOV for the interrupt events.

Identification	Bit Width	Expression	Default
FIMSK _VBNE	1	Binary	0x1
Description			
This register masks the "VBI FIFO not empty" interrupt event.			
Value	Operation or Status		
0	Unmasked		
1	Masked		
Note			
Refer to the description on register FIRQ_VBNE for the interrupt events.			

Identification	Bit Width	Expression	Default
FIMSK _VBAE	1	Binary	0x1
Description			
This register masks the "VBI FIFO almost empty" interrupt event.			
Value	Operation or Status		
0	Unmasked		
1	Masked		
Note			
Refer to the description on register FIRQ_VBAE for the interrupt events.			

Identification	Bit Width	Expression	Default
FIMSK _VBAF	1	Binary	0x1
Description			
This register masks the "VBI FIFO almost full" interrupt event.			
Value	Operation or Status		
0	Unmasked		
1	Masked		
Note			
Refer to the description on register FIRQ_VBAF for the interrupt events.			

Identification	Bit Width	Expression	Default
FIMSK _VBOV	1	Binary	0x1
Description			
This register masks the "VBI FIFO Overflow" interrupt event.			
Value	Operation or Status		
0	Unmasked		
1	Masked		
Note			
Refer to the description on register FIRQ_VBOV for the interrupt events.			

MIMSK_

0x97

Name							R/W	
Misc. Interrupt Mask							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x97	DCCD	NINT	INT	NSTD	STD	NSDET	SDET	VMCLM

Identification	Bit Width	Expression	Default
MIMSK_VMCLM	1	Binary	0x1
Description			
This register masks the "Video mode (video system) changed" interrupt event.			
Value	Operation or Status		
0	Unmasked		
1	Masked		
Note			
Refer to the description on register MIRQ_VMCLM for the interrupt events.			

Identification	Bit Width	Expression	Default
MIMSK _SDET	1	Binary	0x1
Description			
This register masks the "Sync detected" interrupt event.			
Value	Operation or Status		
0	Unmasked		
1	Masked		
Note			
Refer to the description on register MIRQ_SDET for the interrupt events.			

Identification	Bit Width	Expression	Default
MIMSK _NSDET	1	Binary	0x1
Description			
This register masks the "Out of sync" interrupt event.			
Value	Operation or Status		
0	Unmasked		
1	Masked		
Note			
Refer to the description on register MIRQ_NSDET for the interrupt events.			

Identification	Bit Width	Expression	Default
MIMSK _STD	1	Binary	0x1
Description			
This register masks the "Standard signal detected" interrupt event.			
Value	Operation or Status		
0	Unmasked		
1	Masked		
Note			
Refer to the description on register MIRQ_STD for the interrupt events.			

Identification	Bit Width	Expression	Default
MIMSK _NSTD	1	Binary	0x1
Description			
This register masks the "Standard signal not detected" interrupt event.			
Value	Operation or Status		
0	Unmasked		
1	Masked		
Note			
Refer to the description on register MIRQ_NSTD for the interrupt events.			

Identification	Bit Width	Expression	Default
MIMSK _INT	1	Binary	0x1
Description			
This register masks the "Non-interlaced scan not detected " interrupt event.			

Value	Operation or Status
0	Unmasked
1	Masked
Note	
Refer to the description on register MIRQ_INT for the interrupt events.	

Identification	Bit Width	Expression	Default
MIMSK _NINT	1	Binary	0x1
Description			
This register masks the "Non-interlaced scan detected " interrupt event.			
Value	Operation or Status		
0	Masking released		
1	Masking applied		
Note			
Please refer to the description on register MIRQ_NINT for the interrupt events.			

Identification	Bit Width	Expression	Default
MIMSK _DCCD	1	Binary	0x1
Description			
This register masks "Copy Control Data Change" interrupt event.			
Value	Operation or Status		
0	Masking released		
1	Masking applied		
Note			
Please refer to the description on register MIRQ_DCCD for the interrupt events.			

DVFLV_

0x98

Name							R/W	
DV Port FIFO Trigger Level							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x98	AFL 3	AFL 2	AFL 1	AFL 0	AEL 3	AEL 2	AEL 1	AEL 0

Identification	Bit Width	Expression	Default
DVFLV_AEL	4	Binary	0x8
Description			
This register set the level of "DV port FIFO almost empty".			
Value	Operation or Status		
1 to 14	Specifies the level where the "DV port FIFO almost empty" flag is set. When the number of FIFO stages filled becomes equal to or less than this setting value, the "DV port FIFO almost empty" flag becomes "1".		
others	Reserved		
Note			

Identification	Bit Width	Expression	Default
DVFLV_AFL	4	Binary	0x8
Description			
This register set the level for "DV port FIFO almost full".			
Value	Operation or Status		

1 to 14	Specifies the level where the "DV port FIFO almost full" flag is set. When the number of empty FIFO stages becomes equal to or less than this setting value, the "DV port FIFO almost full" flag becomes "1".
others	Reserved
Note	

VBFLV_

0x99

Name							R/W	
VBI FIFO Trigger Level							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x99	rsv	AFL 2	AFL 1	AFL 0	rsv	AEL 2	AEL 1	AEL 0

Identification	Bit Width	Expression	Default
VBFLV_AEL	3	Binary	0x2
Description			
This register set the level for "VBI FIFO almost empty"			
Value	Operation or Status		
0 to 7	Specifies the level where the "VBI FIFO almost empty" flag is set. When the number of FIFO stages filled becomes equal to or less than the twice this setting value, the "VBI FIFO almost empty" flag is set.		
Note			

Identification	Bit Width	Expression	Default
VBFLV_AFL	3	Binary	0x2
Description			
This register set the level for "VBI FIFO almost full".			
Value	Operation or Status		
0 to 7	Specifies the level where the "VBI FIFO almost full" flag is set. When the number of empty FIFO stages becomes equal to or less than the twice this setting value, the "VBI FIFO almost full" flag is set.		
Note			

VBFDEF_

0x9A

Name							R/W	
VBI FIFO Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x9A	CGCRC	CCNULL	WSERR	CGERR	CCERR	WWSS	WCGMS	WCC

Identification	Bit Width	Expression	Default
VBFDEF_WCC	1	Binary	0x0
Description			
This register enables or disables writing the closed-caption extracted data into VBI FIFO.			
Value	Operation or Status		

0	Disable writing
1	Enable writing
Note	

Identification	Bit Width	Expression	Default
VBFDEF_WCGMS	1	Binary	0x0
Description			
This register enables or disables writing the CGMS extracted data into VBI FIFO.			
Value	Operation or Status		
0	Disable writing		
1	Enable writing		
Note			

Identification	Bit Width	Expression	Default
VBFDEF_WWSS	1	Binary	0x0
Description			
This register enables or disables writing the WSS extracted data into VBI FIFO.			
Value	Operation or Status		
0	Disable writing		
1	Enable writing		
Note			

Identification	Bit Width	Expression	Default
VBFDEF_CCERR	1	Binary	0x0
Description			
This register enables writing into VBI FIFO even when error was detected in the closed-caption extracted data.			
Value	Operation or Status		
0	Disable writing (Do not write into VBI FIFO when error is detected.)		
1	Enable writing		
Note			
Effective only when the register VBFDEF_WCC =’1’.			

Identification	Bit Width	Expression	Default
VBFDEF_CGERR	1	Binary	0x0
Description			
This register enables writing into VBI FIFO even when error was detected in the CGMS extracted data.			
Value	Operation or Status		
0	Disable writing (Do not write into VBI FIFO when error is detected.)		
1	Enable writing		
Note			
Effective only when the register VBFDEF_WCGMS= ‘1’.			

Identification	Bit Width	Expression	Default
VBFDEF_WSERR	1	Binary	0x0
Description			
This register enables writing into VBI FIFO even when error was detected in the WSS extracted data.			
Value	Operation or Status		
0	Disable writing (Do not write into VBI FIFO when error is detected.)		
1	Enable writing		

Note
Effective only when the register VBFDEF_WWSS= ‘1’.

Identification	Bit Width	Expression	Default
VBFDEF_CCNULL	1	Binary	0x0
Description			
This register enables writing into VBI FIFO even when NULL code (one or more NULL code on a line) was detected in the closed-caption extracted data.			
Value	Operation or Status		
0	Disable writing (Do not write into VBI FIFO when NULL is detected.)		
1	Enable writing		
Note			
Effective only when the register VBFDEF_WCC= ‘1’.			

Identification	Bit Width	Expression	Default
VBFDEF_CGCRC	1	Binary	0x0
Description			
This register allows writing CRC when writing the CGMS extracted data into VBI FIFO.			
Value	Operation or Status		
0	Disable writing		
1	Enable writing		
Note			
Effective only when the register VBFDEF_WCGMS= ‘1’.			

PWMS_

0x9B

Name							R/W	
PWM Settings							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x9B	MOD	rsv	rsv	TC 4	TC 3	TC 2	TC 1	TC 0

Identification	Bit Width	Expression	Default
PWMS_TC	5	Binary	0x0
Description			
This register specifies the time constant for the PWM signal directed to the VCXO pin.			
Value	Operation or Status		
0 to 31	Time constant: 0: Minimum→31: Maximum		
Note			

Identification	Bit Width	Expression	Default
PWMS_MOD	1	Binary	0x1
Description			
This register specifies the limitation to the duty ratio for the PWM signal directed to the VCXO pin.			
Value	Operation or Status		
0	Duty ratio limit =50% (”H” level period does not go over 50%)		
1	Duty ratio limit = None		
Note			

VCXOS_

0x9C – 0x9D

Name							R/W	
VCXO Settings							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x9C	VXOFS 7	VXOFS 6	VXOFS 5	VXOFS 4	VXOFS 3	VXOFS 2	VXOFS 1	VXOFS 0
0x9D	VXPOL	rsv	rsv	rsv	VXTC 3	VXTC 2	VXTC 1	VXTC 0

Identification	Bit Width	Expression	Default
VCXOS_VXOFS	8	2's complement	0x00
Description			
This register specifies the offset for the VCXO control voltage.			
Value	Operation or Status		
-128 to +127	The voltage level goes down if the value turns to minus, goes up if it turns to plus, based on zero (0) as its center.		
Note			

Identification	Bit Width	Expression	Default
VCXOS_VXTC	4	Binary	0xB
Description			
This register specifies the time constant for the VCXO control.			
Value	Operation or Status		
0 to 15	Time constant: 0: Maximum →15: Minimum		
Note			

Identification	Bit Width	Expression	Default
VCXOS_VXPOL	1	Binary	0x1
Description			
This register specifies the transition characteristics of the VCXO control voltage (set by the F-V characteristics for VCXO.)			
Value	Operation or Status		
0	Inverse F-V characteristic		
1	Positive F-V characteristic		
Note			

CFRDEF_

0x9E – 0x9F

Name							R/W	
Color Field Reset Signal Definition							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0x9E	rsv	FLDP 2	FLDP 1	FLDP 0	rsv	rsv	FLDN 1	FLDN 0
0x9F	LINE 4	LINE 3	LINE 2	LINE 1	LINE 0	rsv	rsv	WID

Identification	Bit Width	Expression	Default
CFRDEF_FLDN	2	Binary	0x3
Description			
This register sets the color field number to output the resetting pulse (CFR), in the NTSC video mode.			
Value	Operation or Status		
0 to 3	Color field #1 ~ #4		
Note			

Identification	Bit Width	Expression	Default
CFRDEF_FLDP	3	Binary	0x7
Description			
This register sets the color field number to output the resetting pulse (CFR), in the PAL video mode.			
Value	Operation or Status		
0 to 7	Color field #1 ~ #8		
Note			

Identification	Bit Width	Expression	Default
CFRDEF_WID	1	Binary	0x1
Description			
This register sets the output width of the resetting pulse.			
Value	Operation or Status		
0	1T(CLKX1)		
1	1 line		
Note			

Identification	Bit Width	Expression	Default
CFRDEF_LINE	5	2's complement	0x00
Description			
This register sets the line number to output the resetting pulse. (The top line of the Vsync shall be the 0 line.)			
Value	Operation or Status		
-16 to +15	From –16th line up to +15th line		
Note			

SYNCDEF_

0xA0

Name							R/W	
SYNC. Detection Definitions							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0xA0	rsv	rsv	rsv	rsv	rsv	rsv	SYRT 1	SYRT 0

Identification	Bit Width	Expression	Default
SYNCDEF_SYRT	2	Binary	0x0
Description			
This registrer sets the time to recover input synchronization from self-running sync output, at the time of weak field strength input.			
Value	Operation or Status		

0 to 3	The bigger the value, the quicker the recovery.
Note	
The parameter only works in the case of unstable input signal such as weak field strength, it has almost no effect when switching over to stable signals like TV or signal generator.	

PDLDEF_

0xA1

Name							R/W	
Pedestal Level Detection Definition							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0xA1	rsv	rsv	rsv	ADPT	MOD	TC 2	TC 1	TC 0

Identification	Bit Width	Expression	Default
PDLDEF_TC	3	Binary	0x4
Description			
This register sets the time constant to synchronize to the digial clamp.			
Value	Operation or Status		
0 to 7	The bigger the value, the quicker it synchronizes.		
Note			

Identification	Bit Width	Expression	Default
PDLDEF_MOD	1	Binary	0x1
Description			
This register sets the operation mode of the pedestal clamp.			
Value	Operation or Status		
0	Reserved		
1	Normal setting		
Note			

Identification	Bit Width	Expression	Default
PDLDEF_ADPT	1	Binary	0x1
Description			
This register sets the synchronization to the pedestal clamp input signal.			
Value	Operation or Status		
0	Always synchronizing		
1	Stops synchronizing when the sync detection unstable.		
Note			
This register setting is only valid when the register PDLDEF_MOD = ‘1’.			

TPGENS_

0xA2

Name							R/W	
Test Pattern Generator Setting							Write/Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0xA2	AMPS 2	AMPS 1	AMPS 0	PICS 2	PICS 1	PICS 0	MODE 1	MODE 0

Identification	Bit Width	Expression	Default
TPGENS_MODE	2	Binary	0x0
Description			
Set the category of the test pattern image.			
Value	Operation or Status		
0	Image of the input signal (test pattern OFF)		
1	Color bar image		
2	Ramp image		
3	Raster image		
Note			

Identification	Bit Width	Expression	Default
TPGENS_PICS	3	Binary	0x0
Description			
This register selects the options for each test pattern image.			
Value	Operation or Status		
0 to 7	For the register TPGENS_MODE setting 1/2/3, the image varies. As for the details please refer to the Table 5.6.		
Note			
There are no other definitions other than Table 5.6.			

Identification	Bit Width	Expression	Default
TPGENS_AMPS	2	Binary	0x0
Description			
This register sets options for each test pattern.			
Value	Operation or Status		
0	1.0 time		
1	0.75 times		
2	0.5 times		
3	0.25 times		
4	0 time		
5 - 7	(1.0 time)		
Note			

Table 5.6 Test Patterns

Pattern Mode	Pattern Option	TPGENS_PICS	TPGENS_MODE
Color Bar	100% Color bar	000	01
	75% Color Bar	001	01
Ramp	Ramp	000	10
	Mod Ramp	001	10
Raster	White	000	11
	Yellow	001	11
	Cyan	010	11
	Green	011	11
	Magenta	100	11
	Red	101	11
	Blue	110	11
	Black	111	11

SNRMON_

0xA8 – 0xA9

Name							R/W	
Signal Noise Ratio Monitor							Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0xA8	SLEV 7	SLEV 6	SLEV 5	SLEV 4	SLEV 3	SLEV 2	SLEV 1	SLEV 0
0xA9	NLEV 7	NLEV 6	NLEV 5	NLEV 4	NLEV 3	NLEV 2	NLEV 1	NLEV 0

Identification	Bit Width	Expression	Default
SNRMON_SLEV	8	Binary	-
Description			
This register indicates the signal level.			
Value	Operation or Status		
0 to 0xFF	Signal level		
Note			

Identification	Bit Width	Expression	Default
SNRMON_NLEV	8	Binary	-
Description			
This register indicates the noise level.			
Value	Operation or Status		
0 to 0xFF	Noise level		
Note			

HLJINF_

0xAA

Name							R/W	
H Lock Judgement Information							Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0xAA	LCKE 7	LCKE 6	LCKE 5	LCKE 4	LCKE 3	LCKE 2	LCKE 1	LCKE 0

Identification	Bit Width	Expression	Default
HLJINF_LCKE	8	Binary	-
Description			
This register indicates the deviation (error level) when operating in VCXO-H-Lock mode.			
Value	Operation or Status		
0 to 0xFF	H-Lock error level		
Note			

CFSINF_

0xAB

Name							R/W	
Color Field Sequence Information							Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0xAB	rsv	rsv	rsv	rsv	CONF	CFSQ 2	CFSQ 1	CFSQ 0

Identification	Bit Width	Expression	Default
CFSINF_CFSQ	3	Binary	-
Description			
This register indicates the current color field number.			
Value	Operation or Status		
0 to 0x7	From color field No#1 to #8		
Note			

Identification	Bit Width	Expression	Default
CFSINF_CONF	1	Binary	-
Description			
This register indicates 1 when CFSINF_CFSQ is firm.			
Value	Operation or Status		
0	Not defined yet		
1	Firm		
Note			

VTRDEF_

0xAC

Name							R/W	
VTR Detection							Read	
Address	D7	D6	D5	D4	D3	D2	D1	D0
0xAC	rsv	rsv	rsv	rsv	rsv	WEAK	VTR 1	VTR 0

Identification	Bit Width	Expression	Default
VTRDEF_VTR	2	Binary	-
Description			
This register indicates the current input signal souce classification the XV750C acknowledges, resulting of VTR judgement.			
Value	Operation or Status		
0	Standard signal such as TV signal		
1	Signal under VTR normal replay		
2	Signal under VTR particular replay		
3	Unable to distinguish		
Note			

Identification	Bit Width	Expression	Default
VTRDEF_WEAK	1	Binary	-
Description			
This register indicates the current input signal souce classification the XV750C acknowledges, resulting of weak field strength judgement.			
Value	Operation or Status		

0	Stable signal
1	Weak field signal
Note	

5.3. Default Values for Register Settings

As for the default value (setting values when the XV750C once reset) in the register settings, please refer to the following main configurations.

Video System	Group Automatic (Active for all modes the XV750C supports)
Analog Input (mode 0)	Composite Video
Analog Input (mode 1)	S Video
Analog Input (mode 2)	Component Video (7:3 Video/Sync Ratio)
Analog Input (mode 3)	Component Video (10:4 Video/Sync Ratio)
Analog Input Selection	Analog Input Mode 0
Digital Output (SV mode)	ITU-R BT.656 Output
Digital Output (DV mode)	Addition SAV and EAV
DV mode Read Clock	Internal Supply
Operating Clock	Freeunning
PJC	AUTO
TBC	On
Comb Filter Selection (PAL)	Adaptive 5 line Comb Filter
AGC/ACC	Hybrid
Interrupt Masking	Masking on every Interrupt Event
GPIO	Register IO Mode
VBI Data Extraction	Ineffective
VBI Path Through	Ineffective

6. Sample Circuit

A sample circuit is shown in Figure 6.2.

IIX Inc. recommends inserting a filter as shown in Figure 6.1 in the analog video signal input stage. This is to cope with the interfering distortion opt to be caused between the sampling clock of the XV750C and the input video signal superposed with 27MHz aliasing noise. In case input video signal carries no such problem, this filer is not required.

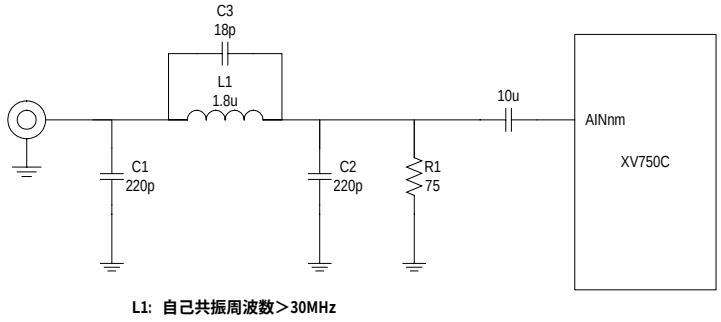


Figure 6.1 Anti Aliasing Filter Sample

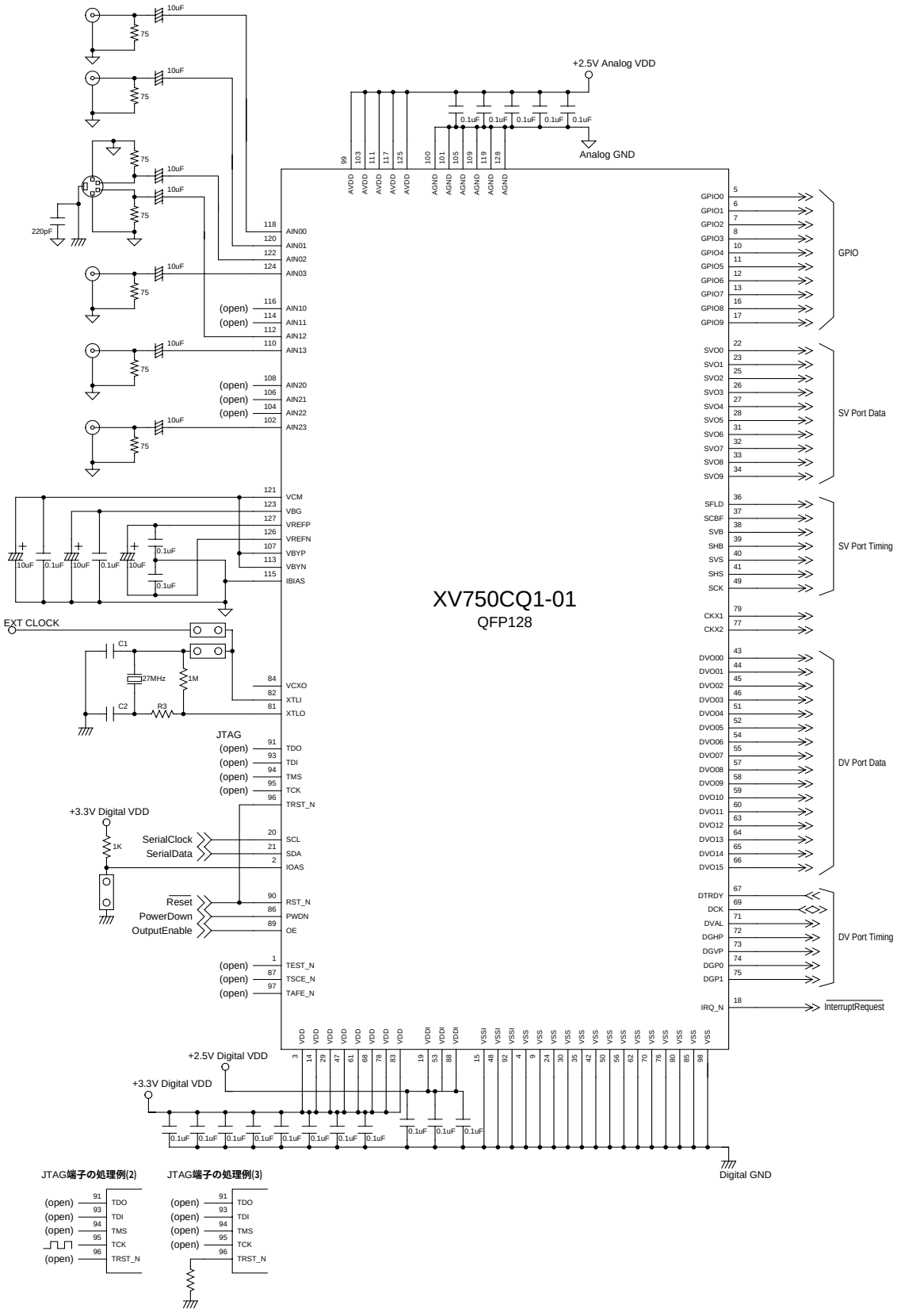


Figure 6.2 Sample circuit

7. Electrical Characteristics

7.1. Absolute Maximum Ratings

Table 7.1 Absolute Maximum Ratings

Item	Symbol	Conditions	Range	Unit
Power Supply	V_{DD33}		-0.5 ~ +4.6	V
	V_{DD25}		-0.5 ~ +3.5	V
Input Volt	V_I		-0.5 ~ +6.0	V
Storage Temp.	Tstg		-65 ~ +150	^oC

7.2. Recommended Operating Conditions

Table 7.2 Recommended Operating Conditions

Item	Symbol	Conditions	MIN.	TYP.	MAX	Unit
Power Supply	V_{DD33}		3.0	3.3	3.6	V
	V_{DD25}		2.25	2.5	2.75	V
	V_{DD25A}		2.25	2.5	2.75	V
Operation Temp.	Topt		0	25	75	^oC
High Level Input Voltage	V_{IH}		2.0		5.5	V
Low Level Input Voltage	V_{IL}		-0.3		0.8	V
Junction Temp.	Tj		0	25	125	^oC

7.3. DC, AC Characteristics

7.3.1. Analog Characteristics

Table 7.3 Analog Characteristics

Item	Symbol	Conditions	MIN.	TYP.	MAX	Unit
Consumption Current	I_{DD25A}	Ych,Cch,Pch ON		100		mA
ADC Effective Number Of Bits	ENOB	fin = 4.45MHz		9.5	-	bit
ADC Differential Non Linearity	DNL	Fin = 4.45MHz		+/-0.8		LSB
ADC Integration Non Linearity	INL	Fin = 4.45MHz		+/-1.5		LSB
ADC Differential Gain	DG			+/-1		%
ADC Differential Phase	DP			+/-1		Deg.
ADC Voltage Reference	V_{REFN}			0.8		V
	V_{REFP}			1.8		V
Analog Input Range	V_{INRG}			2.0		V
AIN0n(n=0,1,2,3) Clamp Voltage	V_{CL0}			0.03		V
AIN1n(n=0,1,2,3) Clamp Voltage	V_{CL1}			1.3		V
AIN2n(n=0,1,2,3) Clamp Voltage	V_{CL2}			1.3		V
Signal Noise Ratio	SNR		50			dB
Channel Cross Talk	CCT	AIN0n – AIN1n AIN1n – AIN2n AIN0n – AIN2n			-50	dB

7.3.2. DC Characteristics (Digital)

Table 7.4 DC Characteristics (Digital)

Item	Symbol	Conditions	MIN.	TYP.	MAX	Unit
High Level Output Voltage	V_{OH}	I_{OH}=8mA	2.4			V
Low Level Output Voltage	V_{OL}	I_{OL}=8mA			0.4	V
High Level Output Current	I_{OH}	V_{OH}=2.4V	9.5			mA
Low Level Output Current	I_{OL}	V_{OL}=0.4V	8.1			mA

7.3.3. AC Characteristics (Digital)

Table 7.5 AC Characteristics (Digital)

PIN	Symbol	Parameter	MIN	TYP	MAX	Unit
RST_N	Trst	Input Pulse Width	37			ns
XTLI	Tclk	Input Clock Frequency			27	MHz
DCK	Tclk	Input Clock Frequency			54	MHz
XTLO	Trise	Clock Rise Delay	1		3	ns
	Tfall	Clock Fall Delay	1		3	ns
CKX2	Trise	Clock Rise Delay	8		16	ns
	Tfall	Clock Fall Delay	7		14	ns
SCK	Trise	Clock Rise Delay	8		18	ns
	Tfall	Clock Fall Delay	7		16	ns
	T13.5rise	Clock Rise Delay	11		24	ns
	T13.5fall	Clock Fall Delay	10		22	ns
DCK	Trise	Clock Rise Delay	7		16	ns
	Tfall	Clock Fall Delay	7		15	ns
CKX1	T13.5rise	Clock Rise Delay	9		19	ns
	T13.5fall	Clock Fall Delay	8		18	ns
VCXO	T13.5aa	Output Delay(13.5MHz)			26	ns
	T13.5dh	Output Delay(13.5MHz)	11			ns
IRQ_N	T13.5aa	Output Delay(13.5MHz)			25	ns
	T13.5dh	Output Delay(13.5MHz)	10			ns
SVB	T27aa	Output Delay(27MHz)			20	ns
	T27dh	Output Delay(27MHz)	8			ns
	T13.5aa	Output Delay(13.5MHz)			20	ns
	T13.5dh	Output Delay(13.5MHz)	8			ns
SHB	T27aa	Output Delay(27MHz)			21	ns
	T27dh	Output Delay(27MHz)	9			ns
	T13.5aa	Output Delay(13.5MHz)			21	ns
	T13.5dh	Output Delay(13.5MHz)	9			ns
SVS	T27aa	Output Delay(27MHz)			20	ns
	T27dh	Output Delay(27MHz)	8			ns
	T13.5aa	Output Delay(13.5MHz)			20	ns

PIN	Symbol	Parameter	MIN	TYP	MAX	Unit
	T13.5dh	Output Delay(13.5MHz)	8			ns
SHS	T27aa	Output Delay(27MHz)			20	ns
	T27dh	Output Delay(27MHz)	8			ns
	T13.5aa	Output Delay(13.5MHz)			21	ns
	T13.5dh	Output Delay(13.5MHz)	9			ns
SFLD	T27aa	Output Delay(27MHz)			20	ns
	T27dh	Output Delay(27MHz)	8			ns
	T13.5aa	Output Delay(13.5MHz)			20	ns
	T13.5dh	Output Delay(13.5MHz)	12			ns
SCBF	T27aa	Output Delay(27MHz)			21	ns
	T27dh	Output Delay(27MHz)	9			ns
	T13.5aa	Output Delay(13.5MHz)			21	ns
	T13.5dh	Output Delay(13.5MHz)	9			ns
SVO	T27aa	Output Delay(27MHz)			20	ns
	T27dh	Output Delay(27MHz)	8			ns
	T13.5aa	Output Delay(13.5MHz)			20	ns
	T13.5dh	Output Delay(13.5MHz)	8			ns
GPIO	T13.5aa	Output Delay(13.5MHz)			26	ns
	T13.5dh	Output Delay(13.5MHz)				ns
DGP0	Twaa	Output Delay(27MHz)			24	ns
	Twdh	Output Delay(27MHz)	9			ns
	Traa	Output Delay(DCK)			12	ns
	Trdh	Output Delay(DCK)	4			ns
DGP1	Twaa	Output Delay(27MHz)			24	ns
	Twdh	Output Delay(27MHz)	9			ns
	Traa	Output Delay(DCK)			12	ns
	Trdh	Output Delay(DCK)	4			ns
DGHP	Twaa	Output Delay(27MHz)			21	ns
	Twdh	Output Delay(27MHz)	9			ns
	Traa	Output Delay(DCK)			12	ns
	Trdh	Output Delay(DCK)	4			ns
DGVP	Twaa	Output Delay(27MHz)			22	ns
	Twdh	Output Delay(27MHz)	9			ns
	Traa	Output Delay(DCK)			13	ns
	Trdh	Output Delay(DCK)	4			ns
DVO	Twaa	Output Delay(27MHz)			21	ns
	Twdh	Output Delay(27MHz)	9			ns
	Traa	Output Delay(DCK)			12	ns
	Trdh	Output Delay(DCK)	4			ns
DTRDY	Tds	Input Setup(27MHz)			0	ns
	Tdh	Input Hold(27MHz)	15			ns
	Tds	Input Setup(DCK)			6	ns
	Tdh	Input Hold(DCK)	1			ns
SDA	Tds	Input Setup			0	ns
	Tdh	Input Hold	20			ns
SCL	Tds	Input Setup			0	ns
	Tdh	Input Hold	20			ns

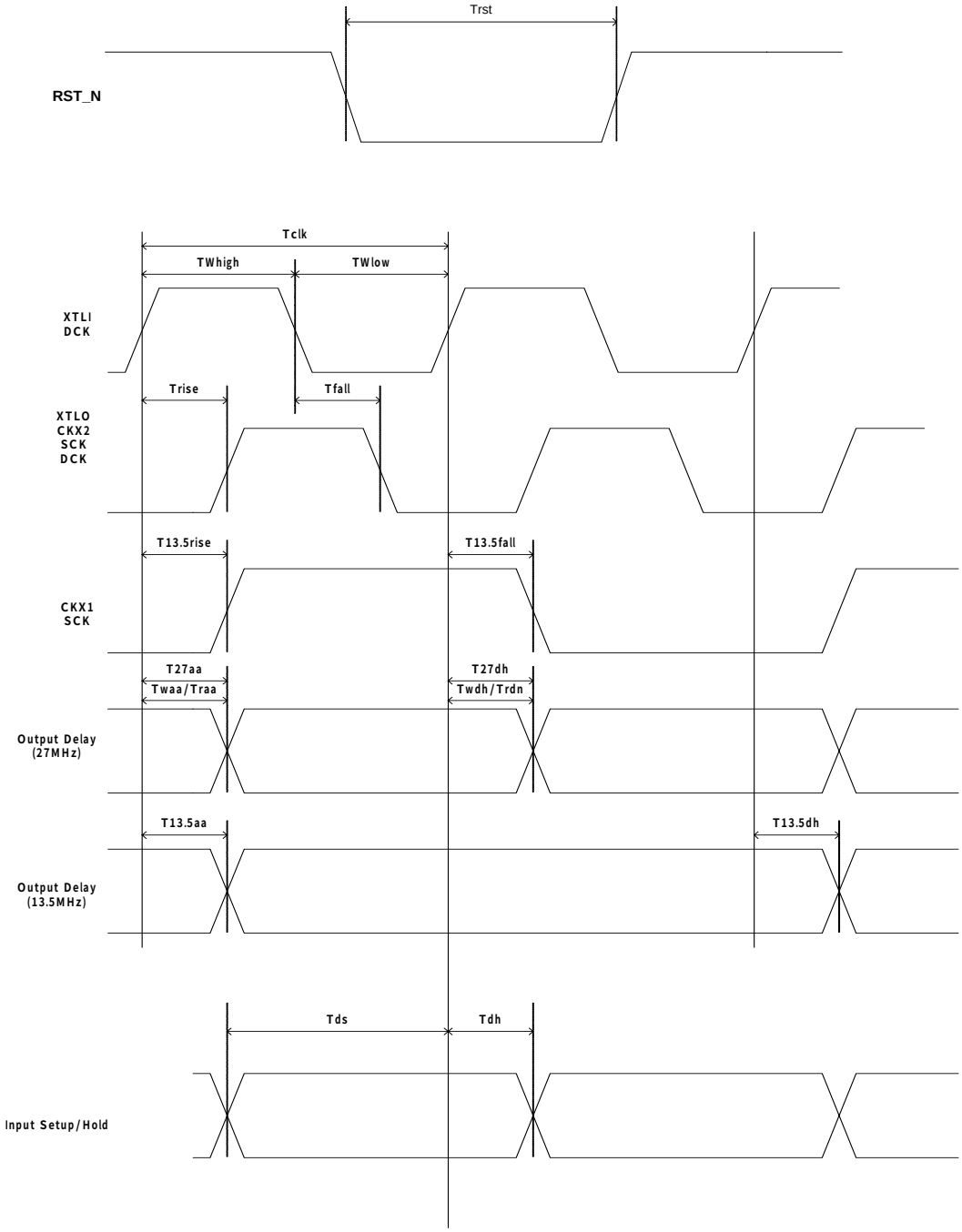
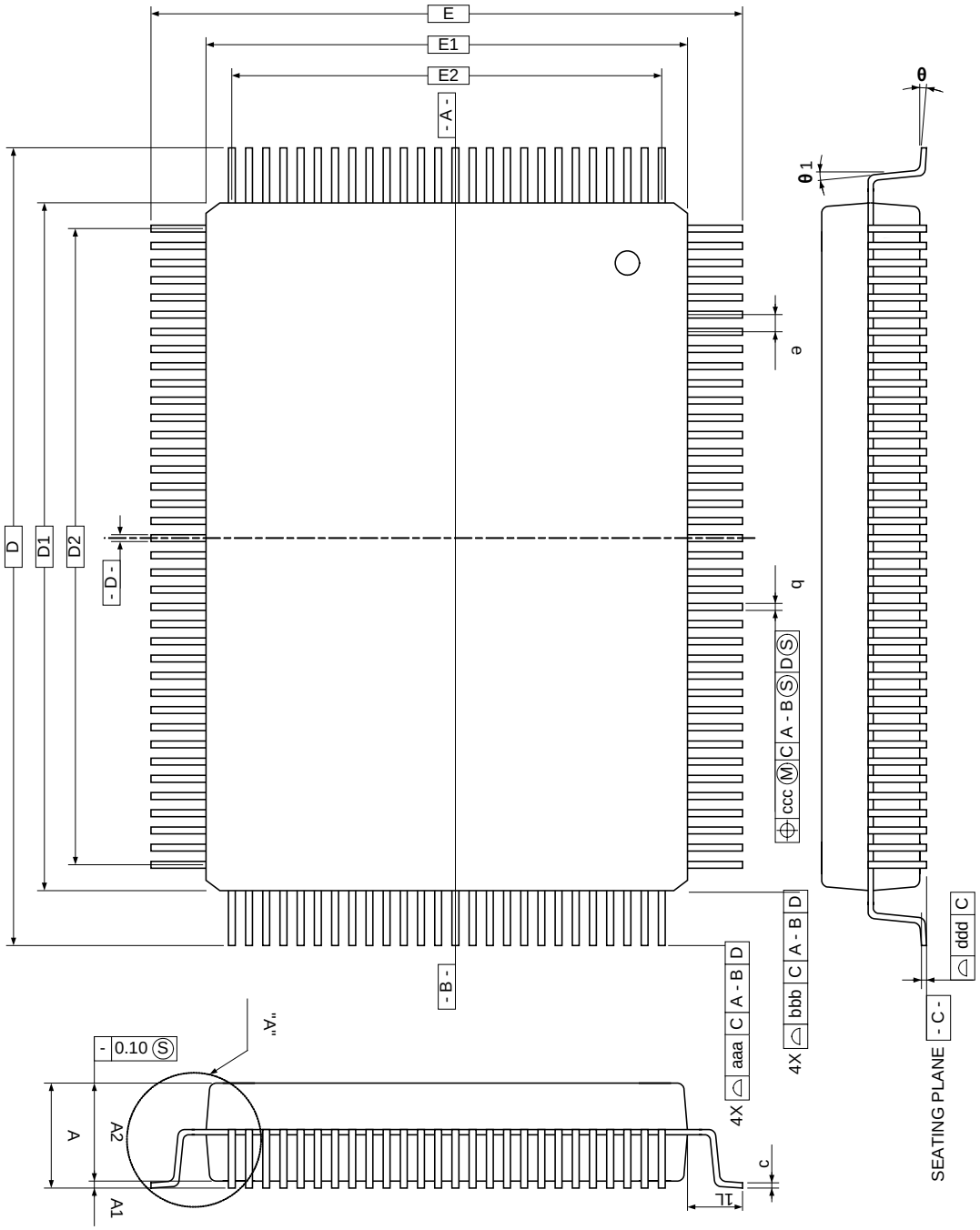
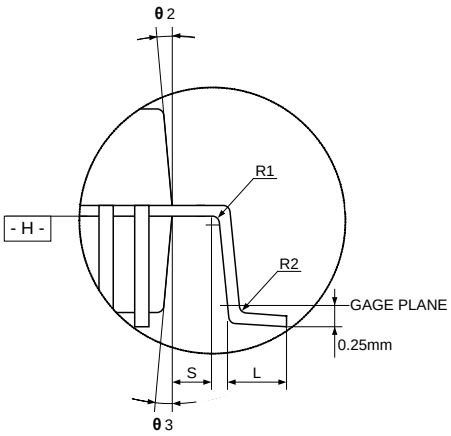


Figure 7.1 AC Characteristics (Digital)

8. Packaging

128pin QFP (XV750CQ1)





DETAIL "A"

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E1	14.00 BASIC			0.551 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0 °	—	7 °	0 °	—	7 °
θ1	0 °	—	—	0 °	—	—
ALLOY 42 L/F θ2, θ3	7 ° REF			7 ° REF		
COPPER L/F θ2, θ3	15 ° REF			15 ° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.170	0.200	0.270	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES:

1. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE - H -

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

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