19-2539; Rev 1; 1/03

MAXIM

Low-Power, Low-Distortion, Central-Office ADSL Drivers and Integrated Drivers/Receivers

General Description

The MAX9480/MAX9481/MAX9482 low-power, low-distortion, class-G, high-current asymmetric digital subscriber line (ADSL) drivers offer Rail-to-Rail® output and are ideal for ADSL in central-office applications. Operating from ±5V and ±2.5V supplies, the drivers incorporate two high-speed current-feedback preamplifiers driving two fixed-gain class-G buffers. The buffers can deliver 20.4dBm average line power with a signal crest factor of 5.3, and are designed to be directly DC or AC bridged across a 1:2.5 transformer.

The MAX9480/MAX9481/MAX9482 employ an active line termination scheme for incoming signals that eliminates the need for back-match resistors, reducing line-card power consumption at full rate to less than half of that required by conventional class-AB line-driver circuits.

The MAX9480 includes a hybrid network and two low-noise, fixed-gain-of-4.6V/V receive amplifiers. The part is designed to recover the receive signal to the same level as that of a conventional line interface circuit that incorporates a 1:2 transformer and standard back-matched hybrid, without degrading signal-to-noise ratio (SNR) or line-impedance sensitivity. The MAX9481 provides only the preamplifiers and buffers without the hybrid or receivers. The MAX9482 provides preamplifiers, buffers, and uncommitted receive amplifiers. All devices have a low-output-impedance shutdown function for saving power when not transmitting.

At full-rate 20.4dBm discrete multitone data transmission (DMT), the total dynamic power dissipation is only 680mW (MAX9480/MAX9482) or 655mW (MAX9481). The MAX9480/MAX9481 are available in a 20-pin TSSOP package and the MAX9482 is available in 28-pin TSSOP and 32-pin QFN packages. All devices operate over the extended -40°C to +85°C temperature range.

Applications

Full-Rate ADSL

HDSL

Central Office

DSLAM

Typical Operating Circuits appear at end of data sheet.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Features

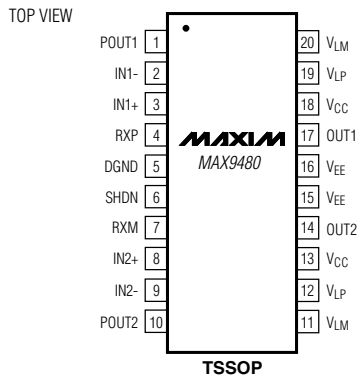
- **Dissipate Only 655mW While Driving 20.4dBm ADSL Full-Rate DMT-Modulated Signal**
- **Operate with ±5.0V and ±2.5V Power Supplies**
- **Complete ADSL Central-Office Line Interface (MAX9480/MAX9482)**
  - **Two Preamplifiers plus Class-G Rail-to-Rail Buffers**
  - **Active Line Termination plus Integrated Hybrid (MAX9480)**
  - **Low-Noise Uncommitted Receive Amplifiers (MAX9482)**
  - **Fixed-Gain Receive Amplifiers (MAX9480)**
  - **Low-Output-Impedance Shutdown Mode**
- **Preamplifiers, Buffers, and Active Line Termination Functions (MAX9481)**
- **High-Output-Drive Capability**
  - **$15V_{P-P}$ Differential Output Voltage Swing at $R_L = 16\Omega$**
  - **500mA Output-Drive**
- **Low Distortion: -71dBc Highest Harmonic at 1MHz and $14V_{P-P}$**
- **High Speed: 250V/µs Slew Rate, 80MHz -3dB Bandwidth (G = -3)**
- **Thermal Shutdown**
- **Exposed Pads Improve Thermal Performance**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9480CUP	-40°C to +85°C	20 TSSOP-EP**
MAX9481CUP	-40°C to +85°C	20 TSSOP-EP
MAX9482CUI	-40°C to +85°C	28 TSSOP-EP
MAX9482CGJ*	-40°C to +85°C	32 QFN

**Future product—contact factory for availability.*
***EP = Exposed pad.*

Pin Configurations



Pin Configurations continued at end of data sheet.

Low-Power, Low-Distortion, Central-Office ADSL Drivers and Integrated Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS

V_{CC} to V_{EE} ..... +12V
V_{LP} to V_{LM} ..... +12V
V_{CC} or V_{LP} to DGND ..... -0.3V to +6V
V_{CC} to V_{LP} ..... -0.3V to +6V
V_{EE} or V_{LM} to DGND ..... -6V to +0.3V
V_{EE} to V_{LM} ..... -6V to +0.3V
Current into V_{LP} or V_{LM} ..... ±250mA
IN1+, IN1-, IN2+, IN2- ..... (V_{CC} + 0.3V) to (V_{EE} - 0.3V)
SHDN ..... (V_{CC} + 0.3V) to (V_{EE} - 0.3V)
BOUT1/BOUT2 Output Short-Circuit Duration to V_{CC}/V_{EE}/V_{LP}/V_{LM} ..... Momentary
BOUT1/BOUT2 Output Current 20mA
OUT1/OUT2 Output Short-Circuit Duration to V_{CC}/V_{EE}/V_{LP}/V_{LM} ..... Momentary
OUT1/OUT2 Output Current 1A
OUT1 to OUT2 Short-Circuit Duration ..... Continuous
POUT1/POUT2 Output Short-Circuit Duration to V_{CC}/V_{EE}/V_{LP}/V_{LM} 10s
POUT1/POUT2 Output Current 100mA
RXP/RXM Output Short-Circuit Duration to V_{CC}/V_{EE}/V_{LP}/V_{LM} 10s
RXP/RXM Output Current 100mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP with Pad Connected to V_{EE} (derate 21.7mW/°C above +70°C) 1739mW
20-Pin TSSOP with Floating Pad (derate 11.0mW/°C above +70°C) 879mW
28-Pin TSSOP with Pad Connected to V_{EE} (derate 23.8mW/°C above +70°C) 1905mW
28-Pin TSSOP with Floating Pad (derate 12.8mW/°C above +70°C) 1026mW
32-Pin QFN (derate 23.3mW/°C above +70°C) 1860mW*
Operating Temperature Range (T_{MIN}, T_{MAX}) ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

**Refer to Application Note HFAN-08-1.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{LP} = +2.5V, V_{LM} = -2.5V, DGND = 0, R_L = 16Ω is connected from OUT1 to OUT2, SHDN = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values specified at T_A = +25°C. Preamp configured for A_V = +1 with 1kΩ from POUT_ to IN_-.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Dynamic Power Dissipation	P_{DISS}	$V_{OUT(DIFF)}$ = 1.327V_{RMS}, crest factor = 5.3	MAX9480/ MAX9482		680		mW
			MAX9481		655		
Dynamic Power Consumption	P_{CONS}	$V_{OUT(DIFF)}$ = 1.327V_{RMS}, crest factor = 5.3	MAX9480/ MAX9482		790		mW
			MAX9481		765		
Supply Voltage Range	V_{CC}	(Note 2)		4.75	5.00	5.25	V
	V_{EE}	(Note 2)		-4.75	-5.00	-5.25	
	V_{LP}	(Note 2)		2.25	2.50	2.75	
	V_{LM}	(Note 2)		-2.25	-2.50	-2.75	
Quiescent Supply Current (Including Preamps)	I_{CC}, I_{EE}, I_{LP}, I_{LM}	MAX9480, R_L = ∞	V_{CC}, V_{EE}		21.5	35.0	mA
			V_{LP}, V_{LM}		22.0	40.0	
		MAX9481, R_L = ∞	V_{CC}, V_{EE}		20.0	34.0	
			V_{LP}, V_{LM}		21.0	39.0	
		MAX9482, R_L = ∞	V_{CC}, V_{EE}		21.5	35.0	
			V_{LP}, V_{LM}		22.0	40.0	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{LP} = +2.5V, V_{LM} = -2.5V, DGND = 0, R_L = 16Ω is connected from OUT1 to OUT2, SHDN = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values specified at T_A = +25°C. Preamp configured for A_V = +1 with 1kΩ from POUT_ to IN_-.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Shutdown Supply Current	I_{SD}	MAX9480, R_L = ∞	V_{CC}, V_{EE}		2.1	6.0	mA
			V_{LP}, V_{LM}		1.5	5.0	
		MAX9481, R_L = ∞	V_{CC}, V_{EE}		0.6	1.2	
			V_{LP}, V_{LM}		0.05	0.1	
		MAX9482, R_L = ∞	V_{CC}, V_{EE}		2.1	6.0	
			V_{LP}, V_{LM}		1.5	5.0	
Transmit Path Power-Supply Rejection Ratio (Single Ended)	PSRR	V_{CC} - V_{EE} = ±4.75V to ±5.25V		50	76		dB
		V_{LP} - V_{LM} = ±2.25V to ±2.75V		50	81		
Common-Mode Rejection	CMR	-200mV ≤ V_{CM} ≤ +200mV			46		dB
Hybrid Rejection Ratio (MAX9480 Only)	HRR	$V_{OUT(DIFF)}$ = ±1.2V			35		dB
Driver-to-Receiver Crosstalk (MAX9482 Only)	X_{TALK}	f = 100kHz			-69		dB
SHDN Logic Low	V_{IL}					0.8	V
SHDN Logic High	V_{IH}			2.0			V
SHDN Input Current	I_{IH}, I_{IL}	SHDN = 0 or SHDN = V_{CC}				±5.0	µA
Shutdown Delay Time	t_{SHDN}				4.8		µs
Shutdown Enable Time	t_{ENABLE}				4		µs
Intermodulation Distortion	I_{MD}	f1 = 1MHz, f2 = 900kHz, *Typical Operating Circuit*, $V_{OUT(DIFF)}$ = $2.0V_{P-P}$			-66		dB
DRIVER							
Maximum RMS Output Power (*Typical Operating Circuit*) (Note 3)	P_{OUT}	DMT modulation (crest factor, Cr = 5.33)		21.4			dBmW
		CAP modulation (crest factor, Cr = 4.00)		24.3			
Closed-Loop Gain	G	$V_{OUT(DIFF)}$ = $1.2V_{P-P}$		-2.7	-3	-3.3	V/V
Second Harmonic Distortion		f = 1MHz, $V_{OUT(DIFF)}$ = $14V_{P-P}$, *Typical Operating Circuit* (Note 4)			-71		dB
Third Harmonic Distortion		f = 1MHz, $V_{OUT(DIFF)}$ = $14V_{P-P}$, *Typical Operating Circuit* (Note 4)			-74		dB
Differential Output Voltage Swing	$V_{OUT(DIFF)}$	*Typical Operating Circuit* (Note 4)			15.0		V_{P-P}
OUT_ Voltage Swing (per Amplifier) (Note 4)	V_{OH}, V_{OL}	R_L = 100Ω	V_{CC} - V_{OH}		0.5		V
			|V_{EE} - V_{OL}|		0.5		
		R_L = 16Ω	V_{CC} - V_{OH}		1.27		
			|V_{EE} - V_{OL}|		1.21		
BOUT_ Voltage Swing (per Amplifier) (Note 4)	V_{BOH}, V_{BOL}		V_{CC} - V_{BOH}		0.45		V
			|V_{EE} - V_{BOL}|		0.42		
Peak Output Current	I_{OUT}				500		mA
Differential Output Offset Voltage	$V_{OS(DIFF)}$	IN1+ = IN2+ = 0			±5		mV

Low-Power, Low-Distortion, Central-Office ADSL Drivers and Integrated Drivers/Receivers

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{LP} = +2.5V, V_{LM} = -2.5V, DGND = 0, R_L = 16Ω is connected from OUT1 to OUT2, SHDN = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values specified at T_A = +25°C. Preamp configured for A_V = +1 with 1kΩ from POUT_ to IN_-.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Output Offset-Voltage Drift	$V_{OS(DRIFT)}$			±12		µV/°C
Output Resistance (per Amplifier)	R_{OUT}	-200mV ≤ V_{OUT} ≤ +200mV	6	8	10	Ω
		SHDN = V_{CC}		8		
-3dB Bandwidth	BW			80		MHz
Slew Rate	SR	$V_{OUT(DIFF)}$ = 14V_{P-P} step		250		V/µs
Output Noise PSD	P_N	f = 100kHz to 1.1MHz, referred to 100Ω line		-127		dBm/Hz
Capacitive Load Stability		No sustained oscillations		1000		pF
PREAMPS AND RECEIVERS (Note 5)						
Open-Loop Transimpedance	Z_{OL}	-2V ≤ P_{OUT} ≤ +2V		300		kΩ
Power-Supply Rejection Ratio	PSRR	V_{CC} - V_{EE} = ±4.75V to ±5.25V	50	87		dB
		V_{LP} - V_{LM} = ±2.25V to ±2.75V	50	100		
Input Offset Voltage	V_{OS}			±2	±10	mV
IN1+, IN2+, RXIN1+, RXIN2+ Bias Current	I_{B+}			±1	±20	µA
IN1+, IN2+, RXIN1+, RXIN2+ Bias Current Matching	I_{OS+}			±0.7		µA
IN1-, IN2-, RXIN1-, RXIN2- Bias Current	I_{B-}			±2.6	±20	µA
IN1-, IN2-, RXIN1-, RXIN2- Bias Current Matching	I_{OS-}			±1.2		µA
Input Resistance	R_{IN}	IN1+, IN2+, RXIN1+, RXIN2+		1.1		MΩ
		IN1-, IN2-, RXIN1-, RXIN2-		200		Ω
Input Capacitance	C_{IN}	IN1+, IN2+, IN1-, IN2-, RXIN1+, RXIN2+, RXIN1-, RXIN2-		2		pF

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 2: Guaranteed by the PSRR test.
Note 3: Implied by worst-case output voltage swing ($V_{OUT(DIFF)}$), crest factor (Cr), and load impedance (R_L):

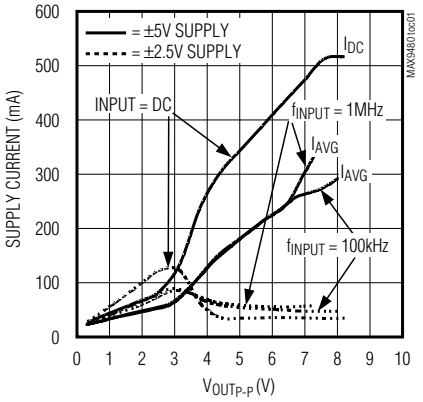
$$P_{DRIVER} = 10\log_{10}\left(\frac{250 \times V^2_{OUT(DIFF)}}{Cr^2 \times R_L}\right) dBmW$$

Note 4: Device may exceed absolute maximum ratings for power dissipation if unit is subjected to full-scale sinusoids for long periods. See the *Applications Information* section.
Note 5: Receiver specifications guaranteed for MAX9482 only.

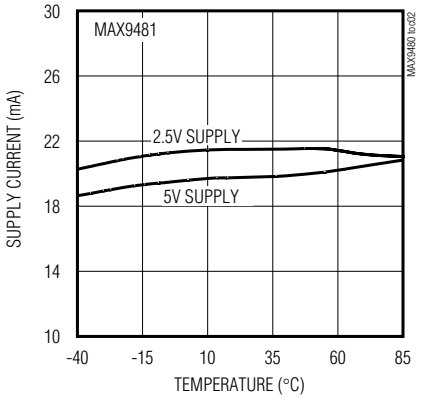
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5V, V_{LP} = +2.5V, V_{LM} = -2.5V, DGND = 0, RXIN1+ = RXIN2+ = 0, IN1+ = IN2+ = 0, R_L = 16Ω is connected from OUT1 to OUT2, SHDN = 0, T_A = +25°C, unless otherwise noted. Preamp configured for A_V = +1 with 1kΩ from RXOUT_- to RXIN_-. Receiver configured for A_V = +1 with 1kΩ from POUT_ to IN_-.)

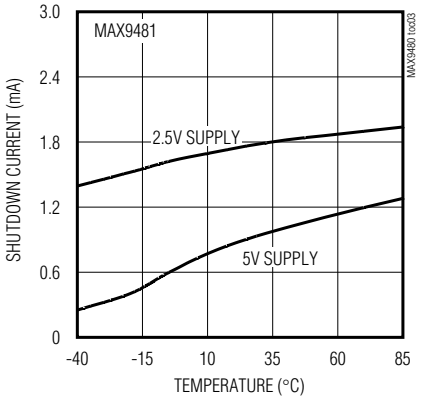
SUPPLY CURRENT vs. OUTPUT VOLTAGE



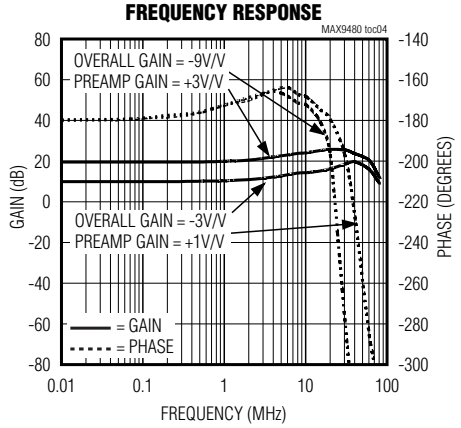
SUPPLY CURRENT vs. TEMPERATURE



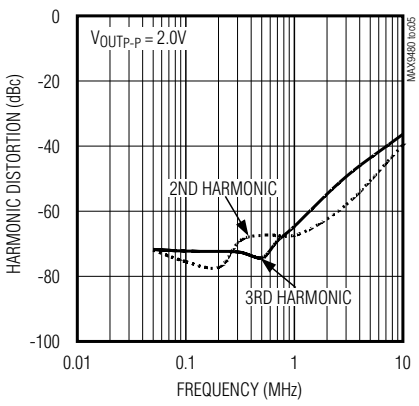
SHUTDOWN CURRENT vs. TEMPERATURE



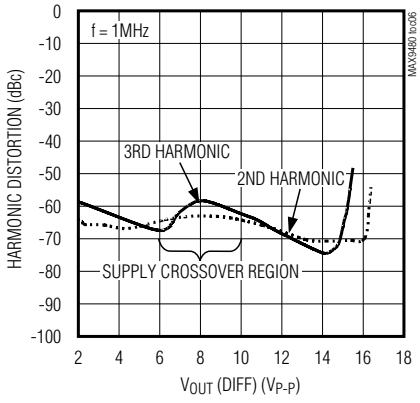
TRANSMIT PATH FREQUENCY RESPONSE



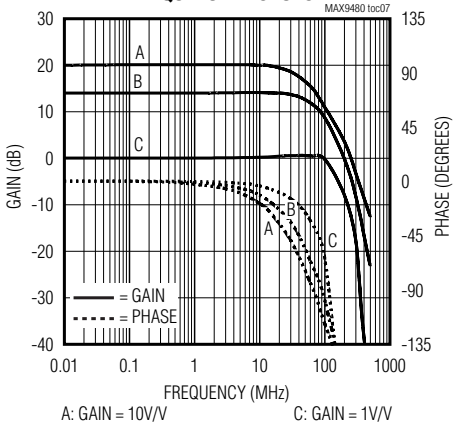
DRIVER HARMONIC DISTORTION vs. FREQUENCY



DRIVER HARMONIC DISTORTION vs. OUTPUT VOLTAGE



RECEIVER AMPLIFIER FREQUENCY RESPONSE



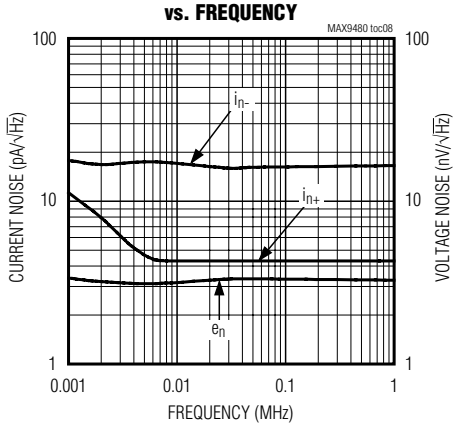
A: GAIN = 10V/V
B: GAIN = 5V/V
C: GAIN = 1V/V

Low-Power, Low-Distortion, Central-Office ADSL Drivers and Integrated Drivers/Receivers

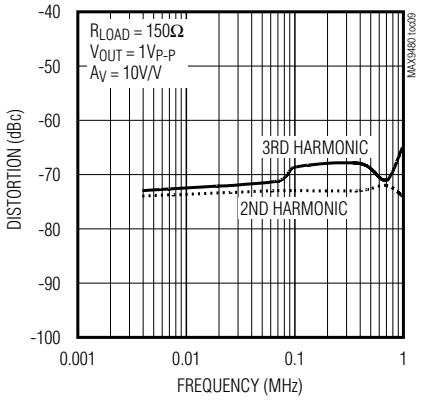
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{LP} = +2.5V, V_{LM} = -2.5V, DGND = 0, RXIN1+ = RXIN2+ = 0, IN1+ = IN2+ = 0, R_L = 16Ω is connected from OUT1 to OUT2, SHDN = 0, T_A = +25°C, unless otherwise noted. Preamp configured for A_V = +1 with 1kΩ from RXOUT_- to RXIN_-. Receiver configured for A_V = +1 with 1kΩ from POUT_ to IN_-.)

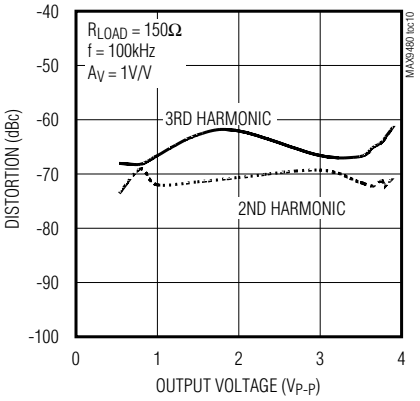
RECEIVER INPUT NOISE vs. FREQUENCY



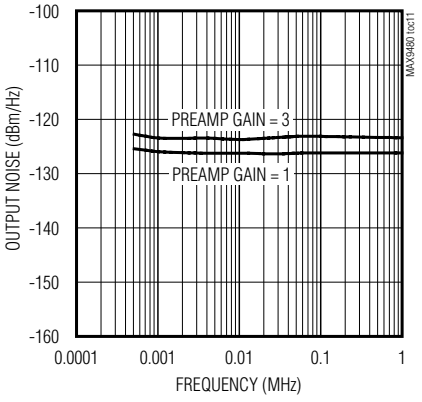
RECEIVER AMPLIFIER HARMONIC DISTORTION vs. FREQUENCY



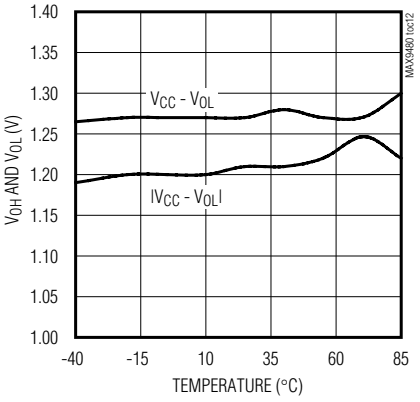
RECEIVER AMPLIFIER HARMONIC DISTORTION vs. OUTPUT AMPLITUDE



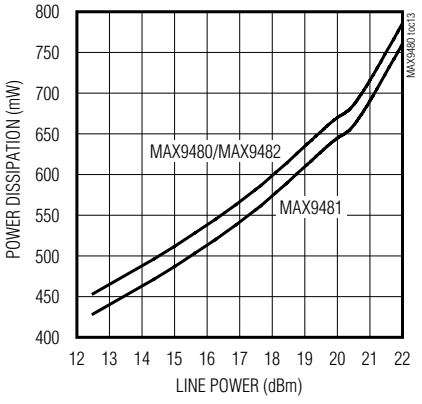
OUTPUT NOISE vs. FREQUENCY



V_{OH} AND V_{OL} vs. TEMPERATURE



POWER DISSIPATION vs. LINE POWER



Pin Description

PIN				NAME	FUNCTION
MAX9480	MAX9481	MAX9482			
		TSSOP	QFN		
1	2	2	31	POUT1	First Preamp Output
2	3	3	1	IN1-	First Inverting Input
3	4	4	2	IN1+	First Noninverting Input
4	—	11	10	RXP	Positive Receiver Output from Internal Hybrid
5	5	5	3	DGND	Ground
6	6	6	4	SHDN	Shutdown Control Pin
7	—	16	15	RXM	Negative Receiver Output from Internal Hybrid
8	7	7	5	IN2+	Second Preamp Noninverting Input
9	8	8	6	IN2-	Second Preamp Inverting Input
10	9	9	7	POUT2	Second Preamp Output
11, 20	11, 20	18, 28	17, 28	V_{LM}	-2.5V Negative Power-Supply Voltage
12, 19	12, 19	19, 27	18, 27	V_{LP}	+2.5V Positive Power-Supply Voltage
13, 18	13, 18	20, 25	19, 24	V_{CC}	+5V Positive Power-Supply Voltage
14	14	21	20	OUT2	Second Driver Output
15, 16	15, 16	22, 23	21, 22	V_{EE}	-5V First Negative Power-Supply Voltage
17	17	24	23	OUT1	First Driver Output
—	1	1	30	BOUT1	First Driver Output Sense
—	10	10	8	BOUT2	Second Driver Output Sense
—	—	12	11	RXIN1-	First Receiver Inverting Input
—	—	13	12	RXIN1+	First Receiver Noninverting Input
—	—	14	13	RXIN2+	Second Receiver Noninverting Input
—	—	15	14	RXIN2-	Second Receiver Inverting Input
—	—	17, 26	9, 16, 25, 26, 29, 32	N.C.	Not Internally Connected
EP	EP	EP	EP	V_{EE}	Exposed pad internally connected to V_{EE}. See the *Applications Information* section.

Low-Power, Low-Distortion, Central-Office ADSL Drivers and Integrated Drivers/Receivers

Detailed Description

The MAX9480/MAX9481/MAX9482 are fully differential line transceivers for ADSL applications. Each transmit path has a high-bandwidth, low-distortion, current-feedback operational amplifier followed by a fixed-gain class-G output buffer.

The MAX9480/MAX9481/MAX9482 are class-G devices and require two dual power supplies, ±5V and ±2.5V. All preamplifier inputs and outputs are available to allow external gain configuration. The MAX9480 contains an internal hybrid echo cancellation circuit with receiver amplifiers set to a fixed gain of 4.6V/V. The MAX9482 has no internal hybrid, but contains two uncommitted low-noise op amps for coupling to an external hybrid network. The MAX9481 has only the preamp and line-driver circuits.

The two class-G output buffers are internally configured for an inverting gain of three, and employ an active termination scheme that presents an 8Ω load to incoming signals. The buffers are designed for use with a 1:2.5 line transformer and can deliver 20.4dBm average line power with a signal crest factor of 5.3 into a standard 100Ω line. The outputs are designed to be directly DC- or AC-bridged across the transformer.

The MAX9480/MAX9481/MAX9482 have a low-output impedance, low-power shutdown mode that is activated by driving SHDN high. Transmit path amplifiers and buffers are disabled while the part is in shutdown, and an 8Ω resistor is coupled directly between OUT_ and the output of a three-state buffer referenced to DGND (0V). The receive amplifiers remain active in shutdown mode.

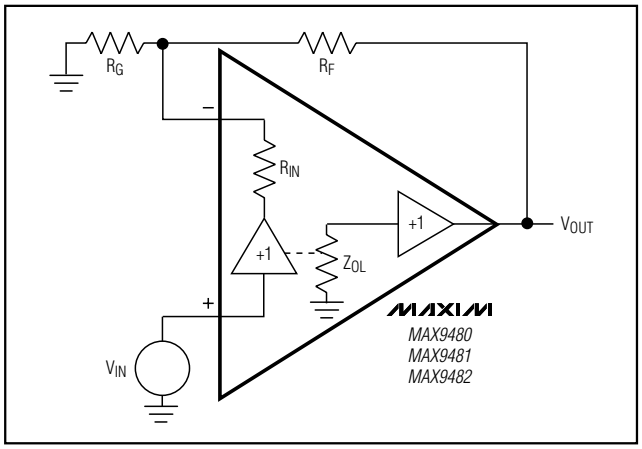


Figure 1. Current Feedback Amplifier Block Diagram

Applications Information

Theory of Operation

The preamplifiers and receivers are current-feedback amplifiers; thus, their open-loop transfer function is expressed as a transimpedance, $\Delta V_{OUT}/\Delta I_{IN}$, or Z_{OL}. The frequency behavior of their open-loop transimpedance is similar to the open-loop gain of a voltage-feedback amplifier; that is, they have a large DC value that decreases at approximately 6dB per octave. Analyzing the follower with gain, as shown in Figure 1, yields the following transfer function:

$$\frac{V_{OUT}}{V_{IN}} = G \times \frac{Z_{OL(S)}}{Z_{OL(S)} + G \times (R_{IN} + R_F)} \quad [\text{Equation 1}]$$

where $G = A_{VCL} = 1 + (R_F/R_G)$, and $R_{IN} = 1/g_M \neq 200\Omega$.

At low gains, $G \times R_{IN} << R_F$. Therefore, the closed-loop bandwidth is essentially independent of closed-loop gain. Similarly, $Z_{OL} >> R_F$ at low frequencies, so that:

$$\frac{V_{OUT}}{V_{IN}} = G = 1 + \frac{R_F}{R_G} \quad [\text{Equation 2}]$$

Shutdown

Forcing SHDN high puts the MAX9480/MAX9481/MAX9482 into low-power shutdown mode. In shutdown mode, OUT1 and OUT2 are low impedance, and the power-supply currents drop to less than 10% of their normal quiescent operating values. When coming out of shutdown, allow about 1.5µs before commencing operation.

PC Board Layout

Power-Supply Bypassing

The MAX9480/MAX9481/MAX9482 are wide-bandwidth devices and require careful board layout, including the possible use of constant-impedance microstrip or stripline techniques. To realize the full AC performance of these high-speed amplifiers, pay careful attention to power-supply bypassing. The PC board should have at least two layers: a signal and power layer on one side, and a large, low-impedance ground plane on the other side. The ground plane should be as free of voids as possible. With multilayer boards, locate the ground plane on a layer that incorporates no signal or power traces. Observe the following guidelines when designing the board. IC sockets increase parasitic capacitance and inductance, and should not be used. Do not make 90° turns; round all corners. Observe high-frequency bypassing techniques to maintain the amplifier's

accuracy. The bypass capacitors should include a 0.1µF ceramic capacitor between each supply pin and the ground plane, located as close to the package as possible. Additionally, place a 1µF to 10µF ceramic or tantalum capacitor in parallel with each 0.1µF capacitor, and as close to them as possible. Place a 10µF to 15µF low-ESR tantalum capacitor at the V_{CC}, V_{LM}, and V_{LP} power-supply points of entry to the PC board. Place a 100µF to 220µF low-ESR tantalum capacitor at the V_{EE} power-supply point of entry to the PC board. The power-supply traces should lead directly from the board input capacitors to V_{CC} and V_{EE}. To minimize parasitic inductance, keep PC traces short and use surface-mount components. Wire-wrapped boards are much too inductive, and breadboards are much too capacitive; neither should be used. Power-supply sequencing is required; apply ±5.0 before applying ±2.5V.

Exposed-Pad Connection

For optimum electrical performance, the EP of the MAX9480/MAX9481/MAX9482 should be soldered to the PC board and electrically connected to V_{EE} with as wide a trace as possible. If using the EP, the 100µF to 220µF low-ESR tantalum capacitor should be used to decouple the EP to the ground plane of the PC board as close to the EP region as possible. For optimum thermal performance, the EP should be additionally connected to a heat sink, as described in the *Thermal Protection and Power Dissipation* section.

Preamp Output Bypassing

In addition to the above layout considerations, and independent of the gain setting, some high-frequency bypassing of the preamp outputs is necessary to prevent instability arising from the high-frequency input impedance characteristics of the buffers. A 50Ω resistor in series with a 2200pF ceramic capacitor should be connected between POUT_ and DGND, with a 47pF capacitor connected directly between POUT_ and DGND.

Choosing Feedback and Gain Resistors

The MAX9480/MAX9481/MAX9482 use current-feedback amplifiers. Figure 2 shows the standard inverting and noninverting configurations. Notice that the gain of the noninverting circuit, Figure 2(b), is 1 plus the magnitude of the inverting closed-loop gain. Increasing feedback resistor values decreases peaking. Use the input resistor, R_G, to change the magnitude of the gain. Do not use feedback capacitance.

DC and Noise Errors

There are several error sources to consider when using any operational amplifier, and this applies to the MAX9480/MAX9481/MAX9482 as well. Offset-error terms are given by equations 3 and 4. Voltage and current-noise errors are root-square summed and therefore computed separately. In Figure 3, the total output offset voltage is determined by:

- The input offset voltage, V_{OS}, times the closed-loop gain (1 + (R_F / R_G)).
- The positive input bias current, I_{B+}, times the source resistor, R_S (typically less than 10Ω), plus the negative input bias current, I_{B-}, times the parallel combination of R_G and R_F. In current-mode feedback amplifiers, the input bias currents may flow into or out of the device. For this reason, there is no benefit to matching the resistance at both inputs, as is common in voltage-feedback amplifiers.

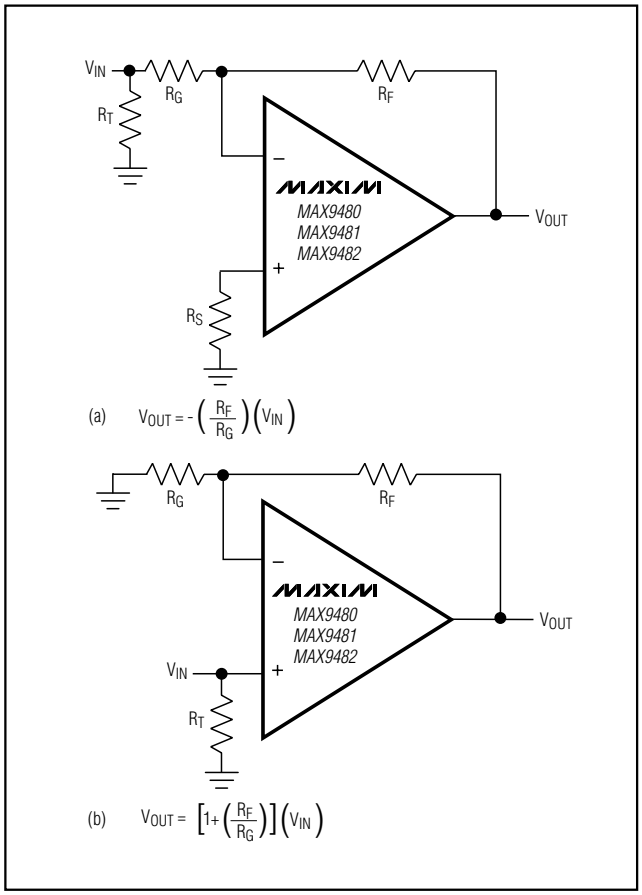


Figure 2. Inverting Gain Configuration and Noninverting Gain Configuration

Low-Power, Low-Distortion, Central-Office ADSL Drivers and Integrated Drivers/Receivers

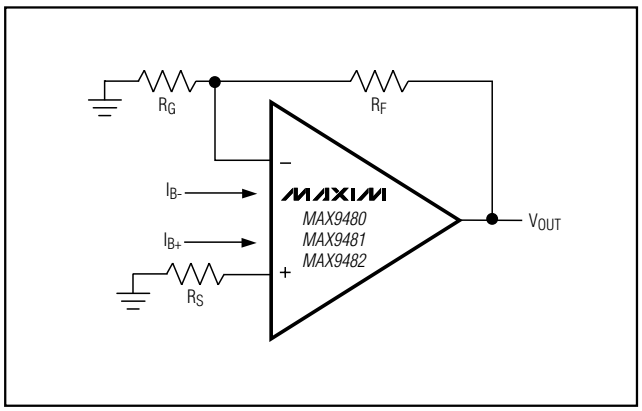


Figure 3. Input Offset Voltage and Current

The equation for total DC error is:

[Equation 3]

$$V_{OUT} = \left[(I_{B+})R_S + (I_{B-})(R_F \,||\, R_G) + V_{OS}\right]\left(1 + \frac{R_F}{R_G}\right)$$

The total output-referred noise voltage is:

[Equation 4]

$$e_{n(OUT)} = \left(1 + \frac{R_F}{R_G}\right)\sqrt{\left[(i_{n+})Rs\right]^2 + \left[(i_{n-})R_F \,||\, R_G\right]^2 + (e_n)^2}$$

The MAX9480/MAX9481/MAX9482 have very low noise input voltage (e_n), 3.5nV/√Hz (typ). The current noise at the noninverting input (i_{n+}) is 4.0pA/√Hz (typ), and the current noise at the inverting input, i_{n-}, is 15pA/√Hz (typ).

An example of the DC error calculations, using the MAX9480 data and the *Typical Operating Circuit* where $R_F = R_G = 1k\Omega$ ($R_F \,||\, R_G = 500\Omega$) and $R_S = 50\Omega$, gives the following, using equation 3:

$$V_{OUT} = \left[\begin{array}{l}\left(1.0\times10^{-6}\right)50 + \left(2.6\times10^{-6}\right)\left(\dfrac{1000\times1000}{1000+1000}\right) \\ +0.002\ x\left(1+\dfrac{1000}{1000}\right)\end{array}\right]$$

where V_{OUT} = 6.7mV at the preamp outputs.

Calculating total preamp output noise using equation 4 yields 16.6nV/√Hz, which then contributes 50nV/√Hz at the driver output. The driver noise contributes an additional 35mV/√Hz, to the overall output noise.

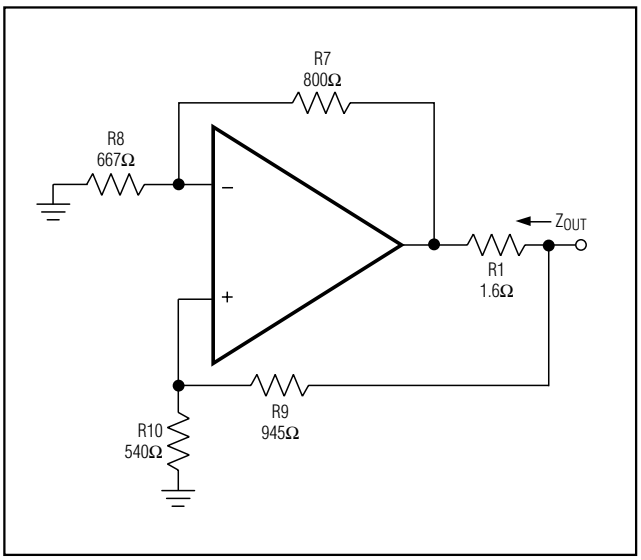


Figure 4. Active Line Termination Scheme, Single Side

Driving Capacitive Loads

The MAX9480/MAX9481/MAX9482 receive amplifiers are optimized for AC performance. They are not designed to drive highly capacitive loads. Reactive loads decrease phase margin and can produce excessive ringing and oscillation.

Output-Impedance Synthesis

To help meet the contradictory requirements of high output power and low-power use, the active termination circuit shown in Figure 5 is used. This circuit is designed to present a line termination of 8Ω. R1 is a physical 1.6Ω resistor voltage feedback from the outboard end of R1 to the noninverting input of the amplifier, introduces positive feedback, which increases the effective output-impedance value from 1.6Ω to 8Ω. Hence, the impedance looking into the port matches the line impedance reflected through the transformer.

Assuming an ideal amplifier, the following equation expresses the output impedance:

$$Z_{OUT} = \frac{R_1}{1 - \left(1 + \dfrac{R_7}{R_8}\right)\dfrac{R_{10}}{R_9 + R_{10}}} \qquad \text{[Equation 5]}$$

Substituting the values of the resistors shown in Figure 4 into equation 5, we obtain $Z_{OUT} = 8\Omega$.

The output equivalent circuit for the line driver is shown in Figure 5.

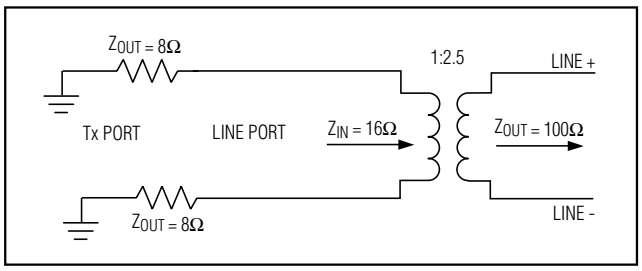


Figure 5. Output Equivalent Circuit

With a 1:2.5 transformer, the two 8Ω impedances realized by the active-feedback network form a perfect line termination. The MAX9480 family's active termination design makes it possible to use a ±5V power supply instead of ±12V or ±15V, significantly increasing driver efficiency.

Hybrid Considerations

The MAX9480 includes an internal hybrid coupling circuit to realize the receive function with no external components. The hybrid couples the transmitted signal from the line-driver port (Tx port) to the line port and cancels the echo in the receiving port (Rx port). The hybrid circuit is detailed in Figure 6. If using the MAX9481 or the MAX9482, external circuitry must be added to realize a receive function. The MAX9482 includes two uncommitted op amps for this purpose.

A traditional hybrid network with a 2:1 resistor ratio must be replaced with a 1.2:1 ratio to achieve nominal echo cancellation. Additionally, the use of a synthesized output impedance has the side effect of preventing a "virtual-ground" condition at the driver output (BOUT), as seen by the receive signal. Hence, the resulting hybrid circuit exhibits an increased attenuation of the receive signal with respect to a traditional case with no synthesis. For central-office ADSL applications, the noise specifications allow this trade-off to be made.

Pseudo-Class-G Amplifier

The driver consists of two stages: the current-feedback preamplifier and the voltage-feedback buffer. To save power, the preamplifier uses a power supply of only ±2.5V. The output swing of the preamplifier is about $3.0V_{P-P}$. The buffer is designed as a pseudo-class-G amplifier with a fixed gain of -3V/V. This buffer stage employs two power supplies: a lower voltage supply, ±2.5V, and a higher voltage supply, ±5V. In the differential driver, two parallel amplifiers provide the output current to the load, as shown in Figure 7.

In this pseudo-class-G amplifier, there is no abrupt supply switchover between the higher voltage and the lower voltage amplifiers, as in a traditional class G. It is a seamless transition that depends only on the amplitude of the input signal and the gain. The lower voltage amplifier has a high conversion conductance, G_A, and the higher voltage amplifier has a low conductance, G_B. With a low input voltage, the lower voltage amplifier provides most of the output current to the load. As the voltage of the input signal increases, the lower voltage amplifier starts to saturate and the higher voltage amplifier begins to drive the output.

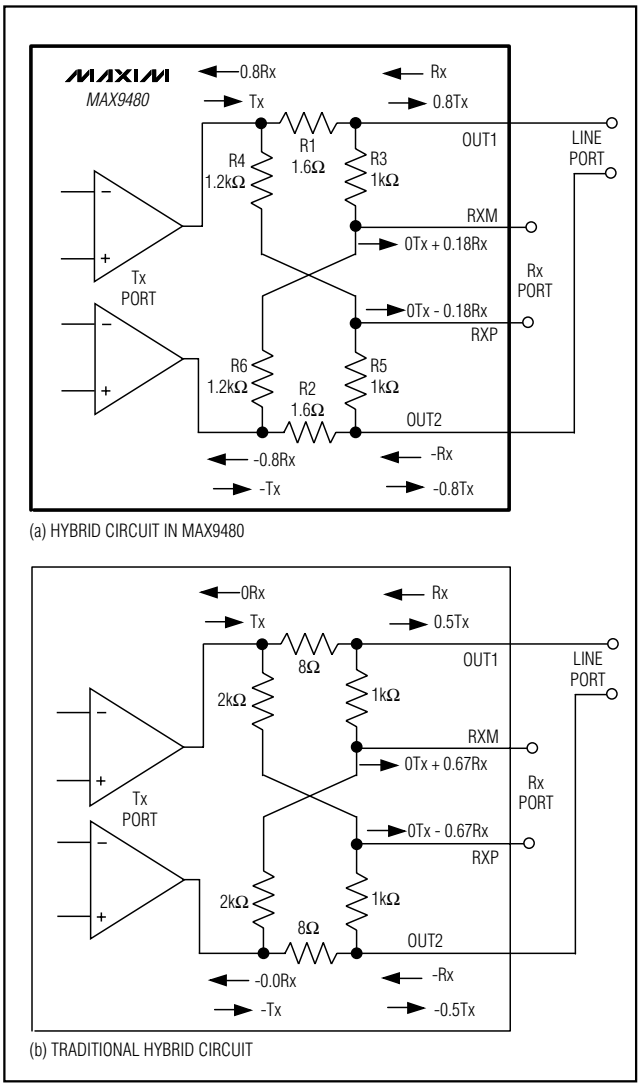


Figure 6. Hybrid Circuit in the MAX9480

Low-Power, Low-Distortion, Central-Office ADSL Drivers and Integrated Drivers/Receivers

This smooth transition between the lower voltage amplifier and the higher voltage amplifier guarantees no glitch on the output signal, and ensures high linearity for high output power, while at the same time consuming minimum power. The relation between the input voltage and the output current of this pseudo-class-G buffer is illustrated in Figure 8.

Thermal Protection and Power Dissipation

The MAX9480/MAX9481/MAX9482 are available in the EP version of the TSSOP. The EP facilitates heat transfer out of the package if the pad is soldered to a heat sink made from an area of circuit board copper. Connect this copper dissipation area to V_{EE}. For a DMT-modulated signal with a crest factor greater than or equal to 5.3, the power dissipation of the MAX9480/MAX9481/MAX9482 should not exceed 700mW; the 20-pin TSSOP-EP package with its EP floating allows 714mW peak power at +85°C. Hence, heat sinking is not essential, but is desirable for attaining optimal electrical performance. Note that the part is capable of 500mA peak output current, which could cause thermal shutdown in applications with elevated ambient temperatures and/or signals with low crest factors. The thermal shutdown feature prevents the die temperature from exceeding +150°C. See Figure 9 for a guide to power derating for each of the packages.

Transformer Selection

Full-rate, central-office ADSL requires the transmission of a +20.4dBm (110mW) DMT signal. The DMT signal has a typical crest factor of 5.3, requiring the line driver to provide peak line power of 35.4dBm (3.4W). The 35.4dBm peak line power translates to a 36V peak-to-peak differential voltage on a 100Ω line. The output swing available from the MAX9480 family of line drivers with a ±5V supply is 15.0V_{P-P}, and hence a step-up transformer with turns ratio of 1:2.5 is needed. In the *Typical Operating Circuit*, the MAX9480 is coupled to the phone line through just such a transformer. The total differential load for the MAX9480 is therefore 16Ω. Active termination is included on all devices in the MAX9480 family (as explained above in the *Output-Impedance Synthesis* section).

Receiver Channel Considerations

A step-up transformer at the output of the differential line driver has a step-down effect on signals received from the line. A voltage attenuation equal to the inverse of the turns ratio is realized in the receive channel. This is an addition to the attenuation due to the hybrid circuitry itself (see the *Hybrid Considerations* section).

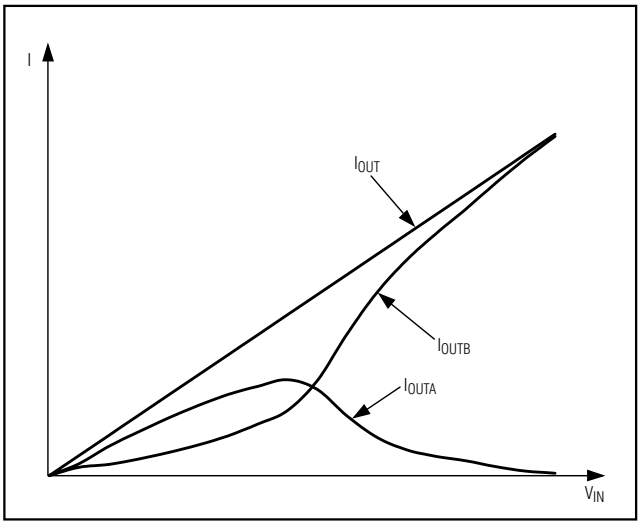


Figure 8. Amplifier Output Characteristics

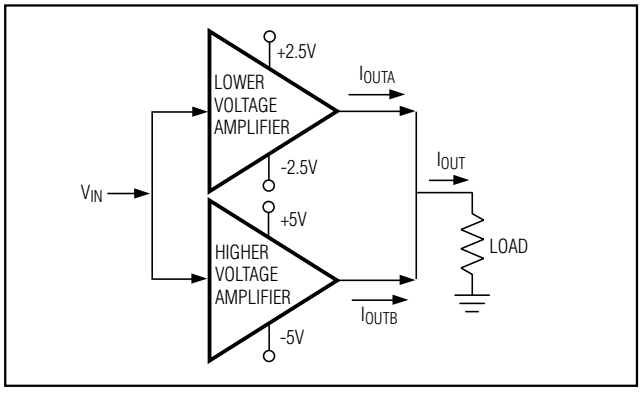


Figure 7. Output Stage of Pseudo-Class-G Amplifier

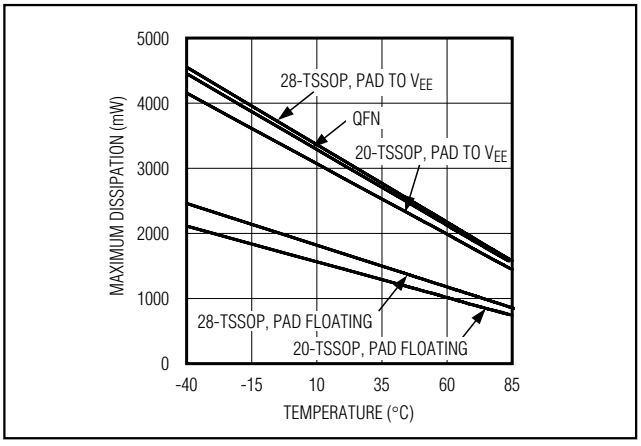
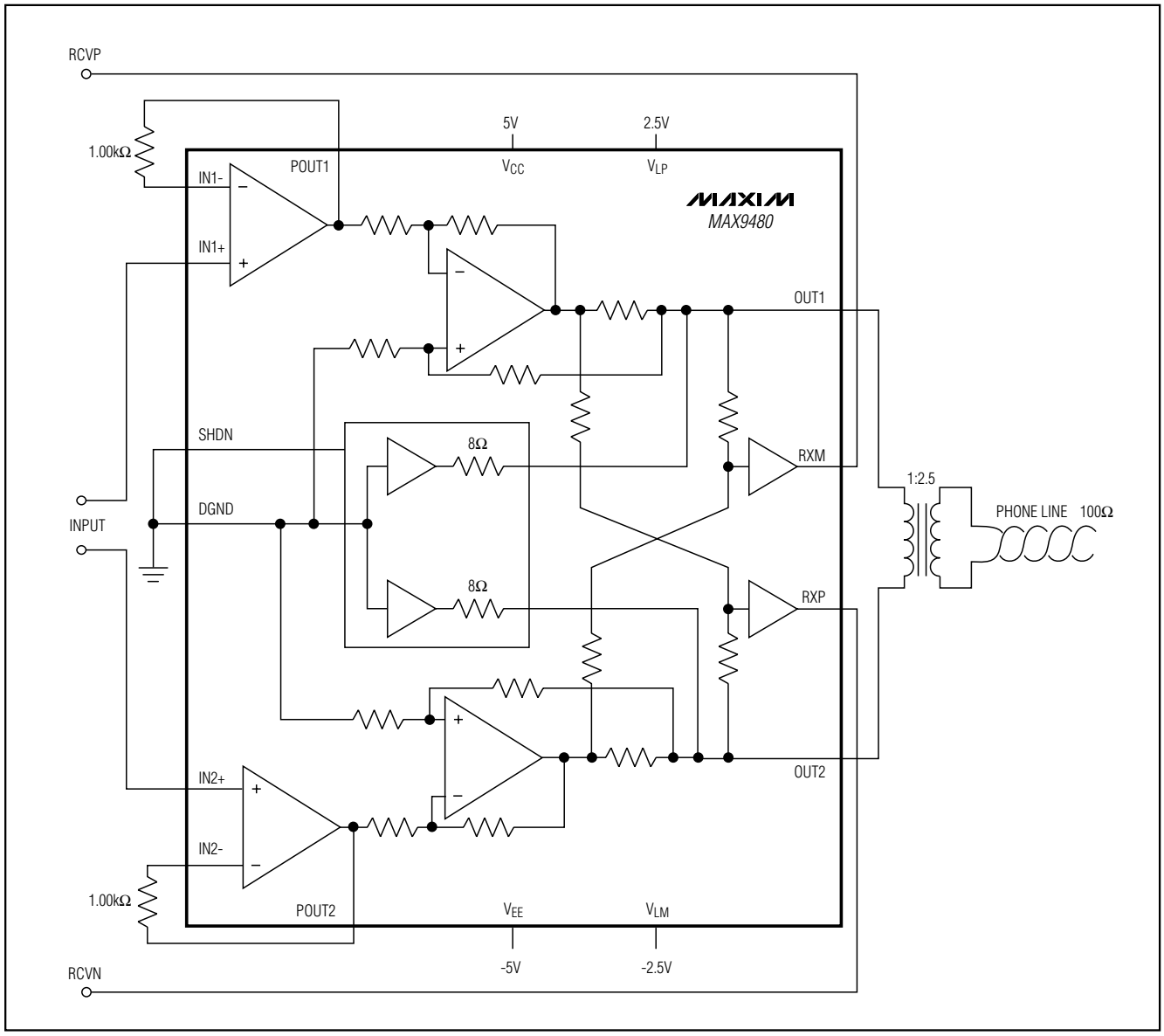


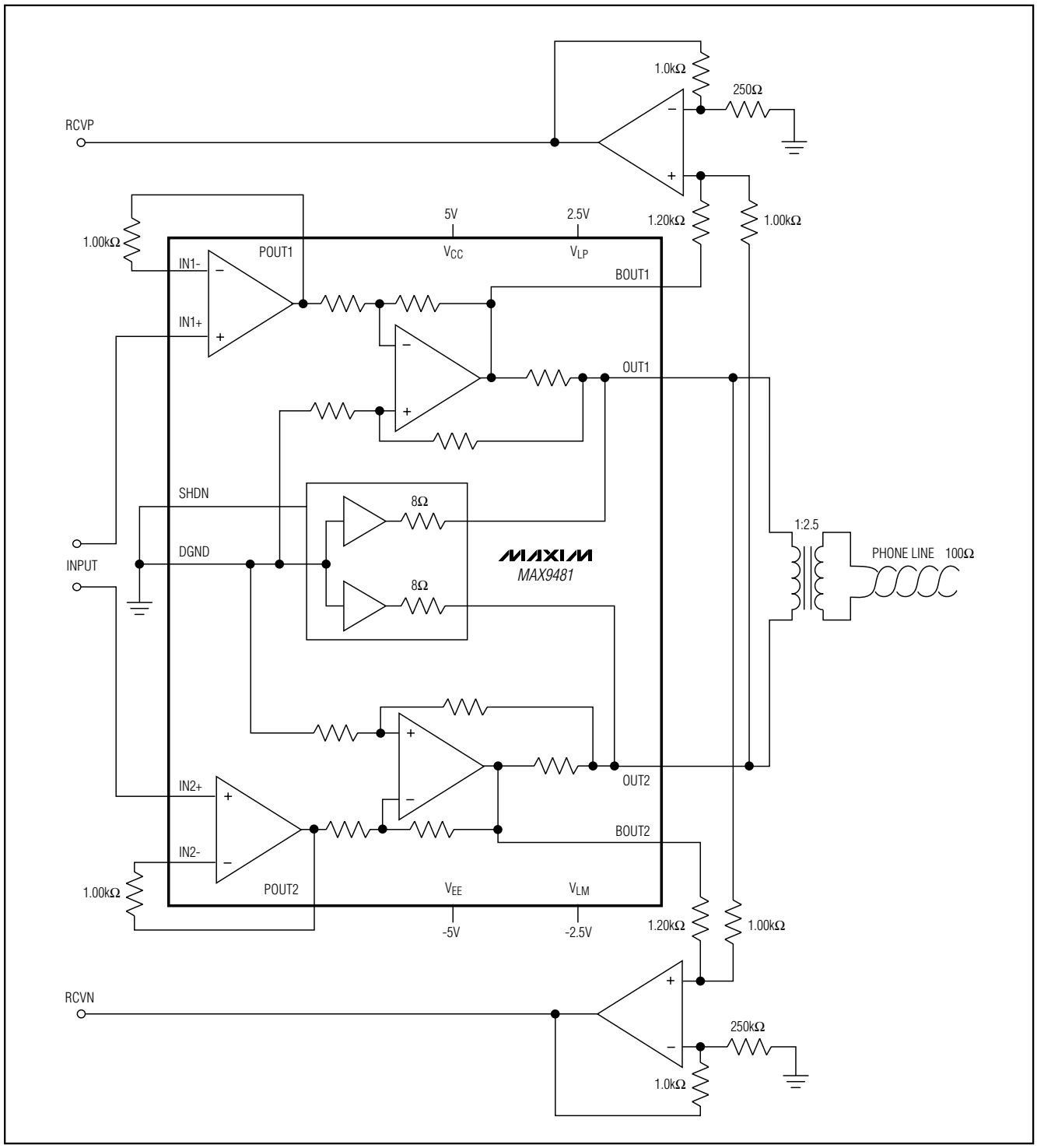
Figure 9. Maximum Power Dissipation vs. Temperature

Typical Operating Circuits

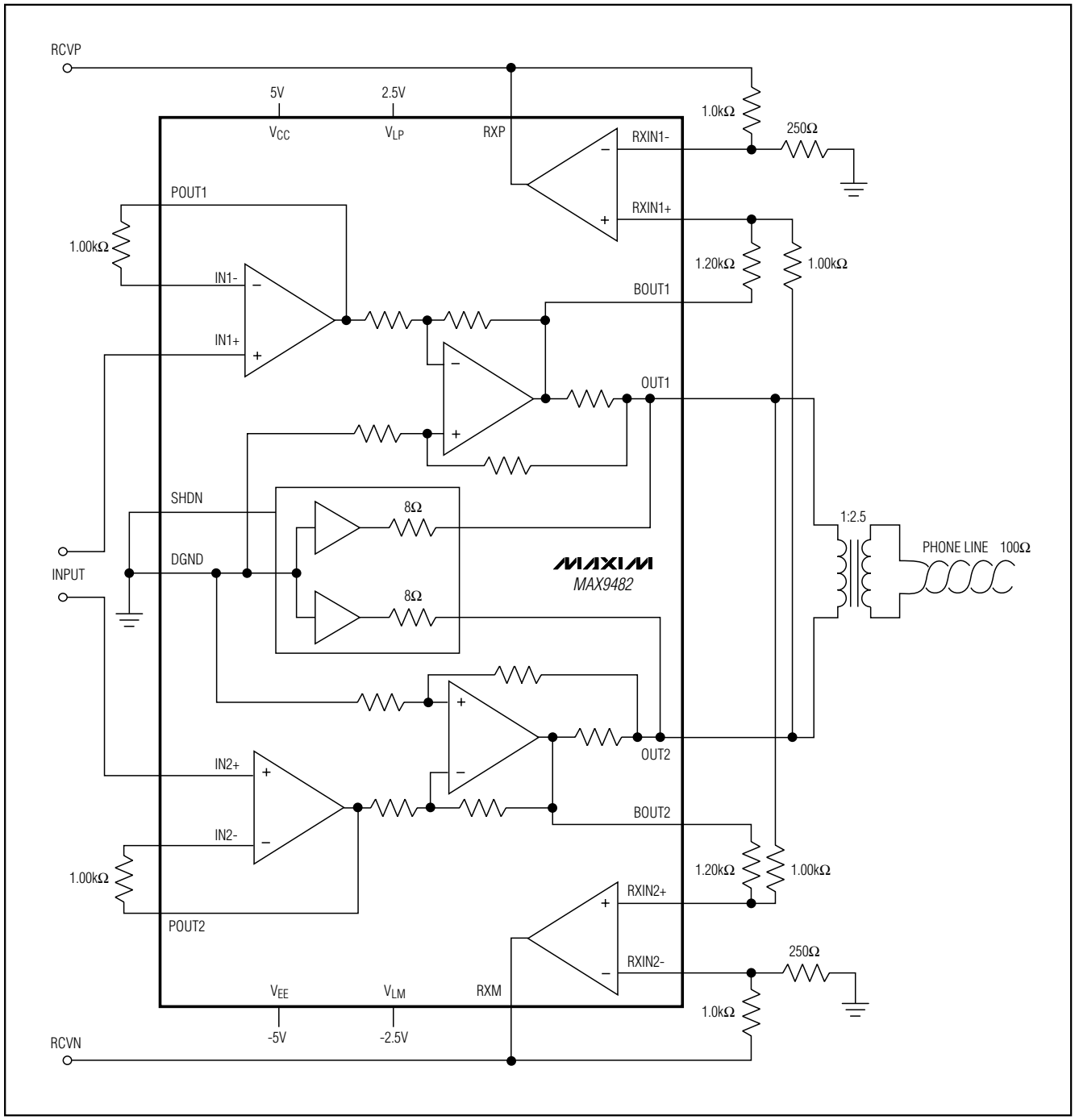


Low-Power, Low-Distortion, Central-Office ADSL Drivers and Integrated Drivers/Receivers

Typical Operating Circuits (continued)

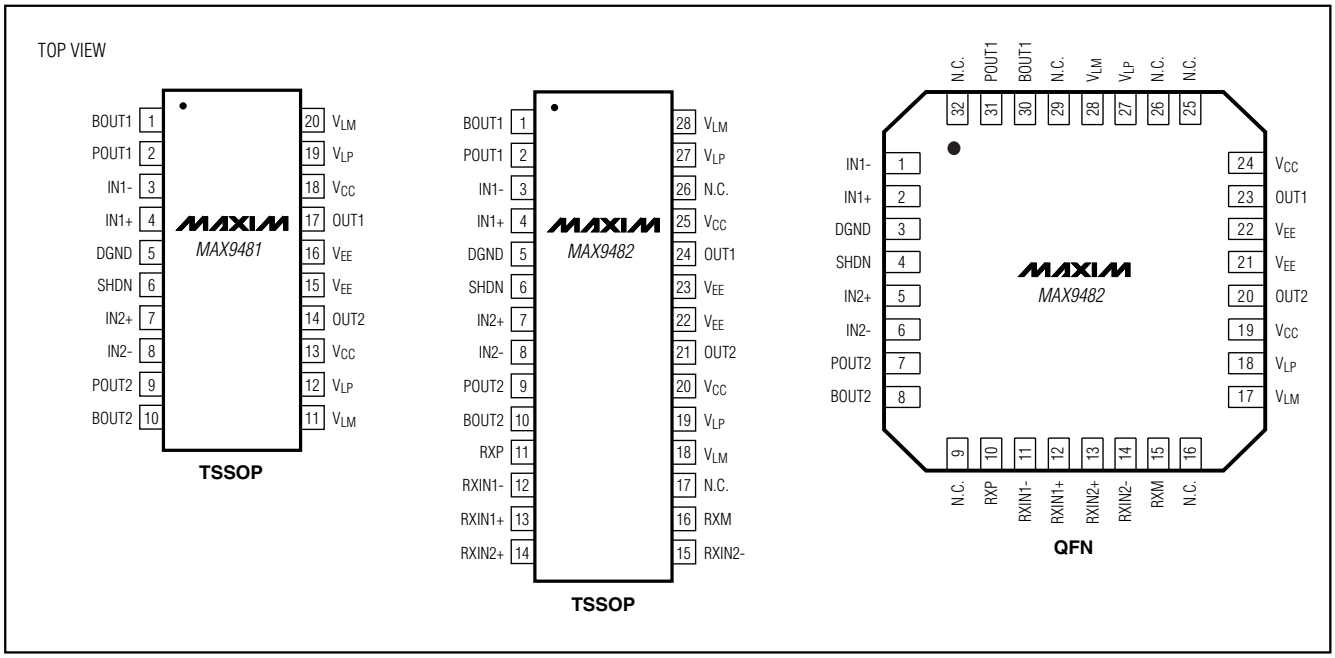


Typical Operating Circuits (continued)



Low-Power, Low-Distortion, Central-Office ADSL Drivers and Integrated Drivers/Receivers

Pin Configurations (continued)



Chip Information

MAX9480 TRANSISTOR COUNT: 2557

MAX9481 TRANSISTOR COUNT: 2557

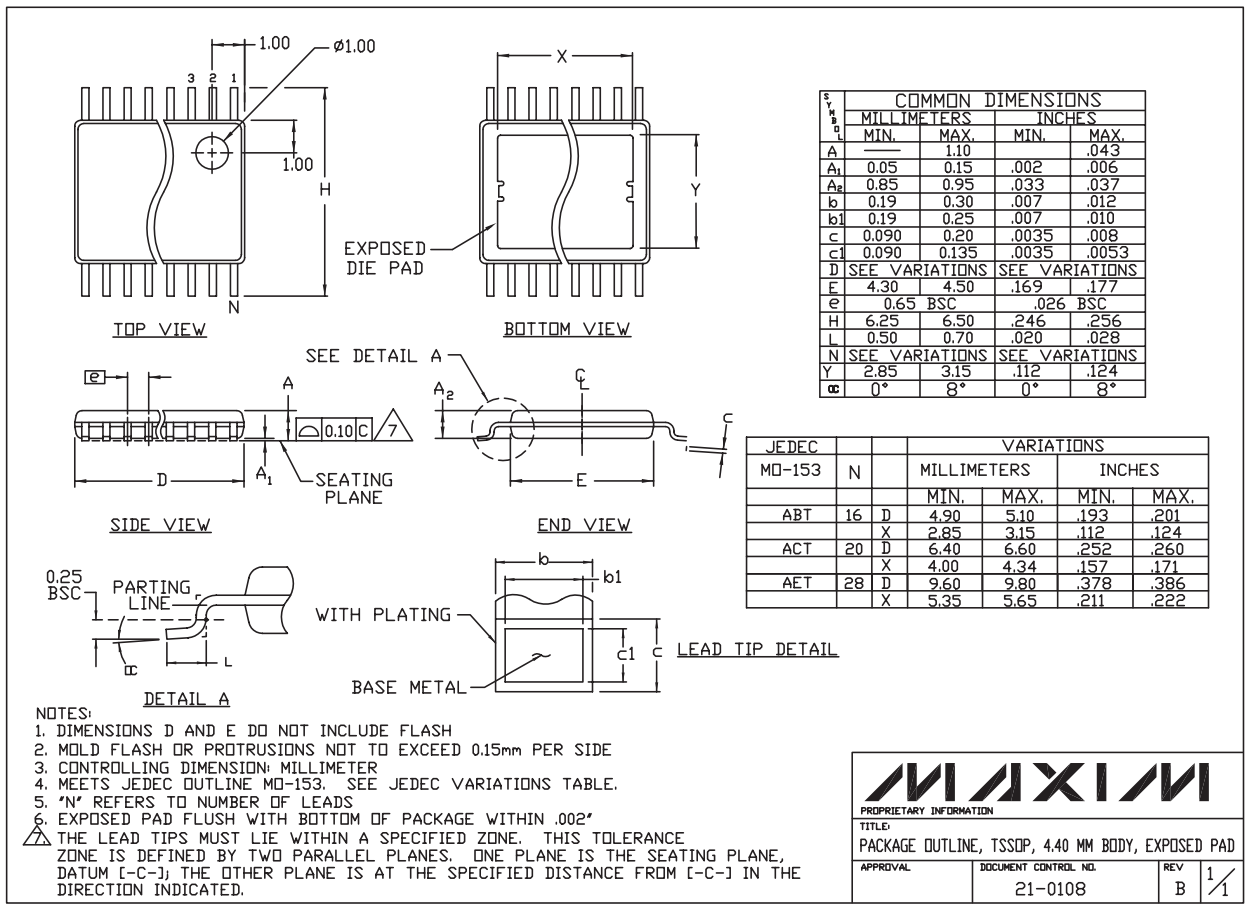
MAX9482 TRANSISTOR COUNT: 2607

PROCESS: Bipolar

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP, 4.0 EXP PADS.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	.112	.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
ABT	16	D	4.90	5.10	.193	.201
		X	2.85	3.15	.112	.124
ACT	20	D	6.40	6.60	.252	.260
		X	4.00	4.34	.157	.171
AET	28	D	9.60	9.80	.378	.386
		X	5.35	5.65	.211	.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002"
7. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY, EXPOSED PAD

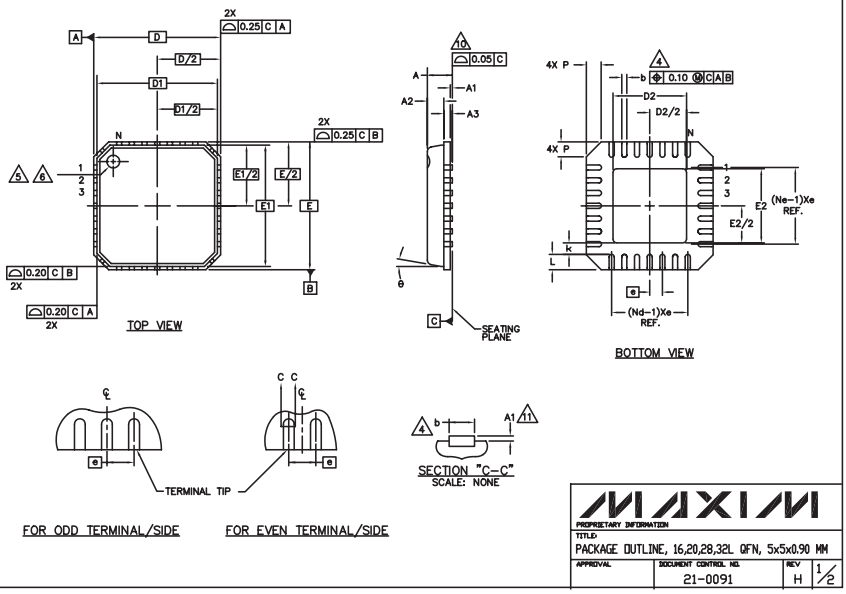
APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0108	B	1/1

Low-Power, Low-Distortion, Central-Office ADSL Drivers and Integrated Drivers/Receivers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

32L QFN.EPS



PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0091	H	1/2

COMMON DIMENSIONS												
PKG	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.28	0.33	0.40	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
D1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.35	0.55	0.75	0.35	0.55	0.75	0.35	0.55	0.75	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
θ	0°		12°	0°		12°	0°		12°	0°		12°

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1655-3	2.95	3.10	3.25	2.95	3.10	3.25
G2055-1	2.55	2.70	2.85	2.55	2.70	2.85
G2055-2	2.95	3.10	3.25	2.95	3.10	3.25
G2855-1	2.55	2.70	2.85	2.55	2.70	2.85
G2855-2	2.95	3.10	3.25	2.95	3.10	3.25
G3255-1	2.95	3.10	3.25	2.95	3.10	3.25

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0091	H	2/2