19-2220; Rev 0; 10/01

EVALUATION KIT AVAILABLE

MAXIM

1:5 Differential LVPECL/LVECL/HSTL Clock and Data Driver

MAX9315

General Description

The MAX9315 low-skew, 1-to-5 differential driver is designed for clock and data distribution. This device allows selection between two inputs. The selected input is reproduced at five differential outputs. The differential inputs can be adapted to accept a single-ended input by connecting the on-chip V_{BB} supply to one input as a reference voltage.

The MAX9315 features low output-to-output skew (20ps), making it ideal for clock and data distribution across a backplane or a board. For interfacing to differential HSTL and LVPECL signals, this device operates over a +2.375V to +3.8V supply range, allowing high-performance clock or data distribution in systems with a nominal +2.5V or +3.3V supply. For differential LVECL operation, this device operates with a -2.375V to -3.8V supply.

The MAX9315 is offered in a space-saving 20-pin TSSOP package.

Features

- ♦ +2.375V to +3.8V Supply for Differential HSTL/LVPECL Operation
- ♦ -2.375V to -3.8V Supply for Differential LVECL Operation
- ♦ Two Selectable Differential Inputs
- ♦ Synchronous Output Enable/Disable
- ♦ 20ps Output-to-Output Skew
- ♦ 360ps Propagation Delay
- ♦ Guaranteed 400mV Differential Output at 1.5GHz
- ♦ On-Chip Reference for Single-Ended Inputs
- ♦ Input Biased Low when Left Open
- ♦ Pin Compatible with MC100LVEP14

Applications

Precision Clock Distribution

Low-Jitter Data Repeater

Data and Clock Driver and Buffer

Central Office Backplane Clock Distribution

DSLAM Backplane

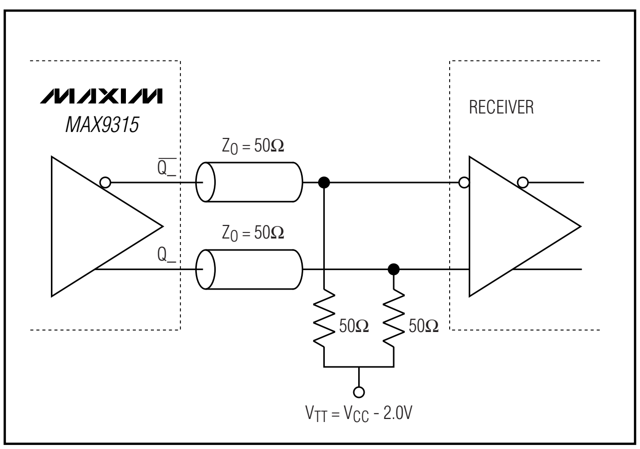
Base Station

ATE

Ordering Information

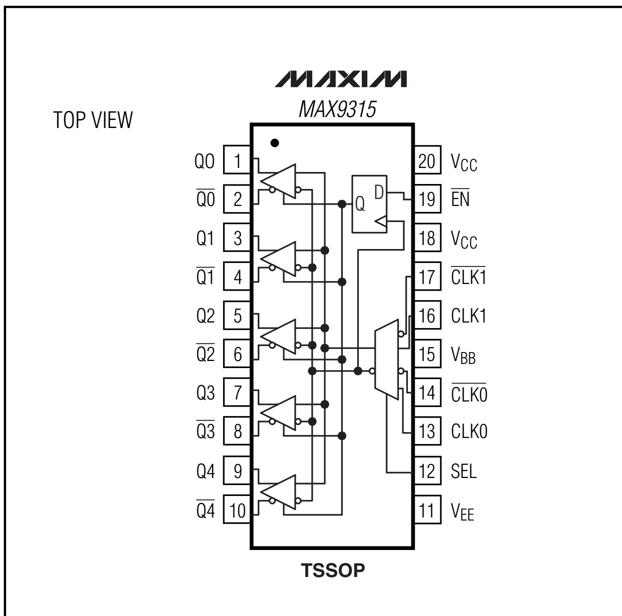
PART	TEMP. RANGE	PIN-PACKAGE
MAX9315EUP	-40°C to +85°C	20 TSSOP

Typical Application Circuit



Functional Diagram appears at end of data sheet.

Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

1:5 Differential LVPECL/LVECL/HSTL Clock and Data Driver

ABSOLUTE MAXIMUM RATINGS

V_{CC} - V_{EE} 4.1V
Inputs (CLK_, $\overline{\text{CLK}}$_, SEL, $\overline{\text{EN}}$)
to V_{EE} ....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
CLK_ to $\overline{\text{CLK}}$_ ....±3.0V
Continuous Output Current 50mA
Surge Output Current..100mA
V_{BB} Sink/Source Current ....±0.65mA
Continuous Power Dissipation (T_A = +70°C)
Single-Layer PC Board
20-Pin TSSOP (derate 7.69mW/°C above +70°C) 615mW
Multilayer PC Board
20-Pin TSSOP (derate 10.9mW/°C above +70°C) 879mW
Junction-to-Ambient Thermal Resistance in Still Air
Single-Layer PC Board
20-Pin TSSOP ....+130°C/W
Multilayer PC Board
20-Pin TSSOP ....+91°C/W
Junction-to-Ambient Thermal Resistance with 500LFPM
Airflow Single-Layer PC Board
20-Pin TSSOP ....+9.6°C/W
Junction-to-Case Thermal Resistance
20-Pin TSSOP ....+20°C/W
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
ESD Protection
Human Body Model (Inputs and Outputs) ....≥2kV
Soldering Temperature (10s)..+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = 2.375V to 3.8V, outputs loaded with 50Ω ±1% to V_{CC} - 2V, SEL = high or low, $\overline{\text{EN}}$ = low, unless otherwise noted. Typical values are at V_{CC} - V_{EE} = +3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SINGLE-ENDED INPUTS (SEL, $\overline{\text{EN}}$)												
Input High Voltage	V_{IH}		V_{CC} - 1.225		V_{CC}	V_{CC} - 1.225		V_{CC}	V_{CC} - 1.225		V_{CC}	V
Input Low Voltage	V_{IL}		V_{EE}		V_{CC} - 1.625	V_{EE}		V_{CC} - 1.625	V_{EE}		V_{CC} - 1.625	V
Input Current	I_{IN}	$V_{IH(MAX)}$, $V_{IL(MIN)}$	-500		500	-500		500	-500		500	µA
DIFFERENTIAL INPUTS (CLK_, $\overline{\text{CLK}}$_)												
Single-Ended Input High Voltage (Note 4)	V_{IH}	V_{BB} connected to $\overline{\text{CLK}}$_, Figure 1	V_{CC} - 1.225		V_{CC}	V_{CC} - 1.225		V_{CC}	V_{CC} - 1.225		V_{CC}	V
Single-Ended Input Low Voltage (Note 4)	V_{IL}	V_{BB} connected to $\overline{\text{CLK}}$_, Figure 1	V_{EE}		V_{CC} - 1.625	V_{EE}		V_{CC} - 1.625	V_{EE}		V_{CC} - 1.625	V
High Voltage of Differential Input	V_{IHD}		V_{EE} + 1.2		V_{CC}	V_{EE} + 1.2		V_{CC}	V_{EE} + 1.2		V_{CC}	V
Low Voltage of Differential Input	V_{ILD}		V_{EE}		V_{CC} - 0.1	V_{EE}		V_{CC} - 0.1	V_{EE}		V_{CC} - 0.1	V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} - V_{EE} = 2.375V to 3.8V, outputs loaded with 50Ω ±1% to V_{CC} - 2V, SEL = high or low, $\overline{EN}$ = low, unless otherwise noted. Typical values are at V_{CC} - V_{EE} = +3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Differential Input Voltage	V_{IHD} - V_{ILD}	For (V_{CC} - V_{EE}) < +3.0V	0.1		V_{CC} - V_{EE}	0.1		V_{CC} - V_{EE}	0.1		V_{CC} - V_{EE}	V
		For (V_{CC} - V_{EE}) ≥ +3.0V	0.1		3.0	0.1		3.0	0.1		3.0	
Input Current	I_{IN}	V_{IH}, V_{IL}, V_{IHD}, V_{ILD}	-150		150	-150		150	-150		150	µA
OUTPUTS (Q_, $\overline{Q}$_)												
Single-Ended Output High Voltage	V_{OH}	Figure 1	V_{CC} - 1.145		V_{CC} - 0.865	V_{CC} - 1.145		V_{CC} - 0.865	V_{CC} - 1.145		V_{CC} - 0.865	V
Single-Ended Output Low Voltage	V_{OL}	Figure 1	V_{CC} - 1.945		V_{CC} - 1.695	V_{CC} - 1.945		V_{CC} - 1.695	V_{CC} - 1.945		V_{CC} - 1.695	V
Differential Output Voltage	V_{OH} - V_{OL}	Figure 1	550		910	550		910	550		910	mV
REFERENCE												
Reference Voltage Output (Note 5)	V_{BB}	I_{BB} = ±0.5mA	V_{CC} - 1.525		V_{CC} - 1.325	V_{CC} - 1.525		V_{CC} - 1.325	V_{CC} - 1.525		V_{CC} - 1.325	V
SUPPLY												
Supply Current (Note 6)	I_{EE}			41	48		45	55		49	65	mA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = 2.375V to 3.8V, outputs loaded with 50Ω ±1% to V_{CC} - 2V, input frequency = 1.5GHz, input transition time = 125ps (20% to 80%), SEL = high or low, $\overline{EN}$ = low, V_{IHD} = V_{EE} + 1.2V to V_{CC}, V_{ILD} = V_{EE} to V_{CC} - 0.15V, V_{IHD} - V_{ILD} = 0.15V to the smaller of 3V or V_{CC} - V_{EE}, unless otherwise noted. Typical values are at V_{CC} - V_{EE} = +3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V.) (Notes 1, 7)

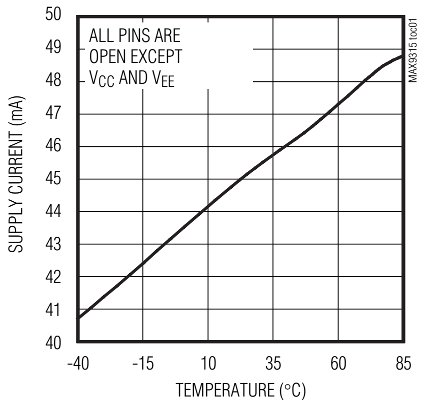
PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	ps
Differential Input-to-Output Delay	t_{PLHD}, t_{PHLD}	Figure 2	290		400	310		440	300		520	ps
Output-to-Output Skew (Note 8)	t_{SKOO}			5	30		20	40		20	50	ps
Part-to-Part Skew (Note 9)	t_{SKPP}				110			130			220	ps
Added Random Jitter (Note 10)	t_{RJ}	f_{IN} = 1.5GHz clock		0.8	1.2		0.8	1.2		0.8	1.2	ps (RMS)
Added Deterministic Jitter (Note 10)	t_{DJ}	1.5Gbps $2E^{23}$-1 PRBS pattern		50	70		50	70		50	70	ps (p-p)
Switching Frequency	f_{MAX}	(V_{OH} - V_{OL}) ≥ 400mV, Figure 2	1.5			1.5			1.5			GHz
Output Rise/Fall Time (20% to 80%)	t_R, t_F	Figure 2	80		120	90		130	90		145	ps

Note 1: Measurements are made with the device in thermal equilibrium.
Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.
Note 3: DC parameters production tested at T_A = +25°C and guaranteed by design over the full operating temperature range.
Note 4: Single-ended input operation using V_{BB} is limited to V_{CC} - V_{EE} = 3.0V to 3.8V.
Note 5: Use V_{BB} only for inputs that are on the same device as the V_{BB} reference.
Note 6: All pins open except V_{CC} and V_{EE}.
Note 7: Guaranteed by design and characterization. Limits are set at ±6 sigma.
Note 8: Measured between outputs of the same part at the signal crossing points for a same-edge transition.
Note 9: Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.
Note 10: Device jitter added to the input signal.

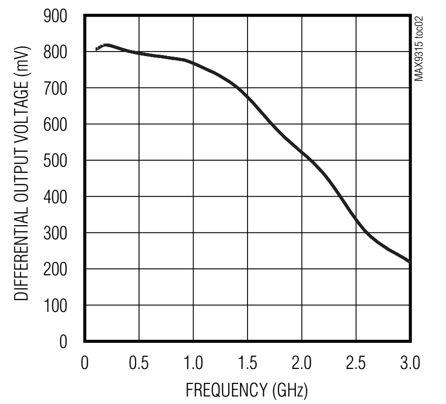
Typical Operating Characteristics

(V_{CC} = +3.3V, V_{EE} = 0, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.15V, input transition time = 125ps (20% to 80%), f_{IN} = 2GHz, outputs loaded with 50Ω to V_{CC} - 2V, T_A = +25°C, unless otherwise noted.)

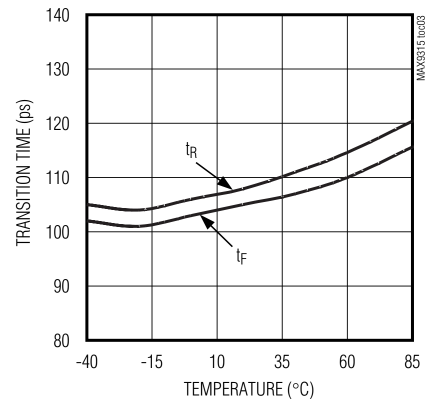
SUPPLY CURRENT vs. TEMPERATURE



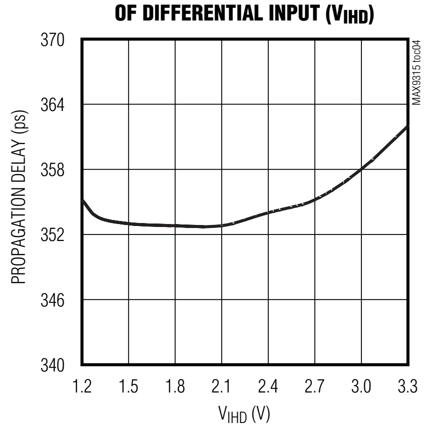
DIFFERENTIAL OUTPUT VOLTAGE (V_{OH} - V_{OL}) vs. FREQUENCY



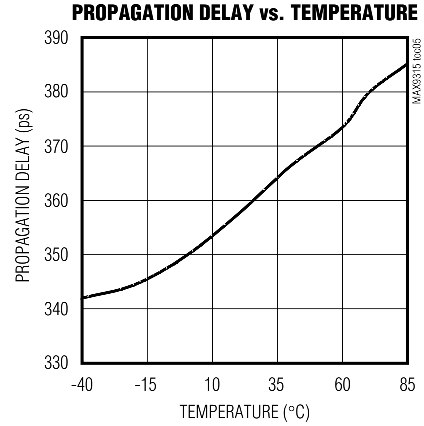
TRANSITION TIME vs. TEMPERATURE



PROPAGATION DELAY vs. HIGH VOLTAGE OF DIFFERENTIAL INPUT (V_{IHD})



PROPAGATION DELAY vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	Q0	Noninverting Q0 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
2	$\overline{Q0}$	Inverting Q0 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
3	Q1	Noninverting Q1 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
4	$\overline{Q1}$	Inverting Q1 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
5	Q2	Noninverting Q2 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
6	$\overline{Q2}$	Inverting Q2 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
7	Q3	Noninverting Q3 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
8	$\overline{Q3}$	Inverting Q3 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
9	Q4	Noninverting Q4 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
10	$\overline{Q4}$	Inverting Q4 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
11	V_{EE}	Negative Supply Voltage
12	SEL	Clock Select Input (Single Ended). Drive low to select the CLK0, $\overline{CLK0}$ input. Drive high to select the CLK1, $\overline{CLK1}$ input. The SEL threshold is equal to V_{BB}. Internal 60kΩ pulldown to V_{EE}.
13	CLK0	Noninverting Differential Clock Input 0. Internal 75kΩ pulldown to V_{EE}.
14	$\overline{CLK0}$	Inverting Differential Clock Input 0. Internal 75kΩ pullup to V_{CC} and 75kΩ pulldown to V_{EE}.
15	V_{BB}	Reference Output Voltage. Connect to the inverting or noninverting clock input to provide a reference for single-ended operation. When used, bypass with a 0.01µF ceramic capacitor to V_{CC}; otherwise, leave open.
16	CLK1	Noninverting Differential Clock Input 1. Internal 75kΩ pulldown to V_{EE}.
17	$\overline{CLK1}$	Inverting Differential Clock Input 1. Internal 75kΩ pullup to V_{CC} and 75kΩ pulldown to V_{EE}.
18, 20	V_{CC}	Positive Supply Voltage. Bypass V_{CC} to V_{EE} with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
19	$\overline{EN}$	Output Enable Input. Outputs are synchronously enabled on the falling edge of the selected clock input when $\overline{EN}$ is low. Outputs are synchronously driven low on the falling edge of the selected clock input when $\overline{EN}$ is high. Internal 60kΩ pulldown to V_{EE}.

Detailed Description

The MAX9315 is a low-skew, 1-to-5 differential driver designed for clock or data distribution. A 2-to-1 MUX selects one of the two differential clock inputs, CLK0, $\overline{CLK0}$ or CLK1, $\overline{CLK1}$. The MUX is switched by the single-ended SEL input. A logic low selects the CLK0, $\overline{CLK0}$ input and a logic high selects the $\overline{CLK1}$, CLK1 input. The SEL logic threshold is set by the internal voltage reference V_{BB}. SEL can be driven to V_{CC} and V_{EE} or by a single-ended LVPECL/LVECL signal. The selected input is reproduced at five differential outputs.

Synchronous Enable

The MAX9315 is synchronously enabled and disabled with outputs in the low state to eliminate shortened clock pulses. $\overline{EN}$ is connected to the input of an edge-triggered D flip-flop. After power-up, drive $\overline{EN}$ low and toggle the selected clock input to enable the outputs. The outputs are enabled on the falling edge of the selected clock input after $\overline{EN}$ goes low. The outputs are set to a low state on the falling edge of the selected clock input after $\overline{EN}$ goes high. The threshold for $\overline{EN}$ is equal to V_{BB}.

Supply

For interfacing to differential HSTL and LVPECL signals, the V_{CC} range is from +2.375V to +3.8V (with V_{EE} grounded), allowing high-performance clock or data distribution in systems with a nominal +2.5V or +3.3V supply. For interfacing to differential LVECL, the V_{EE} range is -2.375V to -3.8V (with V_{CC} grounded). Output levels are referenced to V_{CC} and are considered LVPECL or LVECL, depending on the level of the V_{CC} supply. With V_{CC} connected to a positive supply and

V_{EE} connected to ground, the outputs are LVPECL. The outputs are LVECL when V_{CC} is connected to ground and V_{EE} is connected to a negative supply.

Input Bias Resistors

When the inputs are open, the internal bias resistors set the inputs to low state. The inverting inputs ($\overline{CLK0}$ and $\overline{CLK1}$) are each biased with a 75kΩ pullup to V_{CC} and a 75kΩ pulldown to V_{EE}. The noninverting inputs (CLK0 and CLK1) are each biased with a 75kΩ pulldown to V_{EE}. Similarly, the single-ended $\overline{EN}$ and SEL inputs are each biased low with a 60kΩ pulldown to V_{EE}.

Differential Clock Input Limits

The maximum magnitude of the differential signal applied to the clock input is 3.0V or V_{CC} - V_{EE}, whichever is less. This limit also applies to the difference between any reference voltage input and a single-ended input. Specifications for the high and low voltages of a differential input (V_{IHD} and V_{ILD}) and the differential input voltage (V_{IHD} - V_{ILD}) apply simultaneously.

Single-Ended Clock Input and V_{BB}

The differential clock inputs can be configured to accept single-ended inputs. This is accomplished by connecting the on-chip reference voltage, V_{BB}, to the inverting or noninverting input of a differential input as a reference. For example, the differential CLK0, $\overline{CLK0}$ input is converted to a noninverting, single-ended input by connecting V_{BB} to $\overline{CLK0}$ and connecting the single-ended input signal to CLK0. Similarly, an inverting configuration is obtained by connecting V_{BB} to CLK0 and connecting the single-ended input to $\overline{CLK0}$. With a differential input configured as single ended (using V_{BB}), the single-ended input can be driven to V_{CC} and V_{EE} or with a single-ended LVPECL/LVECL signal. Note that single-ended input must be at least V_{BB} ±100mV or a differential input of at least 100mV to switch the outputs to the V_{OH} and V_{OL} levels specified in the *DC Electrical Characteristics* table.

If V_{BB} is used, the supply must be in the V_{CC} - V_{EE} = +2.725V to +3.8V range because one of the inputs must be V_{EE} + 1.2V or higher for proper input stage operation. V_{BB} must be at least V_{EE} + 1.2V because it becomes the high-level input when the other (single-ended) input swings below it. Therefore, minimum V_{BB} = V_{EE} + 1.2V. The minimum V_{BB} output of the MAX9315 is V_{CC} - 1.525V. Substituting the minimum V_{BB} output into V_{BB} = V_{EE} + 1.2V results in a minimum supply of +2.725V. Rounding up to standard supplies gives the single-ended operating supply range of V_{CC} - V_{EE} = +3.0V to +3.8V.

When using the V_{BB} reference output, bypass it with a 0.01µF ceramic capacitor to V_{CC}. If the V_{BB} reference is not used, leave it open. The V_{BB} reference can source or sink 0.5mA, which is sufficient to drive two inputs. Use V_{BB} only for inputs that are on the same device as the V_{BB} reference.

Applications Information

Supply Bypassing

Bypass V_{CC} to V_{EE} with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors in parallel as close to the device as possible, with the 0.01µF capacitor closest to the device. Use multiple parallel vias to minimize parasitic inductance. When using the V_{BB} reference output, bypass it with a 0.01µF ceramic capacitor to V_{CC} (if the V_{BB} reference is not used, it can be left open).

Controlled-Impedance Traces

Input and output trace characteristics affect the performance of the MAX9315. Connect high-frequency input and output signals with 50Ω characteristic impedance traces. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through cables and connectors. Reduce skew within a differential pair by matching the electrical length of the traces.

Output Termination

Terminate outputs with 50Ω to V_{CC} - 2V or use an equivalent Thevenin termination. When a single-ended signal is taken from a differential output, terminate both outputs. For example, if Q0 is used as a single-ended output, terminate both Q0 and $\overline{Q0}$.

Chip Information

TRANSISTOR COUNT: 616

PROCESS: Bipolar

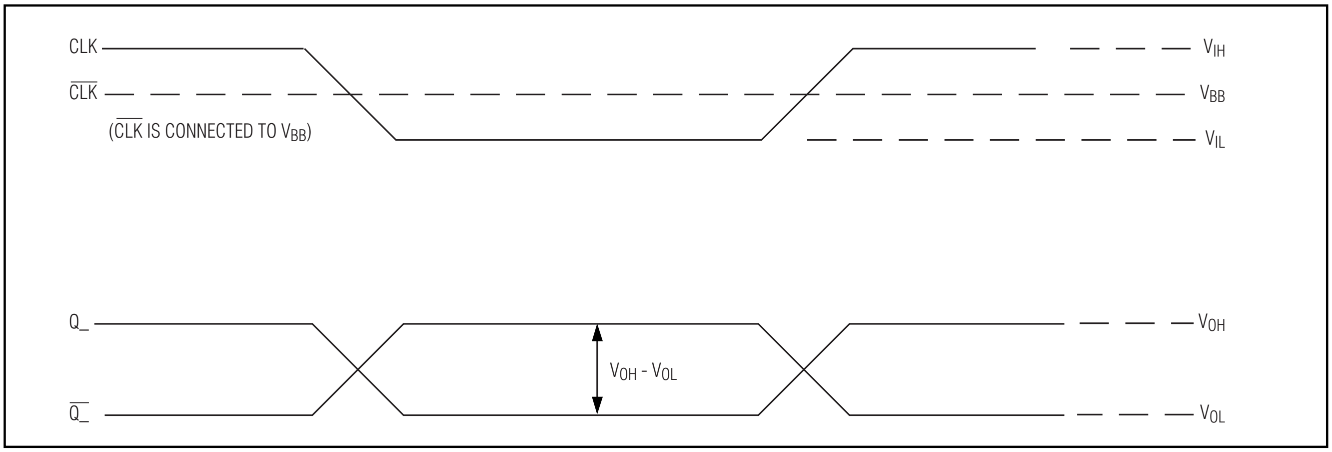


Figure 1. MAX9315 Switching Characteristics with Single-Ended Input

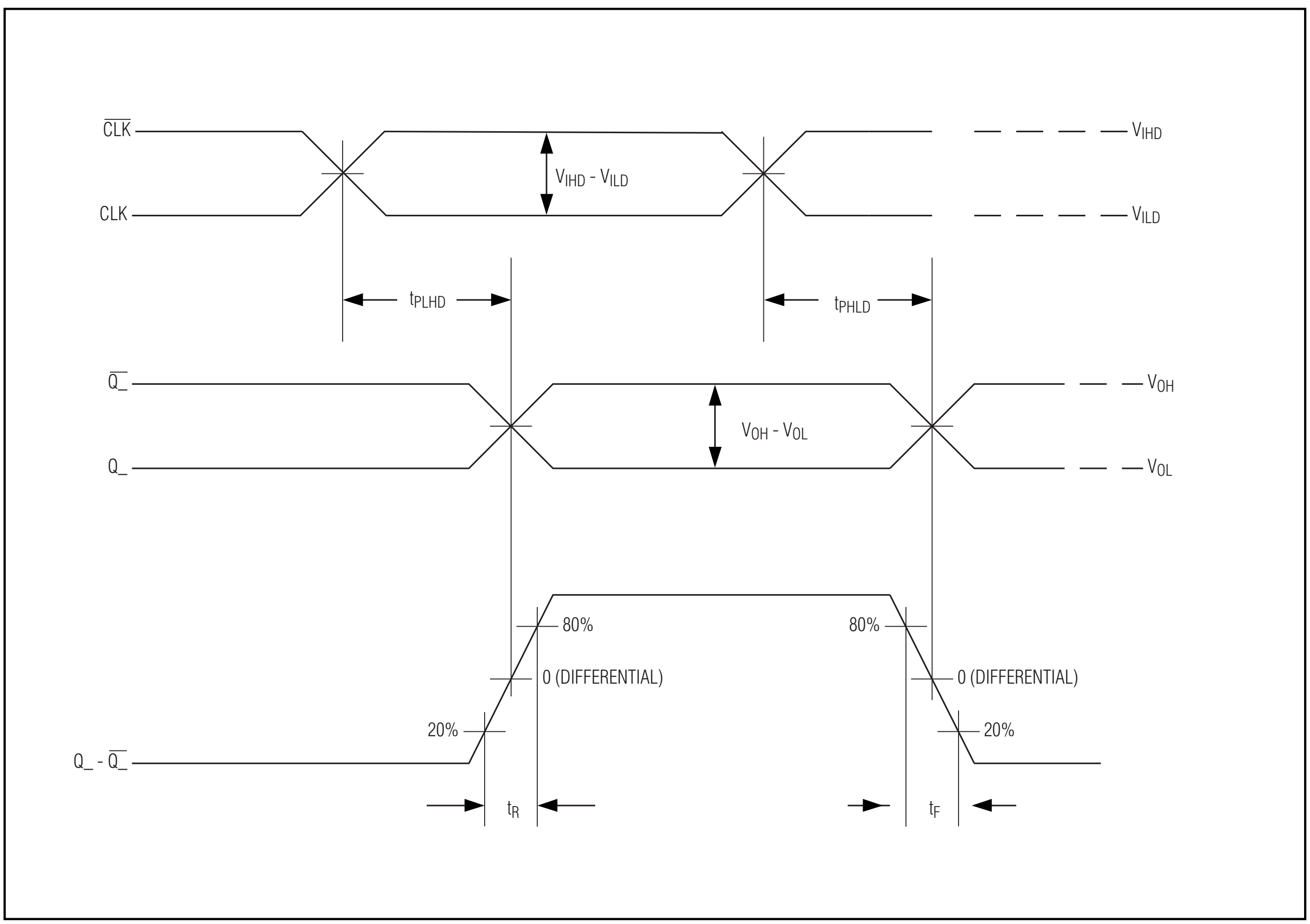


Figure 2. MAX9315 Timing Diagram

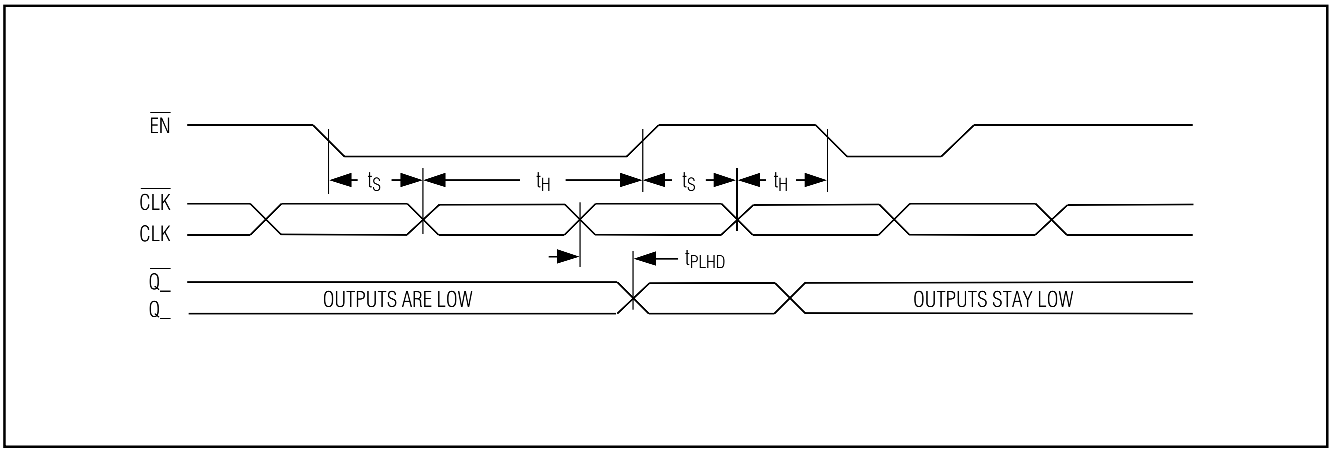
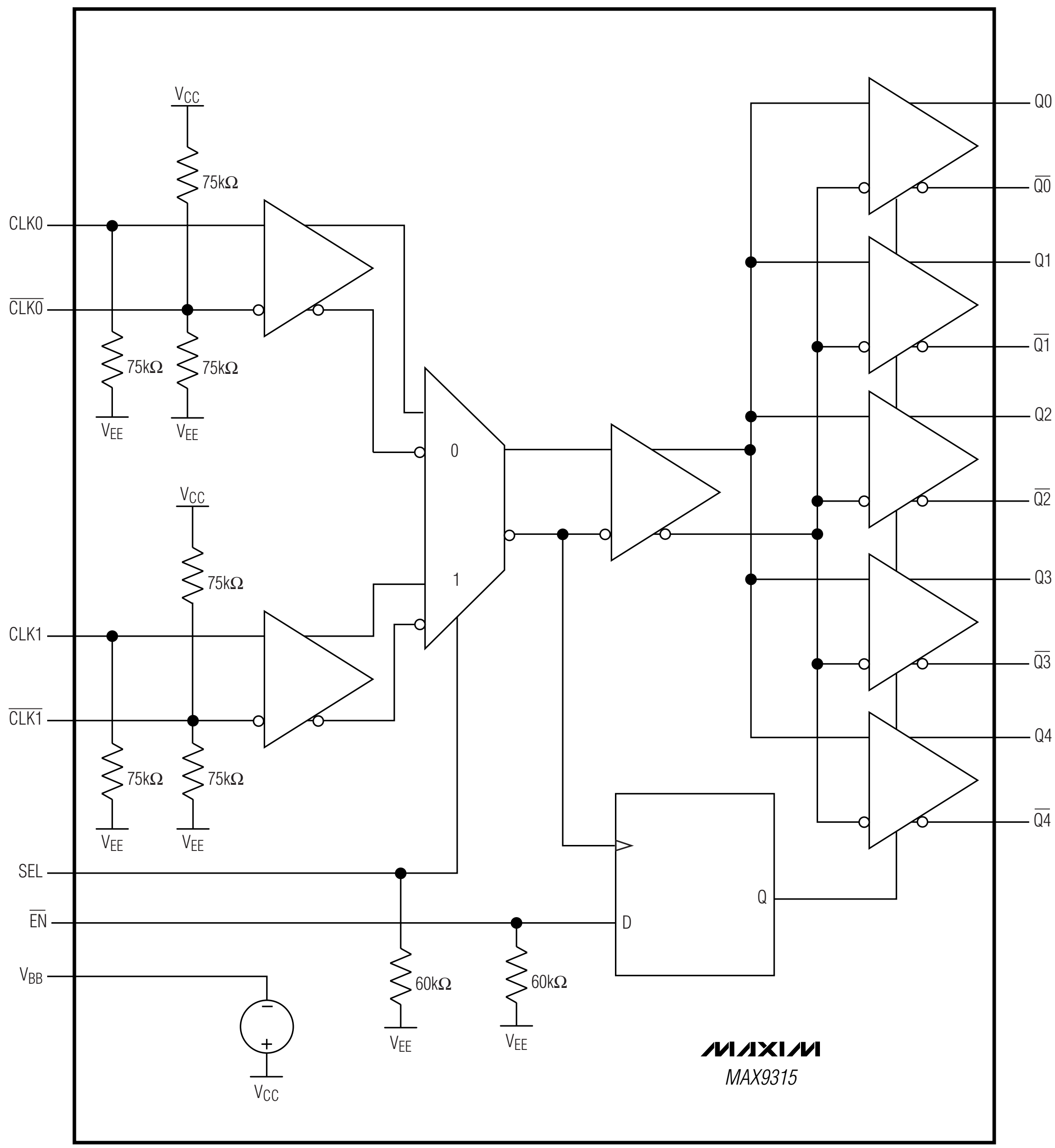


Figure 3. MAX9315 $\overline{EN}$ Timing Diagram

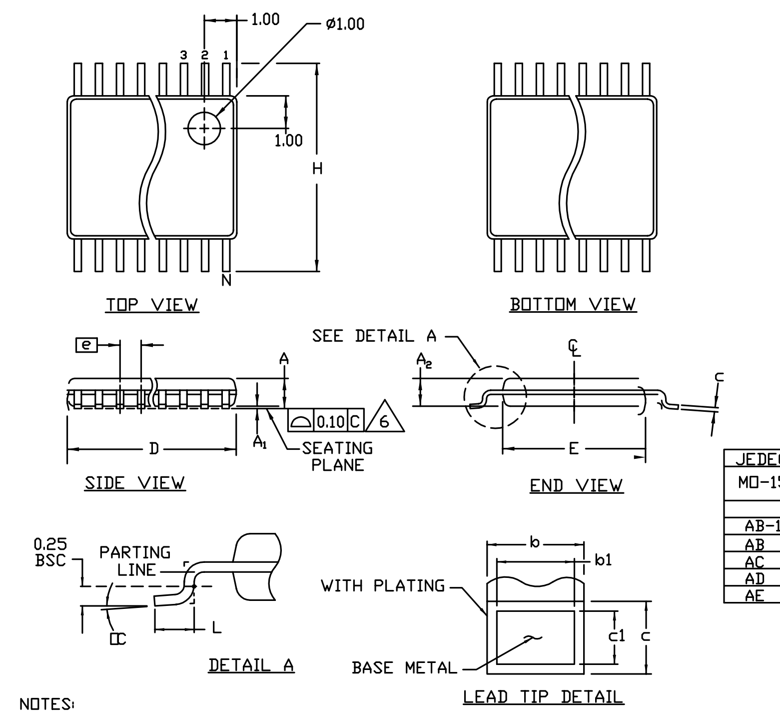
1:5 Differential LVPECL/LVECL/HSTL Clock and Data Driver

Functional Diagram



Package Information

TSSOP,NO PADS.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10		.043
A1	0.05	0.15	.002	.006
A2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY
APPROVAL | DOCUMENT CONTROL NO. 21-0066 | REV E | 1/1