Ordering number : ENN7028

Bi-CMOS IC

LV2210V

Basic Data Communication Receiver IC

Overview

The LV2210V is a basic data communication receiver IC that integrates on a single chip a frequency synthesizer that can be controlled by serial data, a downconverter mixer, a narrow-band FM IF system, and a data shaper circuit.

Features

- Operating frequency range: 7 to 50 MHz
- Operating supply voltage range: 2.7 to 5.5 V
- Miniature package: SSOP24 (275 mil)

Functions

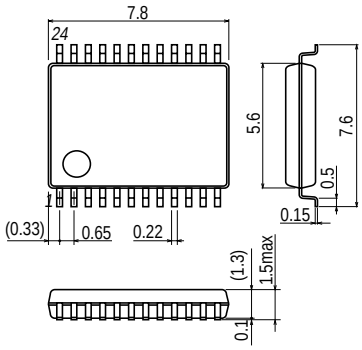
- PLL synthesizer
- Downconverter mixer
- VCO transistor
- IF amplifier, limiter, and RSSI
- FM detector (quadrature)
- Data shaper

Package Dimensions

unit: mm

3175B-SSOP24 (275 mil)

[LV2210V]



SANYO: SSOP-24 (275 mil)

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		6.0	V
Maximum input voltage	Vin max		V_{CC} + 0.3	V
Maximum output voltage	Vout max		V_{CC} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	180	mW
Operating temperature	Topr		–20 to +70	°C
Storage temperature	Tstg		–40 to +125	°C

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32502RM (OT) No. 7028-1/15

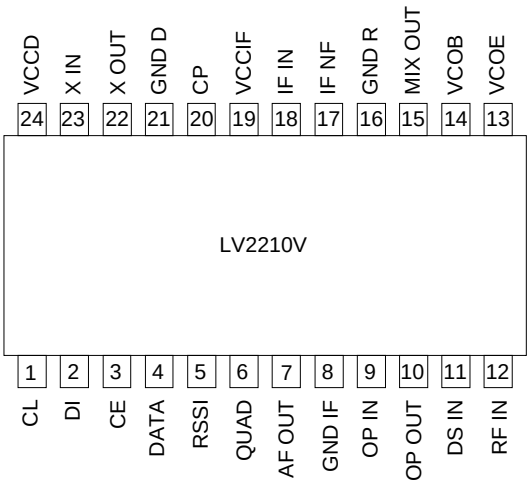
Allowable Operating Ranges at Ta = –20 to +70°C

Parameter	Symbol	Pins	Ratings			Unit
			min	typ	max	
Supply voltage	V_{CC}	VCCIF, VCCD	2.7	5	5.5	V
High-level input voltage	V_{IH}	CE, CL, DI	$V_{CC} \times 0.7$		5.5	V
Low-level input voltage	V_{IL}	CE, CL, DI	0		+0.6	V
XIN operating frequency	Fxin	XIN, XOUT	5		20	MHz
XIN input level	Vxin	XIN, XOUT	–12		0	dBm
PLL operating frequency	Fin	PLL section	7		50	MHz
PLL input level	Vin	PLL section	–12		0	dBm

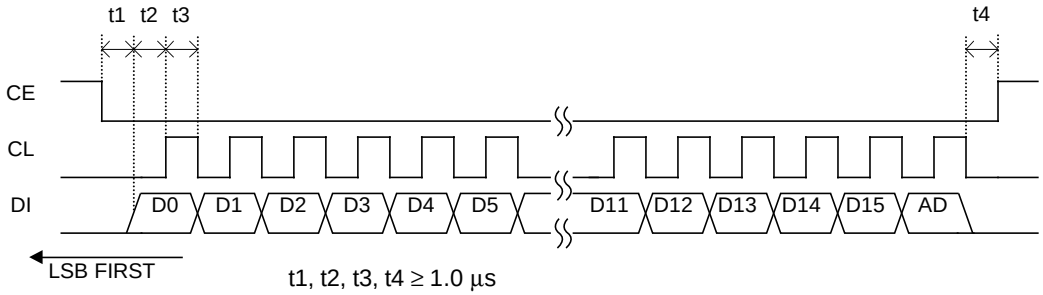
Electrical Characteristics at Ta = 25°C, VCCIF = VCCD = 5 V, Frf = 27 MHz, Flo = 26.545 MHz, Fif = 455 KHz, Fmod = 1 KHz, Fdev = ±3 KHz

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CC}	VCCIF, VCCD		7.5	13	mA
CP output off leakage current	Icpoff	CP : Vo = 1.5 V, CP data “1”			100	nA
CP output current 1	Icp1	CP : Vo = 1.5 V, CP data “0”		±100		µA
CP output current 2	Icp2	CP : Vo = 1.5 V, CP data “1”		±400		µA
High-level input current	I_{IH}	CE, CL, DI : Vi = 3 V			5	µA
Low-level input current	I_{IL}	CE, CL, DI : Vi = 0 V			5	µA
Mixer operating input frequency	Fmix		7		50	MHz
Conversion gain	Gmix			25		dB
Intercept point	Iip3			–13		dBm
Mixer output impedance	Zomix			330		Ω
IF frequency	Fif			455		kHz
IF amplifier gain	Gif			105		dB
IF input impedance	Ziif			2		kΩ
RSSI output voltage 1	Vrssi1	Rfin : –90 dBm	0.3	0.5	0.75	V
RSSI output voltage 2	Vrssi2	Rfin : –50 dBm	1.1	1.4	1.75	V
Demodulator output	Vodet	Rfin : –30 dBm	150	190	240	mVrms
12 dB SINAD sensitivity	12SD			–100	–90	dBm
Total harmonic distortion	THD	Rfin : –30 dBm		2.0	3.0	%
Signal-to-noise ratio	S/N	Rfin : –30 dBm	40	50		dB
AM rejection ratio	AMR	AM 30% mod	30	40		dB
Data shaper duty ratio	DR	Opin : 1 kHz, 100 mVrms	45	50	55	%

Pin Assignment



Serial Data Timing



Control Data Format and Description

CONTROL DATA																AD
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	AD
R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	CP	SW	T2	T1	0
P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	*	*	1

BIT	DESCRIPTION
AD	Latch selection bit
T1, T2	Test bits. These bits must always be set to 0.
R0 to R11	Reference divider bits. R0 is the LSB. This is a binary value field.
P0 to P13	Programmable divider bits. P0 is the LSB. This is a binary value field.
CP	Charge pump current switching bit. 0: 100 µA, 1: 400 µA
SW	On/off switch for the reference voltage for the data shaper. 1: On, 0: Off

Reference divider divisor setting data

- The circuit consists of a fixed divide-by-two circuit and a 12-bit reference divider.
- A divisor, which is a multiple of 2 with a value of up to 8190, can be set by sending the reference divider data.
- The value of the divisor is determined as follows.

  Divisor $N = 2\,(R0 + R1 \times 2^{1} + R2 \times 2^{2} + R3 \times 2^{3} + \cdots\cdots + R11 \times 2^{11})$

Programmable divider divisor setting data

- The circuit consists of a 4-bit swallow counter and a 10-bit programmable counter.
- A divisor with a value in the range 240 to 16,383 can be set by sending the swallow counter and programmable counter data.
- The value of the divisor is determined as follows.

  Divisor $N = (16D + A)$

  $D = P4 + P5 \times 2^{1} + P6 \times 2^{2} + P7 \times 2^{3} + \cdots\cdots + P13 \times 2^{9}$

  $A = P0 + P1 \times 2^{1} + P2 \times 2^{2} + P3 \times 2^{3}$

PLL Divisor Setup Example

- The reference divider divisor is calculated as follows when a 12.8 MHz crystal element is used, the comparison frequency in the phase detector is 5 kHz, and the VCO oscillator frequency is 26.545 MHz.

  12.8 MHz ÷ 5 kHz = 2560 (divisor value)

  Since there is a fixed divide-by-two circuit, the required divisor is as follows.

  $2560 \times 1/2 = 1280$

  The value 1280 converted to binary (10100000000) is the reference divider setting data.

  The programmable divider divisor is calculated as follows.

  26.545 MHz ÷ 5 kHz = 5309 (divisor value)

  The value 5309 converted to binary (1010010111101) is the programmable divider setting data.

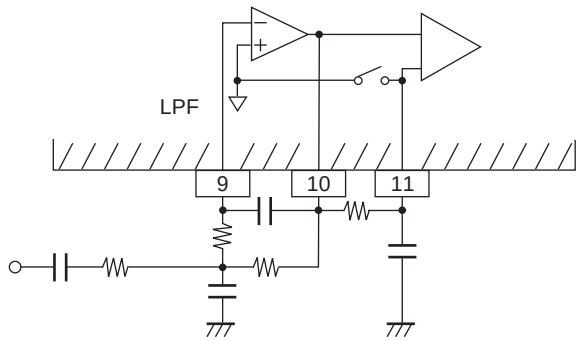
- The control data is set as follows

CONTROL DATA																AD
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	AD
0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0
1	0	1	1	1	1	0	1	0	0	1	0	1	0	0	0	1

(Charge pump current = 100 μA, Data shaper switch = on)

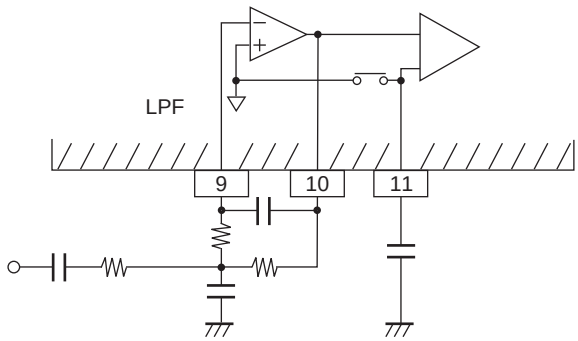
Low-Pass Filter and Data Shaper Application Examples

Example 1 (Switch: 0)



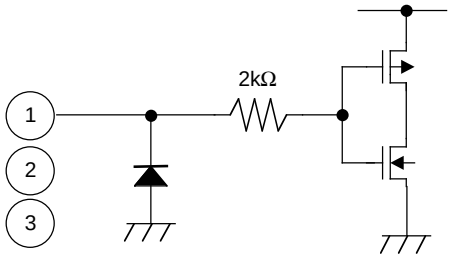
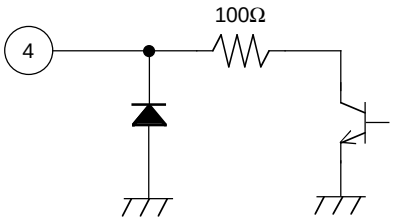
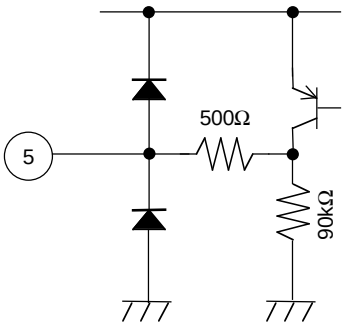
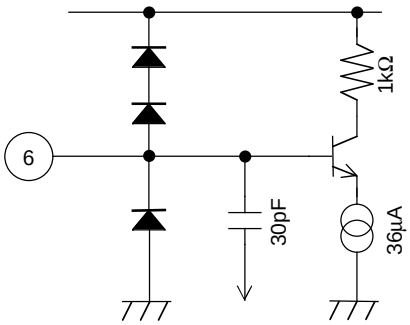
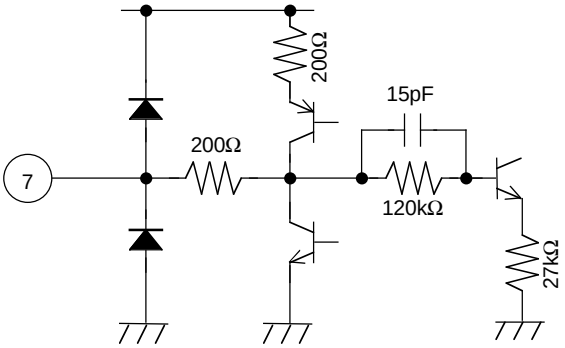
ILV00150

Example 2 (Switch: 1)



ILV00151

Pin Functions

Pin No.	Pin	Equivalent circuit	Notes
1 2 3	CL DI CE		Serial data input
4	DATA		Data shaper output
5	RSSI		RSSI output
6	QUAD		Quadrature coil/discriminator connection
7	AFOUT		AF signal output

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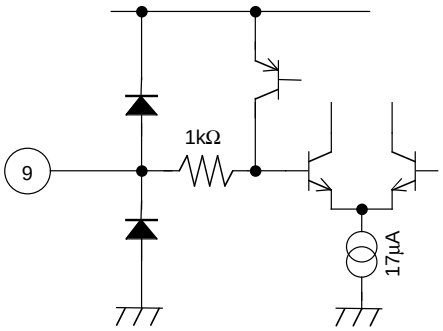
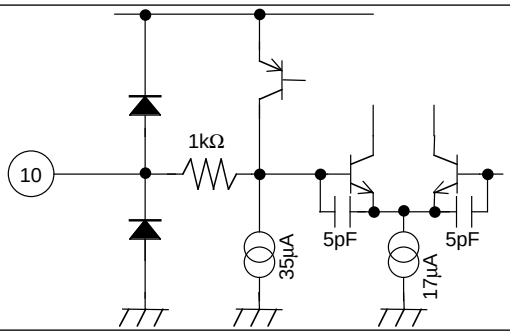
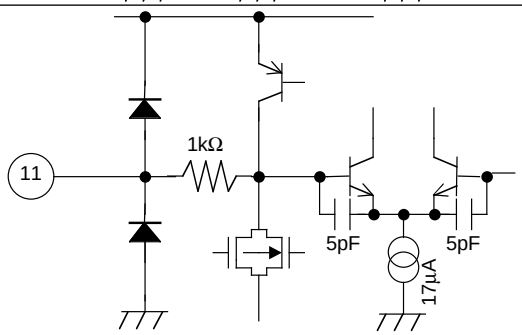
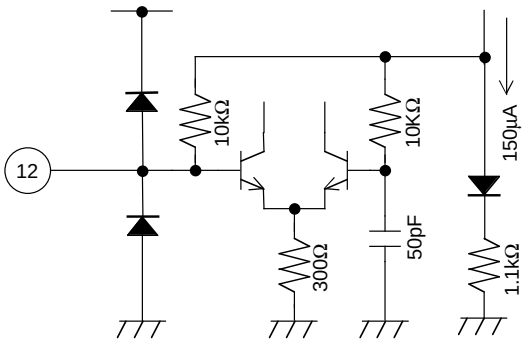
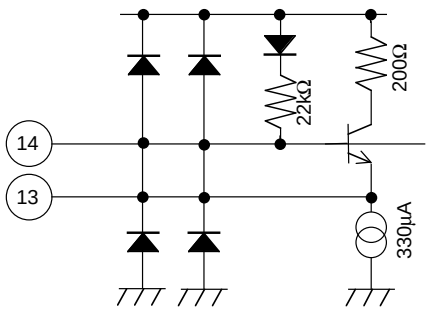
Pin No.	Pin	Equivalent circuit	Notes
8	GNDIF		IF ground
9	OPIN		Low-pass filter input
10	OPOUT		Low-pass filter output
11	DSIN		Data shaper input
12	RFIN		Mixer input
13 14	VCOE VCOB		VCO circuit

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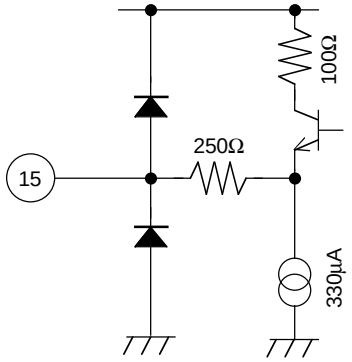
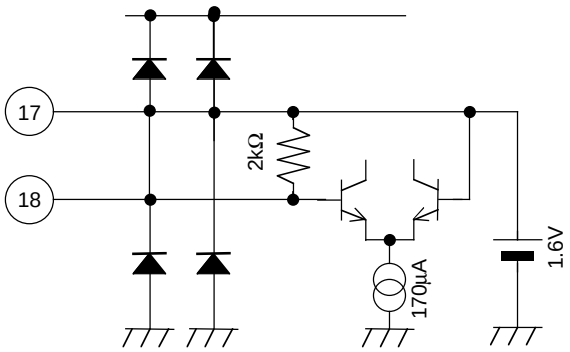
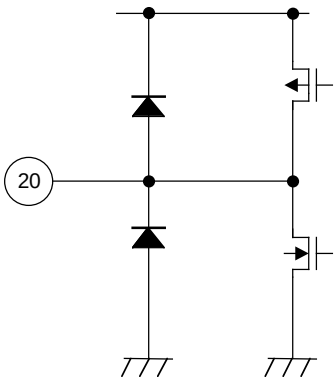
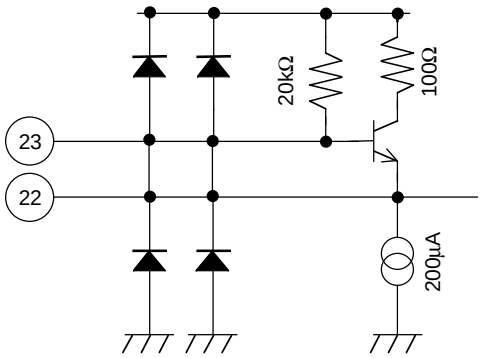
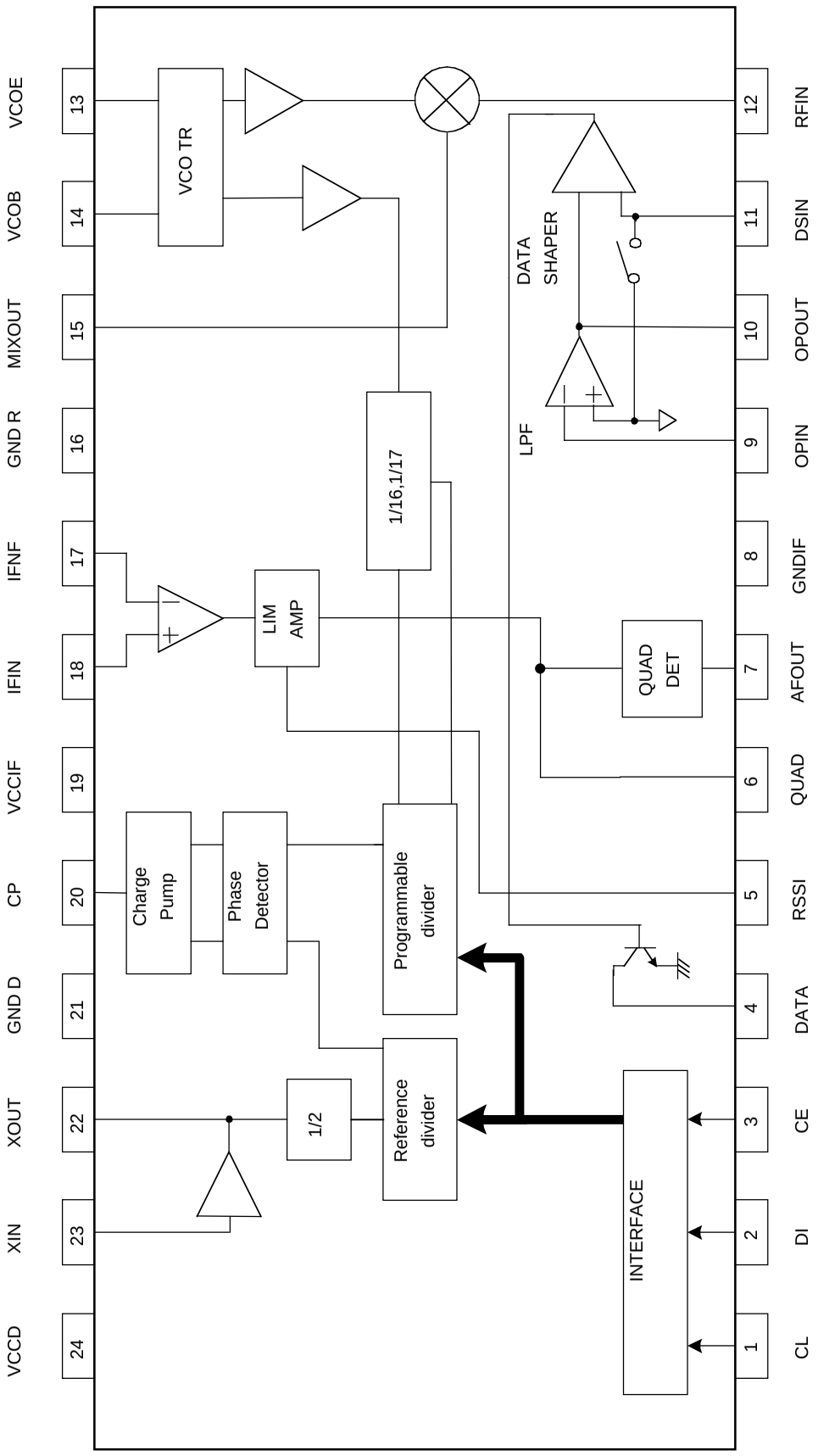
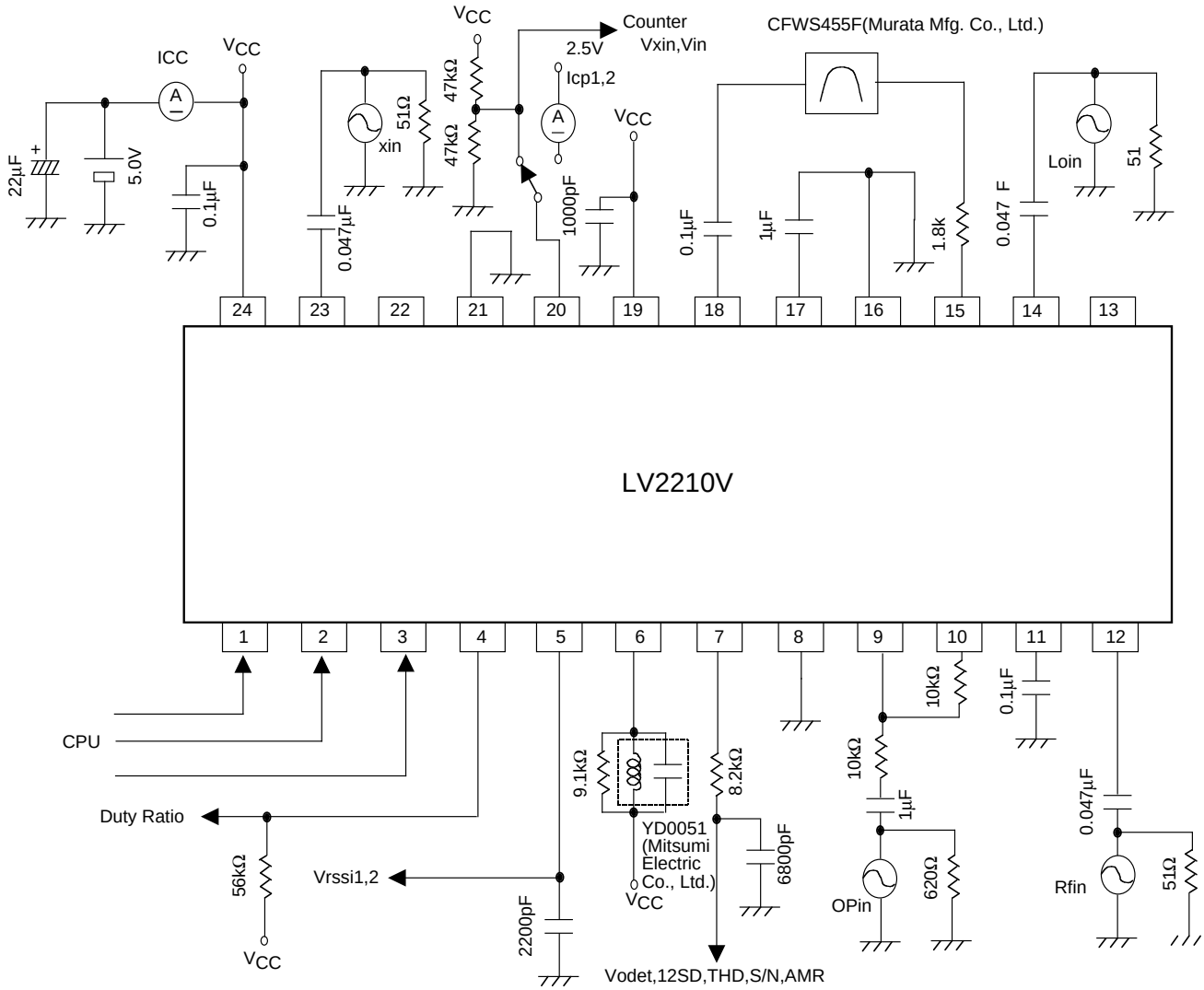
Pin No.	Pin	Equivalent circuit	Notes
15	MIXOUT		Mixer output
16	GNDR		RF ground
17 18	IFNF IFIN		IF input
19	VCCIF		IF VCC
20	CP		Charge pump output
21	GNDD		Digital system ground
22 23	XOUT XIN		Crystal oscillator circuit
24	VCCD		Digital system VCC

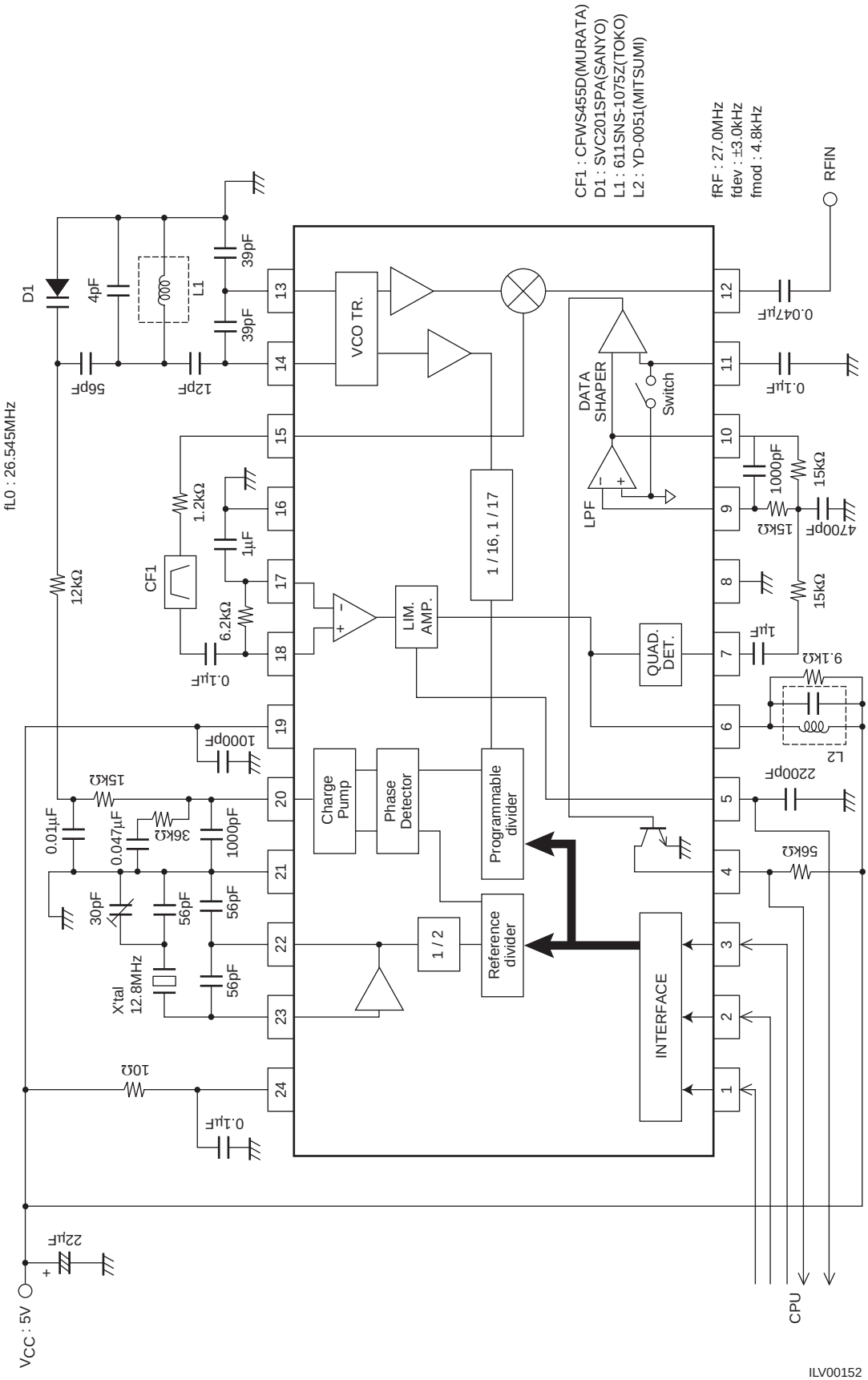
Block Diagram



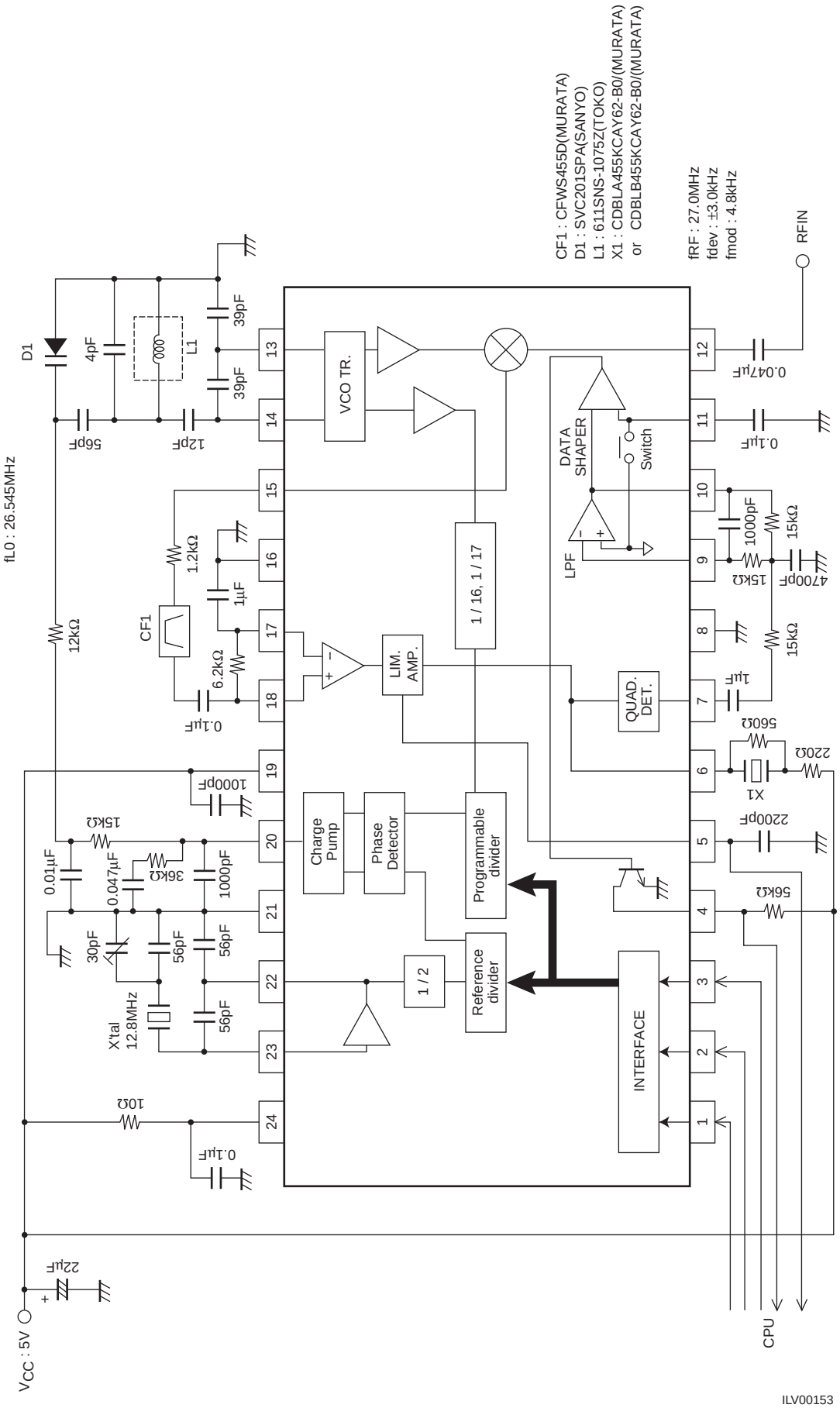
Test Circuit Diagram



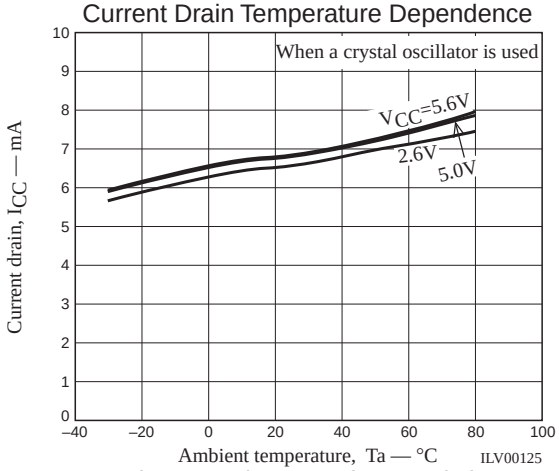
Sample Application Circuit 1 (Using a quadrature coil)



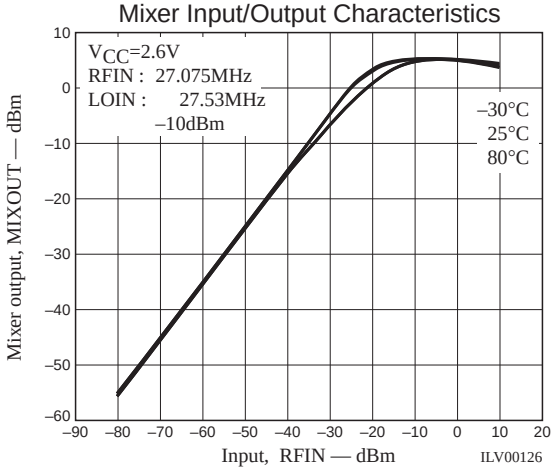
Sample Application Circuit 2 (Using a discriminator)



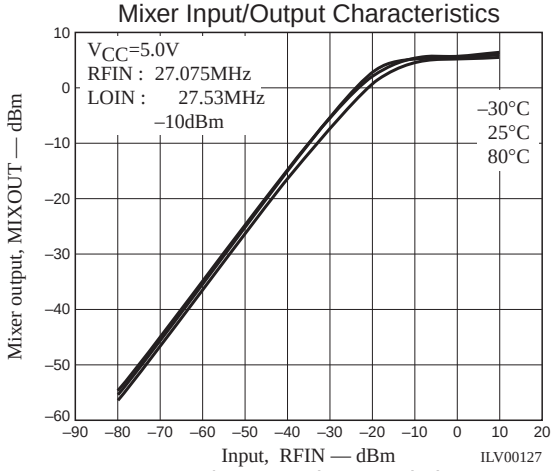
Current Drain Temperature Dependence



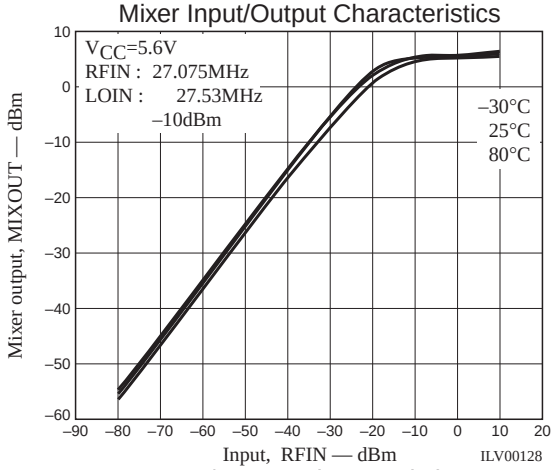
Mixer Input/Output Characteristics



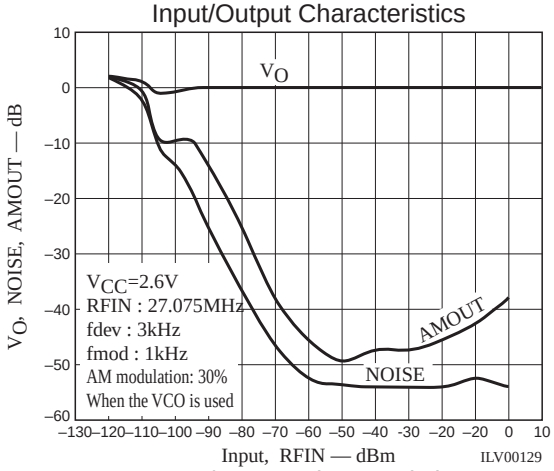
Mixer Input/Output Characteristics



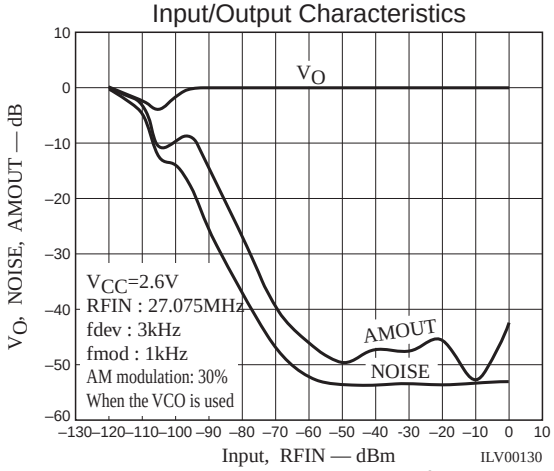
Mixer Input/Output Characteristics



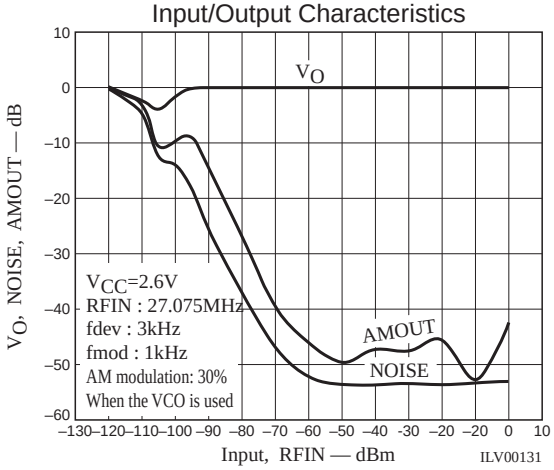
Input/Output Characteristics



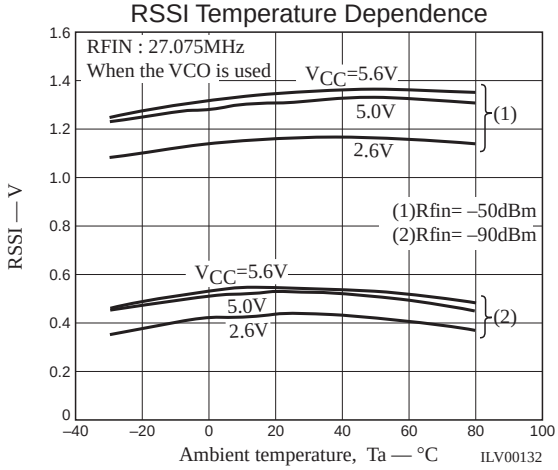
Input/Output Characteristics



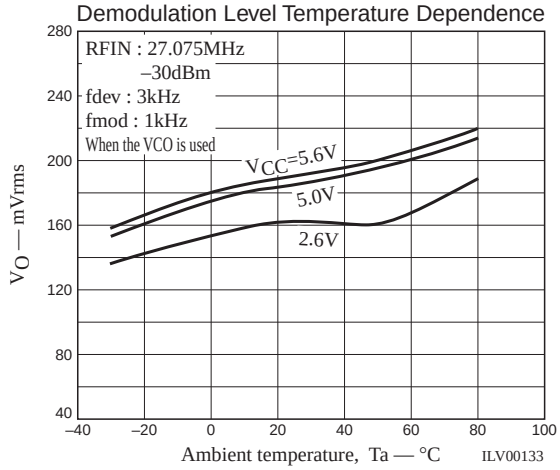
Input/Output Characteristics



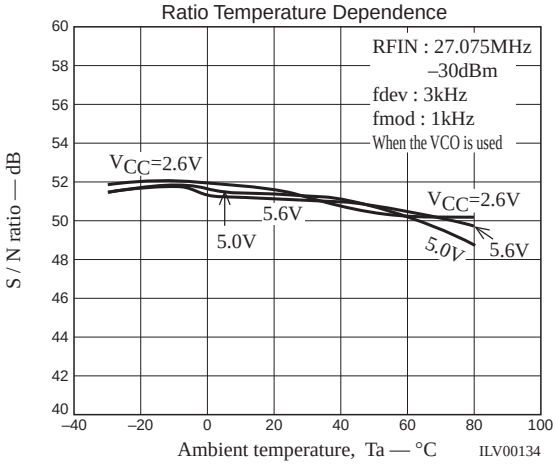
RSSI Temperature Dependence



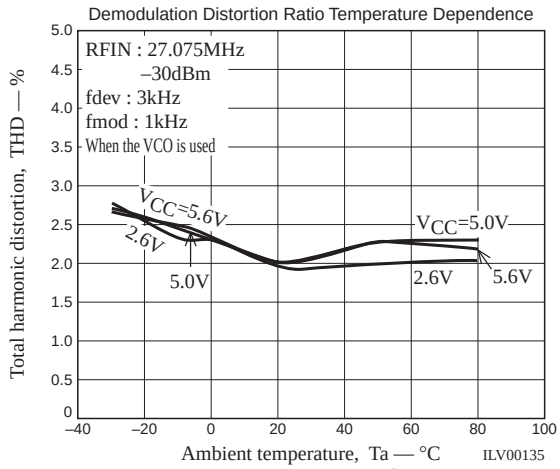
Demodulation Level Temperature Dependence



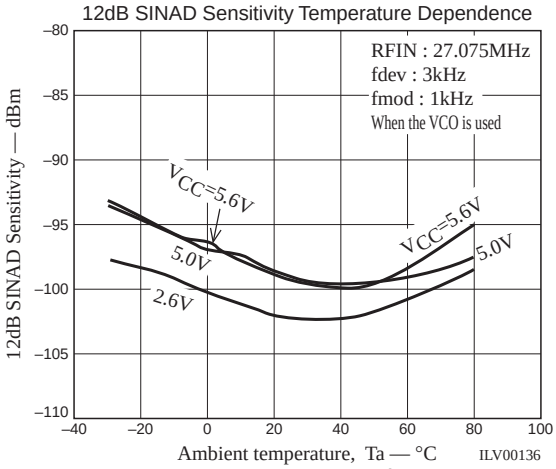
Demodulation Signal to Noise Ratio Temperature Dependence



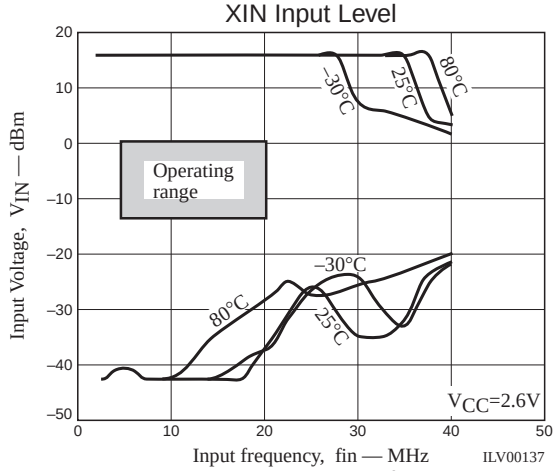
Demodulation Distortion Ratio Temperature Dependence



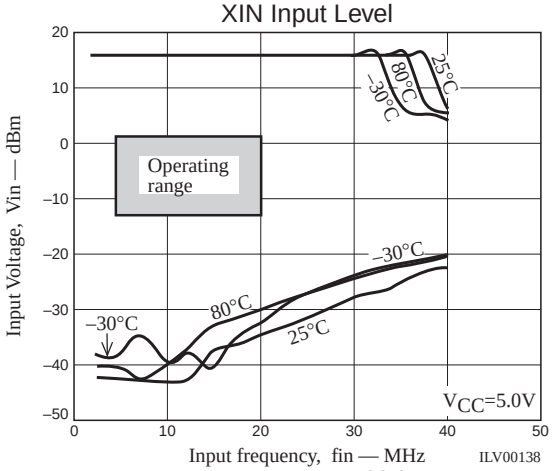
12dB SINAD Sensitivity Temperature Dependence



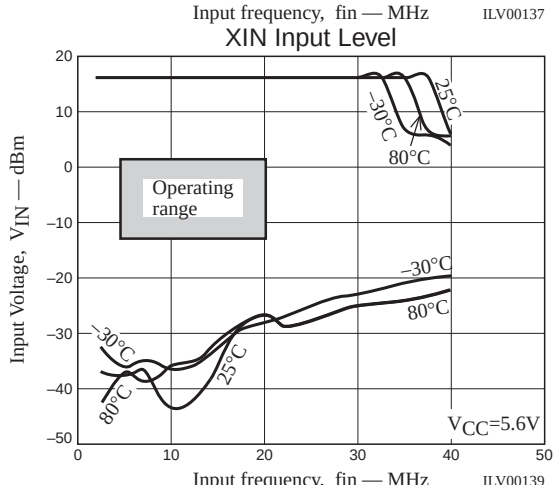
XIN Input Level



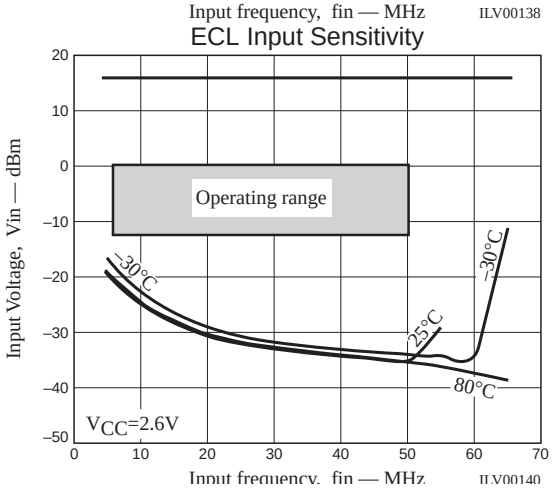
XIN Input Level



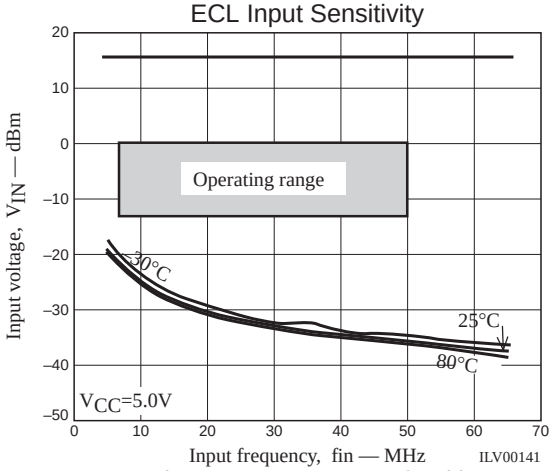
XIN Input Level



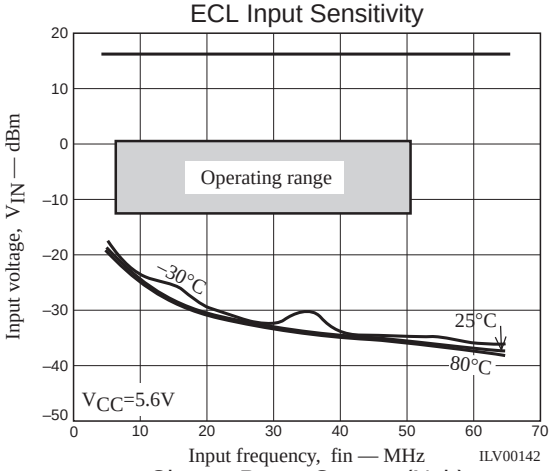
ECL Input Sensitivity



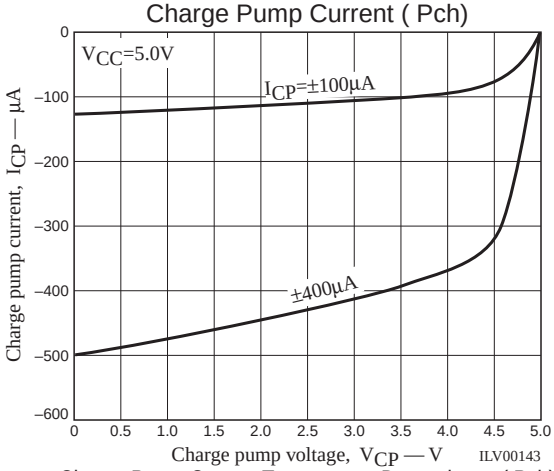
ECL Input Sensitivity



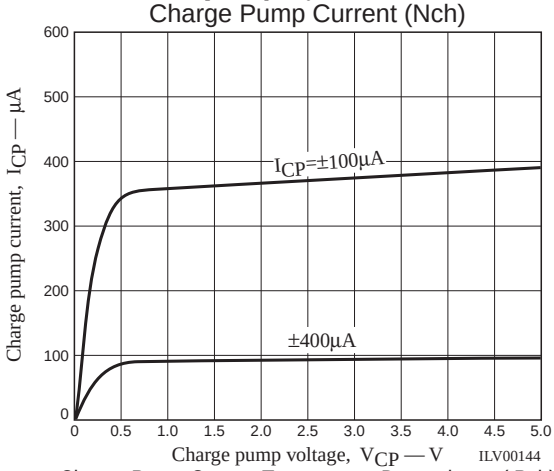
ECL Input Sensitivity



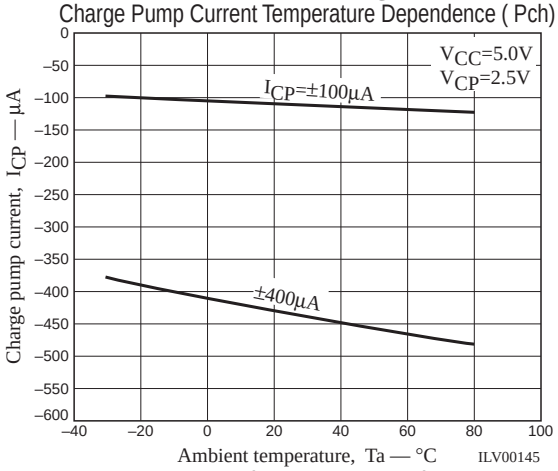
Charge Pump Current (Pch)



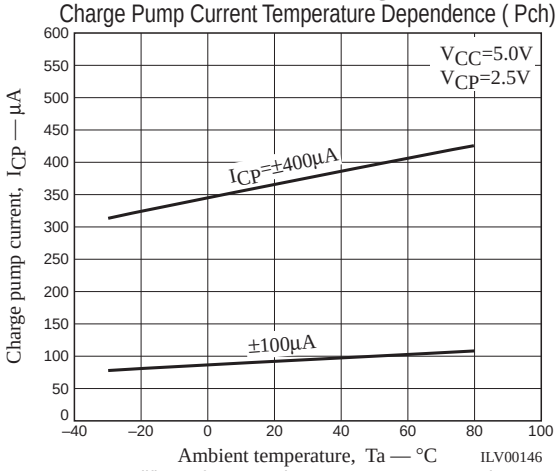
Charge Pump Current (Nch)



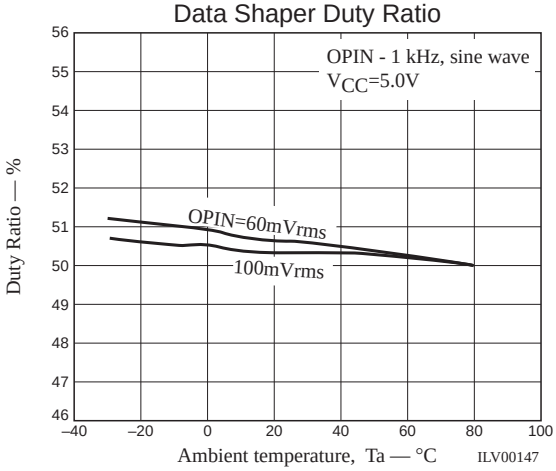
Charge Pump Current Temperature Dependence (Pch)



Charge Pump Current Temperature Dependence (Pch)



Data Shaper Duty Ratio



IF Amplifier Reference Voltage Temperature Dependence