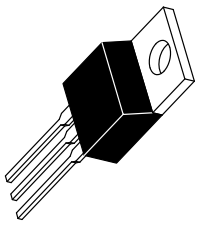
Silicon Controlled Rectifiers
Reverse Blocking Triode Thyristors

C122F1

SCR
8 AMPERES RMS
50 VOLTS

. . . designed primarily for full-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half–wave silicon gate–controlled, solid–state devices are needed.

- Glass Passivated Junctions and Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 50 Volts



CASE 221A-07
(TO-220AB)
STYLE 3

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Repetitive Peak Off–State Voltage(1) (T_J = 25 to 100°C, Gate Open) Repetitive Peak Reverse Voltage	V_{DRM} V_{RRM}	50	Volts
Peak Non–repetitive Reverse Voltage(1)	V_{RSM}	75	Volts
Forward Current RMS ($T_C \leq 75°C$) (All Conduction Angles)	$I_{T(RMS)}$	8	Amps
Peak Forward Surge Current (1/2 Cycle, Sine Wave, 60 Hz)	I_{TSM}	90	Amps
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	34	A^2s

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, (cont.) positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

MAXIMUM RATINGS — continued

Rating	Symbol	Value	Unit
Forward Peak Gate Power (t = 10 μs)	P_{GM}	5	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2	Amps
Operating Junction Temperature Range	T_J	–40 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.8	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (V_{AK} = Rated V_{DRM} or V_{RRM}, Gate Open) T_C = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_C = 100°C		—	—	0.5	mA
Peak On–State Voltage(1) (I_{TM} = 16 A Peak, T_C = 25°C)	V_{TM}	—	—	1.83	Volts
Gate Trigger Current (Continuous dc)	I_{GT}				mA
(V_D = 6 V, R_L = 91 Ohms, T_C = 25°C)		—	—	25	
(V_D = 6 V, R_L = 45 Ohms, T_C = –40°C)		—	—	40	
Gate Trigger Voltage (Continuous dc)	V_{GT}				Volts
(V_D = 6 V, R_L = 91 Ohms, T_C = 25°C)		—	—	1.5	
(V_D = 6 V, R_L = 45 Ohms, T_C = –40°C)		—	—	2	
(V_D = Rated V_{DRM}, R_L = 1000 Ohms, T_C = 100°C)		0.2	—	—	
Holding Current	I_H				mA
(V_D = 24 Vdc, I_T = 0.5 A, 0.1 to 10 ms Pulse, Gate Trigger Source = 7 V, 20 Ohms) T_C = 25°C		—	—	30	
T_C = –40°C		—	—	60	
Turn-Off Time (V_D = Rated V_{DRM}) (I_{TM} = 8 A, I_R = 8 A)	t_q	—	50	—	μs
Critical Rate–of–Rise of Off–State Voltage (V_D = Rated V_{DRM}, Linear, T_C = 100°C)	dv/dt	—	50	—	V/μs

1. Pulse Test: Pulse Width = 1 ms, Duty Cycle ≤ 2%.

FIGURE 1 – CURRENT DERATING (HALF–WAVE)

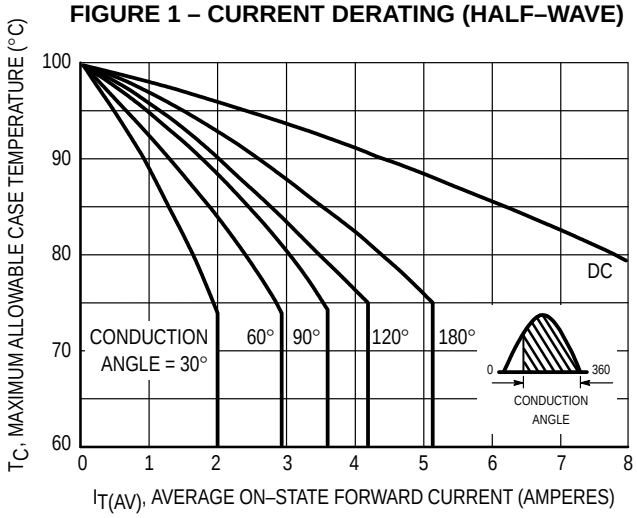


FIGURE 2 – CURRENT DERATING (FULL–WAVE)

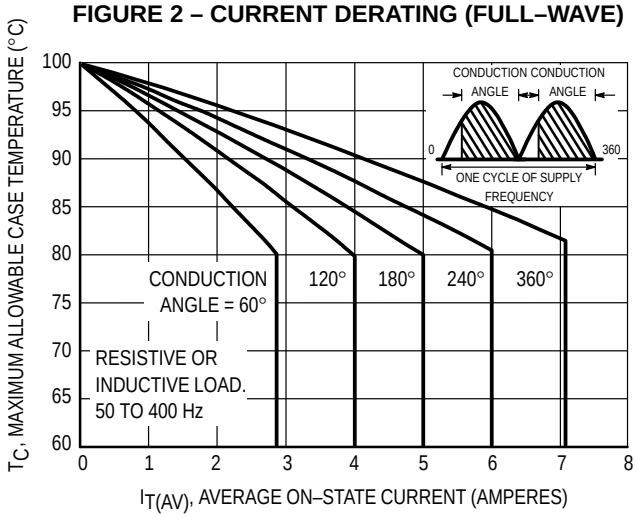


FIGURE 3 – MAXIMUM POWER DISSIPATION (HALF–WAVE)

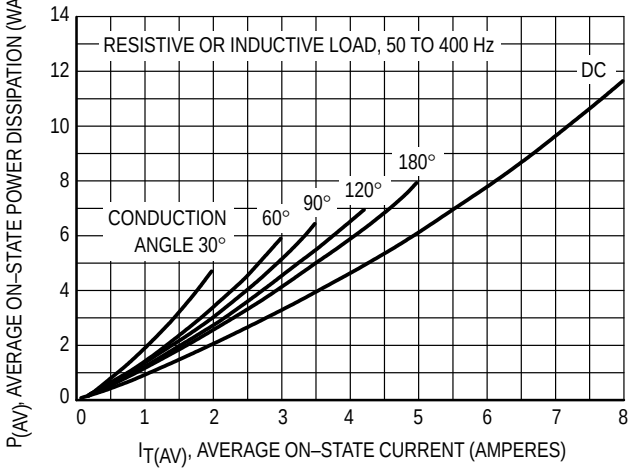
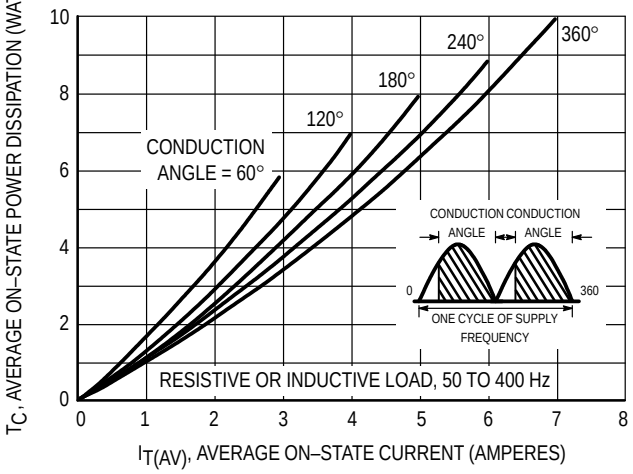
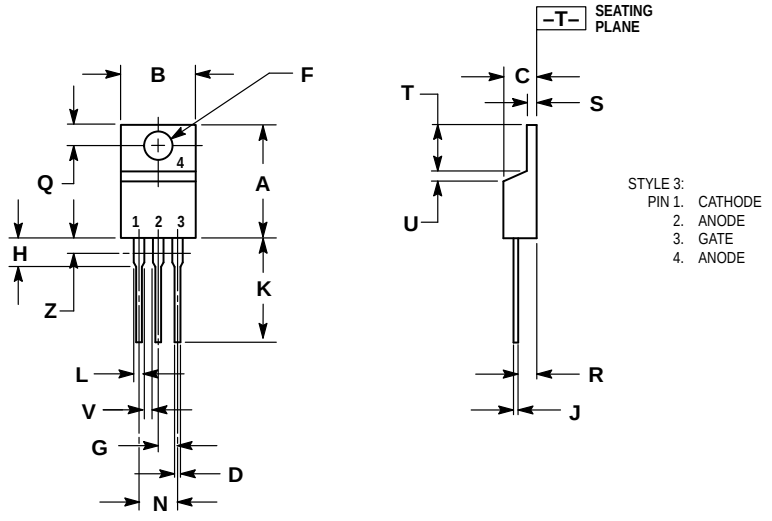


FIGURE 4 – MAXIMUM POWER DISSIPATION (FULL–WAVE)



PACKAGE DIMENSIONS



STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.022	0.36	0.55
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

CASE 221A-07
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ISSUE Z

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51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

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