

# DATA SHEET

## **2N7000**

**N-channel enhancement mode  
vertical D-MOS transistor**

Product specification  
File under Discrete Semiconductors, SC13b

April 1995

# N-channel enhancement mode vertical D-MOS transistor

2N7000

### FEATURES

- Low  $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

### DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line transformer drivers.

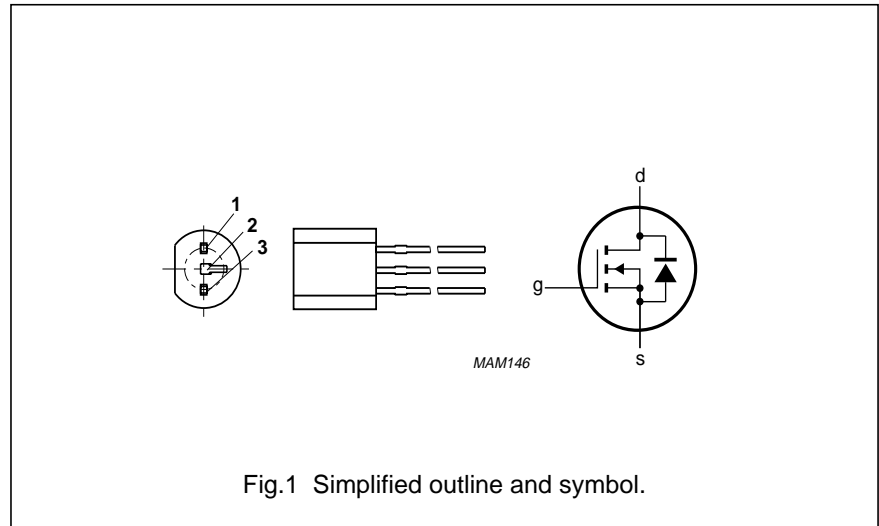
### PINNING - TO-92 VARIANT

PIN	DESCRIPTION
1	drain
2	gate
3	source

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$V_{DS}$	drain-source voltage		60	V
$I_D$	drain current	DC value	280	mA
$R_{DS(on)}$	drain-source on-resistance	$I_D = 500\text{ mA}$ $V_{GS} = 10\text{ V}$	5	$\Omega$
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$ $V_{GS} = V_{DS}$	3	V

### PIN CONFIGURATION



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## LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	60	V
$V_{DG}$	drain-gate voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	40	V
$I_D$	drain current	DC value	–	280	mA
$I_{DM}$	drain current	peak value	–	1.3	A
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	–	830	mW
$T_{stg}$	storage temperature range		–55	150	°C
$T_j$	junction temperature		–	150	°C

## THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient	150	K/W

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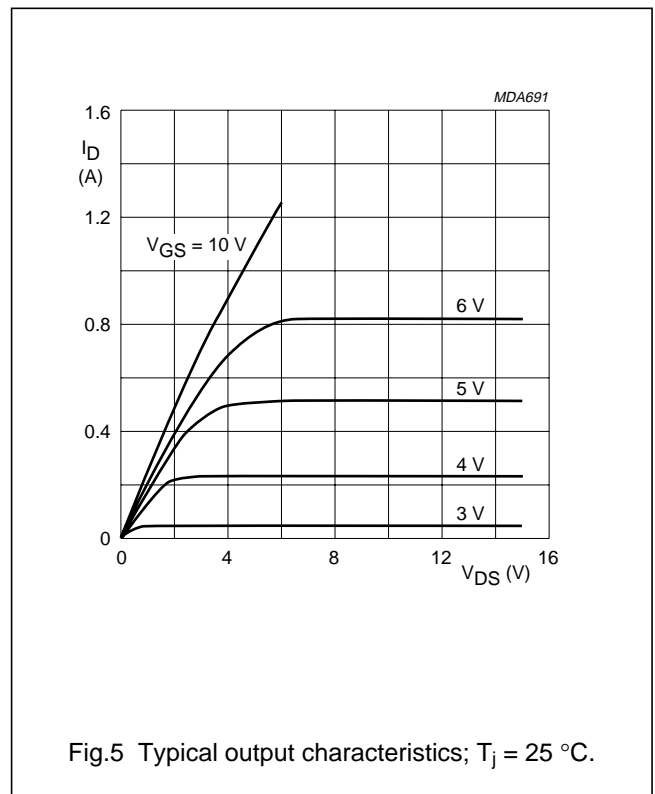
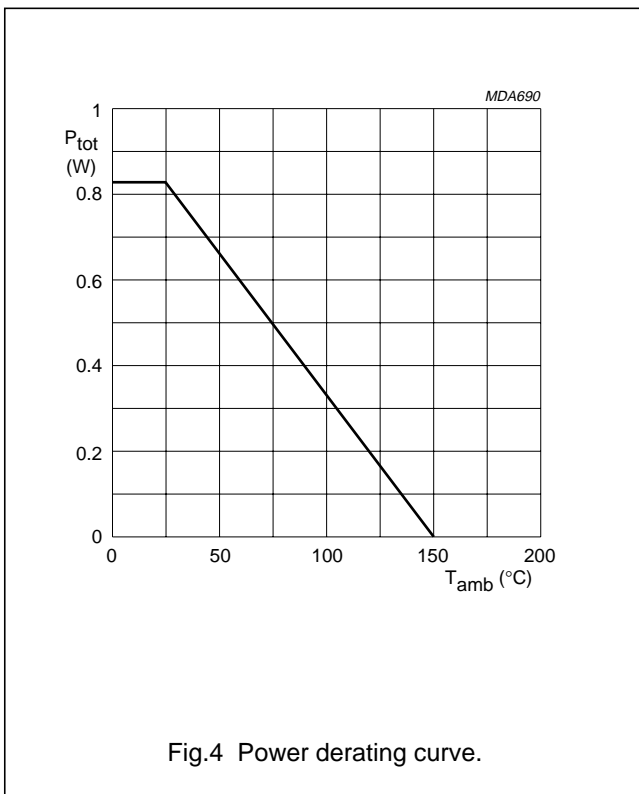
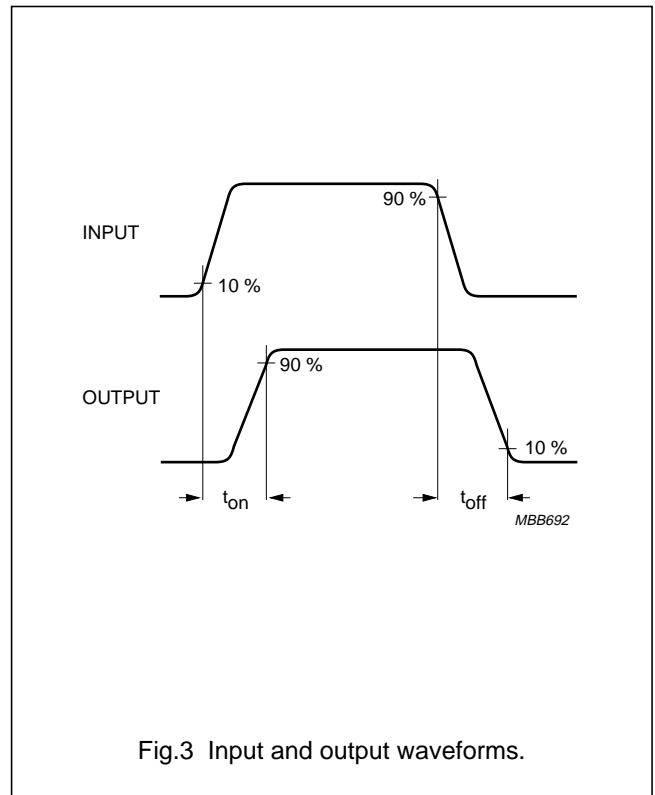
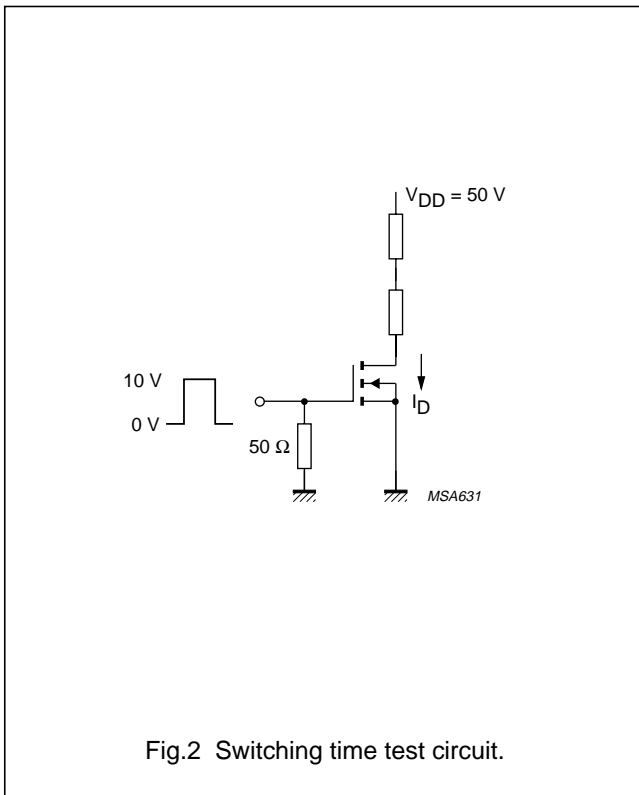
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**CHARACTERISTICS** $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\ \mu\text{A}$ $V_{GS} = 0$	60	90	–	V
$I_{DSS}$	drain-source leakage current	$V_{DS} = 48\ \text{V}$ $V_{GS} = 0$	–	–	1	$\mu\text{A}$
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS} = 15\ \text{V}$ $V_{DS} = 0$	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$ $V_{GS} = V_{DS}$	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	$I_D = 500\ \text{mA}$ $V_{GS} = 10\ \text{V}$	–	3.5	5	$\Omega$
		$I_D = 75\ \text{mA}$ $V_{GS} = 4.5\ \text{V}$	–	–	5.3	$\Omega$
$ Y_{fs} $	transfer admittance	$I_D = 200\ \text{mA}$ $V_{DS} = 10\ \text{V}$	100	200	–	mS
$C_{iss}$	input capacitance	$V_{DS} = 10\ \text{V}$ $V_{GS} = 0$ $f = 1\ \text{MHz}$	–	25	40	pF
$C_{oss}$	output capacitance	$V_{DS} = 10\ \text{V}$ $V_{GS} = 0$ $f = 1\ \text{MHz}$	–	22	30	pF
$C_{rss}$	feedback capacitance	$V_{DS} = 10\ \text{V}$ $V_{GS} = 0$ $f = 1\ \text{MHz}$	–	6	10	pF
<b>Switching times (see Figs 2 and 3)</b>						
$t_{on}$	turn-on time	$I_D = 200\ \text{mA}$ $V_{DD} = 50\ \text{V}$ $V_{GS} = 0\ \text{to}\ 10\ \text{V}$	–	4	10	ns
$t_{off}$	turn-off time	$I_D = 200\ \text{mA}$ $V_{DD} = 50\ \text{V}$ $V_{GS} = 0\ \text{to}\ 10\ \text{V}$	–	4	10	ns

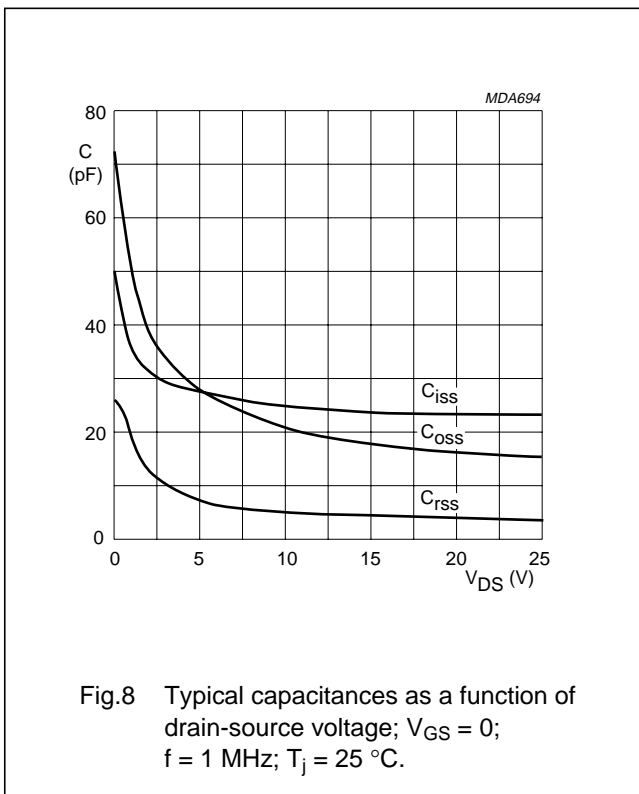
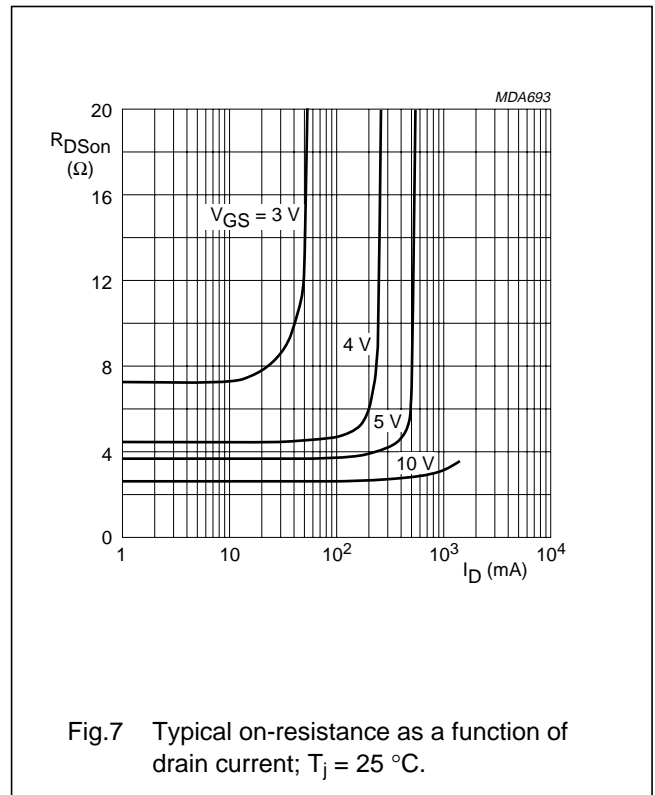
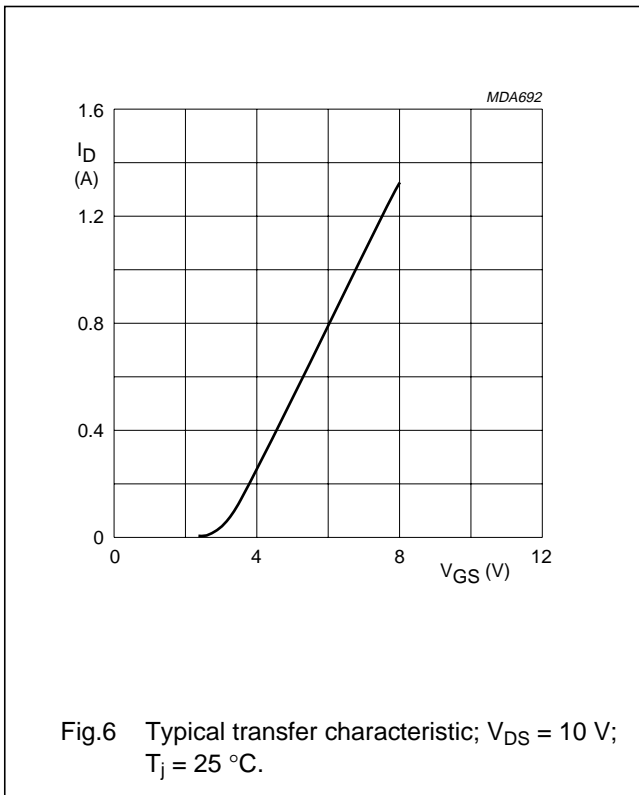
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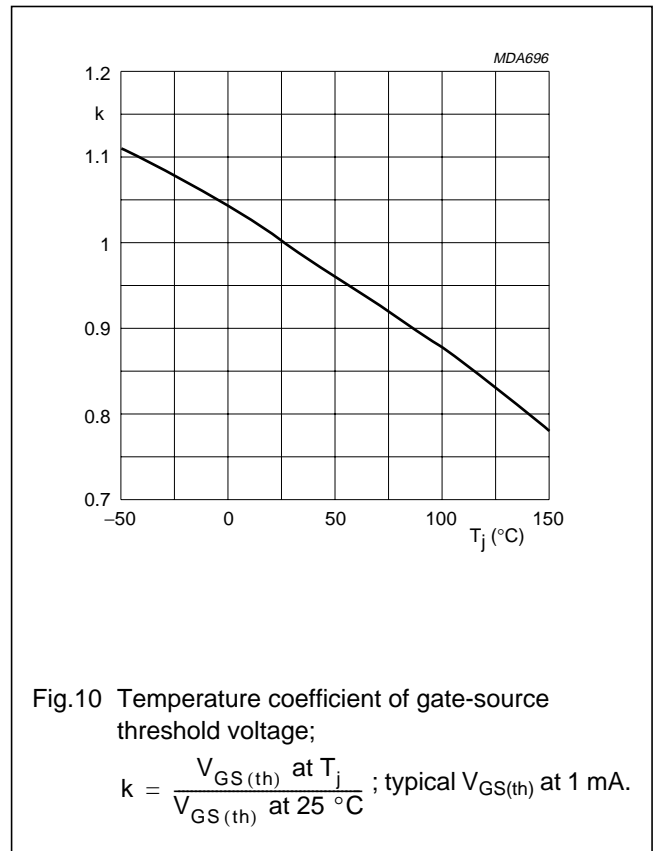
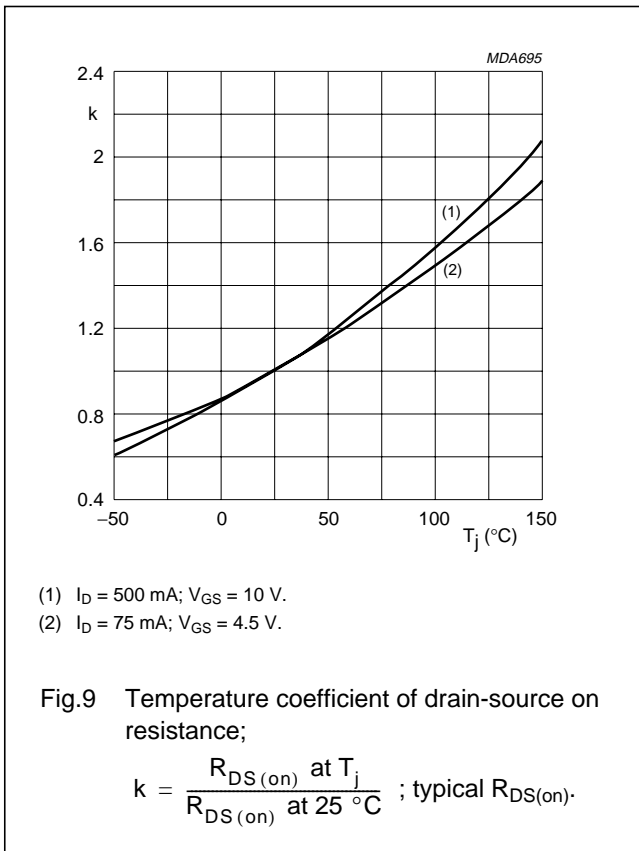
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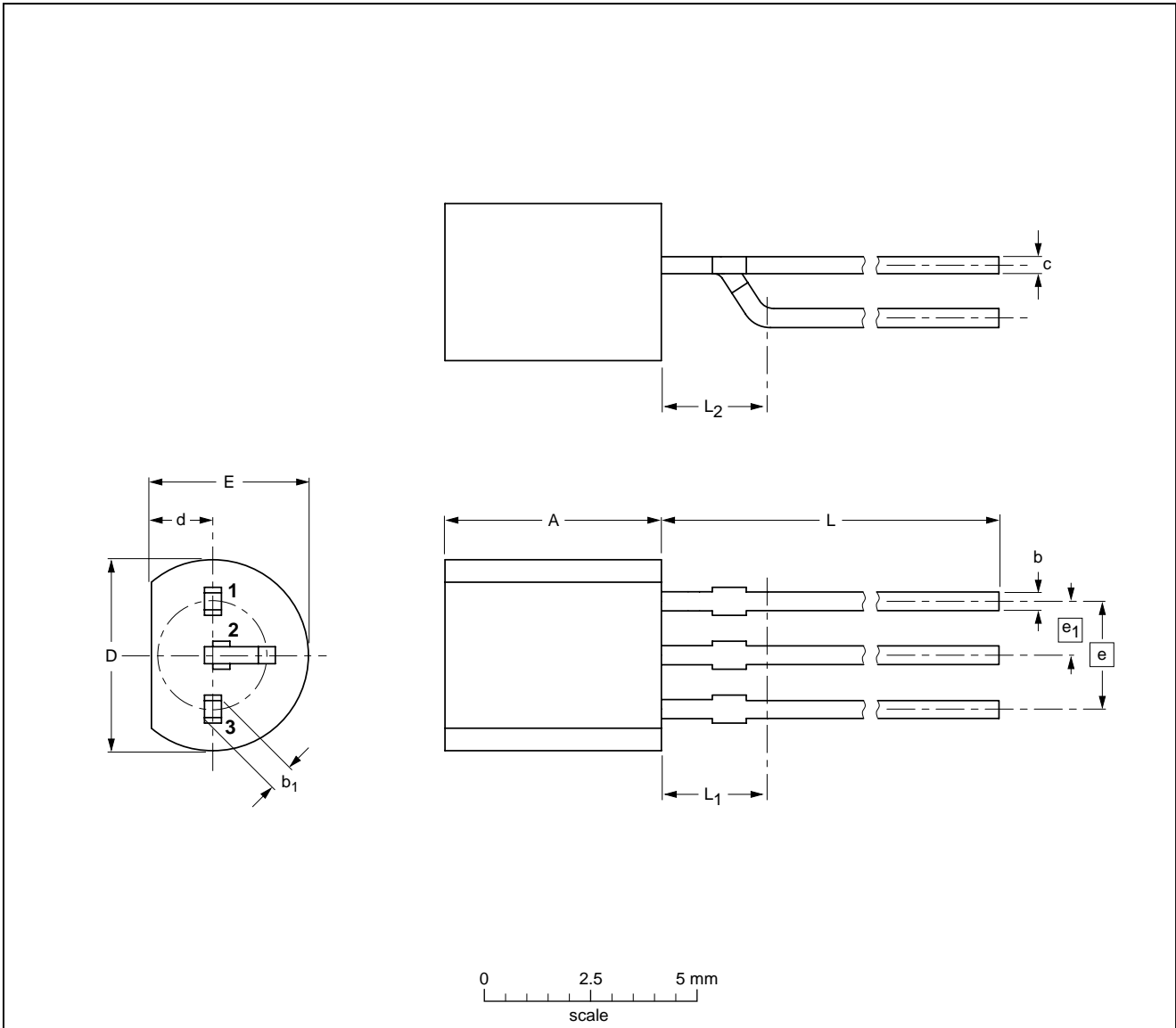
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PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads (on-circle)

SOT54 variant



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b <sub>1</sub>	c	D	d	E	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup> max	L <sub>2</sub> max
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54 variant		TO-92	SC-43			97-04-14



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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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**NOTES**

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**NOTES**

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