# DATA SHEET


# TDA10021HT
## DVB-C channel receiver

Product specification
Supersedes data of 2000 Jun 21
File under Integrated Circuits, IC02

2001 Oct 01

Philips
Semiconductors

PHILIPS

## FEATURES

- 4, 16, 32, 64, 128 and 256 Quadrature Amplitude Modulation (QAM) demodulator (DVB-C compatible: ETS 300-429/ITU-T J83 annex A/C)
- High performance for 256 QAM, especially for direct IF applications
- On-chip 10-bit Analog-to-Digital Converter (ADC)
- On-chip Phase-Locked Loop (PLL) for crystal frequency multiplication (typically 4 MHz crystal)
- Digital downconversion
- Programmable half Nyquist filter (roll off = 0.15 or 0.13)
- Two Pulse Width Modulated (PWM) AGC outputs with programmable take over point (for tuner and downconverter control)
- Clock timing recovery, with programmable 2nd-order loop filter
- Variable symbol rate capability from SACLK/64 to SACLK/4 (SACLK = 36 MHz maximum)
- Programmable anti-aliasing filters
- Full digital carrier recovery loop
- Carrier acquisition range up to 18% of symbol rate
- Integrated adaptive equalizer (linear transversal equalizer or decision feedback equalizer)
- On-chip Forward Error Correction (FEC) decoder (de-interleaver and RS decoder) and fully DVB-C compliant
- DVB compatible differential decoding and mapping
- Parallel and serial transport stream interface simultaneously
- $I^2C$-bus interface, for easy control
- CMOS 0.2 μm technology.

## APPLICATIONS

- Cable set-top boxes
- Cable modems
- MMDS (ETS 300-749) set-top boxes.

## GENERAL DESCRIPTION

The TDA10021HT is a single-chip DVB-C channel receiver for 4, 16, 32, 64, 128 and 256 QAM modulated signals. The device interfaces directly to the IF signal, which is sampled by a 10-bit ADC.

The TDA10021HT performs the clock and the carrier recovery functions. The digital loop filters for both clock and carrier recovery are programmable in order to optimize their characteristics according to the current application.

After baseband conversion, equalization filters are used for echo cancellation in cable applications. These filters are configured as either a T-spaced transversal equalizer or a Decision Feedback Equalizer (DFE), so that the system performance can be optimized according to the network characteristics. A proprietary equalization algorithm, independent of carrier offset, is achieved in order to assist carrier recovery. A decision directed algorithm then takes place, to achieve final equalization convergence.

The TDA10021HT implements a FORNEY convolutional de-interleaver of depth 12 blocks and a Reed-Solomon decoder which corrects up to 8 erroneous bytes. The de-interleaver and the RS decoder are automatically synchronized by the frame synchronization algorithm which uses the MPEG-2 sync byte. Finally descrambling according to DVB-C standard, is achieved at the Reed Solomon output. This device is controlled via an $I^2C$-bus.

Designed in 0.2 μm CMOS technology and housed in a 64 pin TQFP package, the TDA10021HT operates over the commercial temperature range.

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| TDA10021HT | TQFP64 | plastic thin quad flat package; 64 leads; body 10 × 10 × 1.0 mm | SOT357-1 |

## BLOCK DIAGRAM

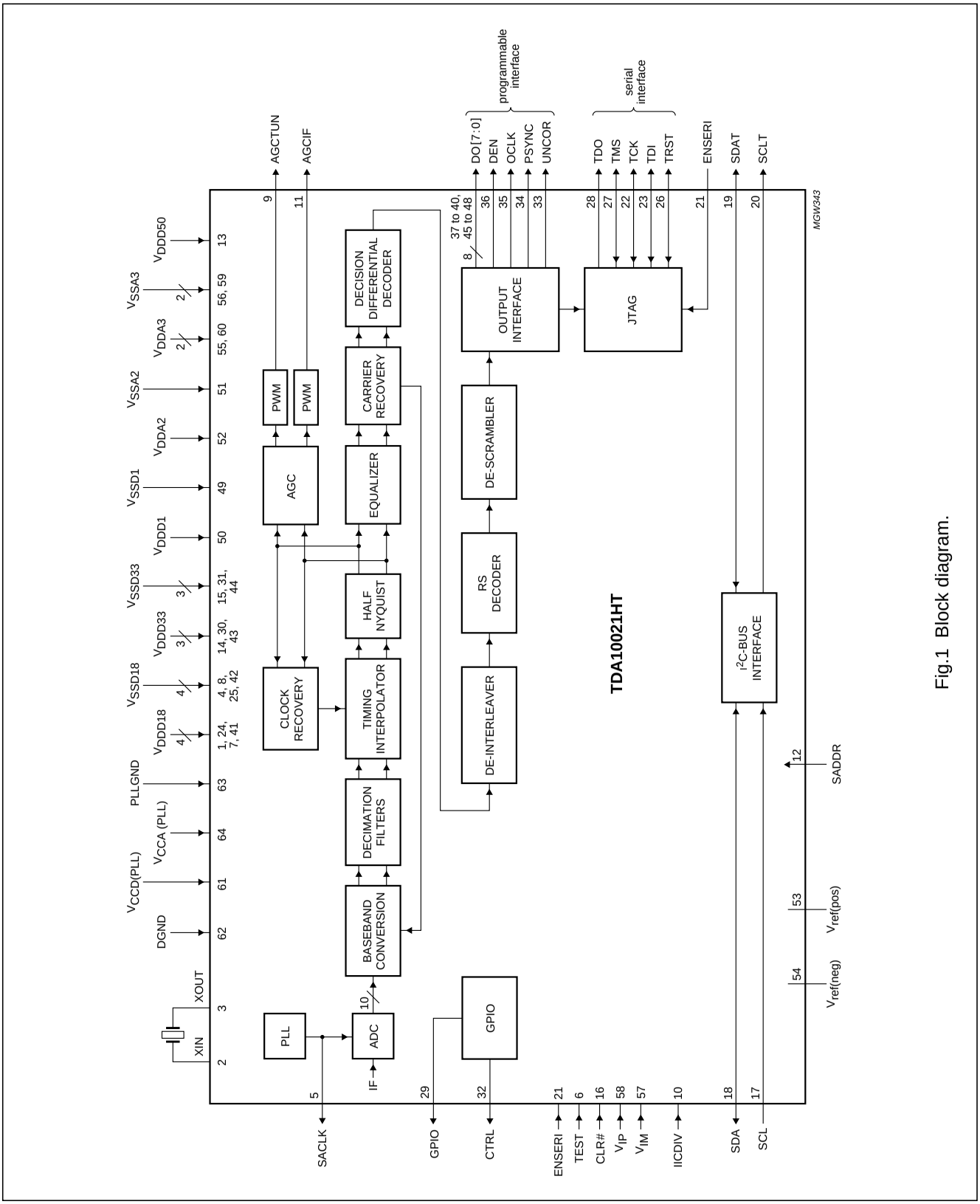



Fig.1 Block diagram.

**PINNING**

| SYMBOL | PIN | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| $V_{DDD18}$ | 1 | S | digital supply voltage for the core (1.8 V typ.) |
| XIN | 2 | I | XTAL oscillator input pin: a fundamental XTAL oscillator is connected between the XIN and XOUT pins. The XTAL frequency must be chosen so that the system frequency SYSCLK (XIN × multiplying factor of the PLL) equals 1.6 times the tuner output intermediate frequency; i.e. SYSCLK = 1.6 × IF. |
| XOUT | 3 | O | XTAL oscillator output pin: a fundamental XTAL oscillator is connected between the XIN and XOUT pins |
| $V_{SSD18}$ | 4 | G | digital ground for the core |
| SACLK | 5 | O | sampling clock: this output clock can be fed to an external 10-bit ADC as the sampling clock; SACLK = SYSCLK/2 |
| TEST | 6 | I | test input pin: in normal mode, pin TEST must be connected to ground |
| $V_{DDD18}$ | 7 | S | digital supply voltage for the core (1.8 V typ.) |
| $V_{SSD18}$ | 8 | G | digital ground for the core |
| AGCTUN | 9 | O/OD | first PWM encoded output signal for AGC tuner: this signal is fed to the AGC amplifier through a single RC network. The maximum signal frequency on the VAGC output is XIN/16. AGC information is refreshed every 1024 symbols. |
| IICDIV | 10 | I | IICDIV: this pin allows the frequency of the $I^2C$-bus internal system clock to be selected, depending on the crystal frequency. The internal $I^2C$-bus clock is a division of XIN by $4^{IICDIV}$. |
| AGCIF | 11 | O/OD | second PWM encoded output signal for the AGC IF: This signal is fed to the AGC amplifier through a single RC network. The maximum signal frequency on the VAGC output is XIN/16. AGC information is refreshed every 1024 symbols. However AGCIF can also be configured to output a PWM signal, the value of which can be programmed through the $I^2C$-bus interface. |
| SADDR | 12 | I | SADDR is the LSB of the $I^2C$-bus address of the TDA10021HT. The MSBs are internally set to 000110. Therefore the complete $I^2C$-bus address of the TDA10021HT is (MSB to LSB) 0, 0, 0, 1, 1, 0 and SADDR. |
| $V_{DDD50}$ | 13 | S | digital supply voltage for the pad 5.0 V (necessary for 5 V tolerant inputs) |
| $V_{DDD33}$ | 14 | S | digital supply voltage for the pads (3.3 V typ.) |
| $V_{SSD33}$ | 15 | G | digital ground for the pads |
| CLR# | 16 | I | the CLR# input is asynchronous and active LOW, and clears the TDA10021HT: When CLR# goes LOW, the circuit immediately enters its reset mode and normal operation will resume 4 XIN falling edges after CLR# returns HIGH. The $I^2C$-bus register contents are all initialized to their default values. The minimum width of CLR# at LOW level is 4 XIN clock periods. |
| SCL | 17 | I | $I^2C$-bus clock input: SCL should nominally be a square wave with a maximum frequency of 400 kHz. SCL is generated by the system $I^2C$-bus master. |
| SDA | 18 | I/OD | SDA is a bidirectional signal: it is the serial input/output of the $I^2C$-bus internal block. A pull-up resistor (typically 4.7 kΩ) must be connected between SDA and $V_{DDD50}$ for proper operation (open-drain output). |
| SDAT | 19 | I/OD | SDAT is equivalent to SDA I/O of the TDA10021HT but can be 3-stated by $I^2C$-bus programming. It is actually the output of a switch controlled by parameter BYPIIC of register TEST (index 0F). SDAT is an open-drain output and therefore requires an external pull-up resistor. |

| SYMBOL | PIN | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| SCLT | 20 | OD | SCLT can be configured to be a control line output or to output the SCL input. This is controlled by parameter BYPIIC and CTRL_SCLT of register TEST (index 0F). SCLT is an open-drain output and therefore requires an external pull-up resistor. |
| ENSERI | 21 | I | when HIGH this pin enables the serial output transport stream through the boundary scan pins TRST, TDO, TCK, TDI and TMS (serial interface). Must be set LOW in bist and boundary scan mode. |
| TCK | 22 | I/O | test clock: an independent clock used to drive the TAP controller in boundary scan mode. In normal mode of operation, TCK must be set LOW. In serial stream mode, TCK is the clock output (OCLK). |
| TDI | 23 | I/O | test data input: the serial input for test data and instruction in boundary scan mode. In normal mode of operation, TDI must be set LOW. In serial stream mode, the TDI is the PSYNC output. |
| $V_{DDDI8}$ | 24 | S | digital supply voltage for the core (1.8 V typ.) |
| $V_{SSDI8}$ | 25 | G | digital ground for the core |
| TRST | 26 | I/O | test reset: this active LOW input signal is used to reset the TAP controller in boundary scan mode. In normal mode of operation, TRST must be set LOW. In serial stream mode, TRST is the uncorrectable output (UNCOR). |
| TMS | 27 | I/O | test mode select: this input signal provides the logic levels needed to change the TAP controller from state to state. In normal mode of operation, TMS must be set to HIGH. In serial stream mode, TMS is the DEN output. |
| TDO | 28 | O | test data output: this is the serial test output pin used in boundary scan mode. Serial data is provided on the falling edge of TCK. In serial stream mode, TDO is the data output (DO). |
| GPIO | 29 | OD | GPIO can be configured by the $I^2C$-bus either as:<br>• A Front-End Lock indicator (FEL) (default mode)<br>• An active LOW output interrupt line (IT) which can be configured by the $I^2C$-bus interface<br>• A control output pin programmable by $I^2C$-bus.<br>GPIO is an open-drain output and therefore requires an external pull-up resistor. |
| $V_{DDD33}$ | 30 | S | digital supply voltage for the pads (3.3 V typ.) |
| $V_{SSD33}$ | 31 | G | digital ground for the pads |
| CTRL | 32 | OD | CTRL is a control output pin programmable by the $I^2C$-bus. CTRL is an open-drain output and therefore requires an external pull-up resistor. |
| UNCOR | 33 | O | uncorrectable packet: this output signal is HIGH when the provided packet is uncorrectable (during the 188 bytes of the packet). The uncorrectable packet is not affected by the Reed Solomon decoder, but the MSB of the byte following the sync byte is forced to logic 1 for the MPEG-2 process: error flag indicator (if RSI and IEI are set LOW in the $I^2C$-bus table). |
| PSYNC | 34 | O | pulse synchro: this output signal goes HIGH when the sync byte (0x47) is provided, then it goes LOW until the next sync byte |
| OCLK | 35 | O | output clock: this is the output clock for the DO[7:0] data outputs. OCLK is internally generated depending on which interface is selected. |
| DEN | 36 | O | data enable: this output signal is HIGH when there is valid data on the output bus DO[7:0] |

| SYMBOL | PIN | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| DO[7:4] | 37 to 40 | O | data output bus: this 8-bit parallel data is the output from the TDA10021HT after demodulation, de-interleaving, RS decoding and de-scrambling. When one of the two possible parallel interfaces is selected (parameter SERINT = 0, index 20) then DO[7:0] is the transport stream output. When the serial interface is selected (parameter SERINT = 1, index 20) then the serial output is on pin DO[0]. |
| $V_{DDDI8}$ | 41 | S | digital supply voltage for the core (1.8 V typ.) |
| $V_{SSD18}$ | 42 | G | digital ground for the core |
| $V_{DDD33}$ | 43 | S | digital supply voltage for the pads (3.3 V typ.) |
| $V_{SSD33}$ | 44 | G | digital ground for the pads |
| DO[3:0] | 45 to 48 | O | data output bus: this 8-bit parallel data is the output from the TDA10021HT after demodulation, de-interleaving, RS decoding and de-scrambling. When one of the two possible parallel interfaces is selected then DO[7:0] is the transport stream output. When the serial interface is selected then the serial output is on pin DO[0]. |
| $V_{SSD1}$ | 49 | G | ground return for the digital switching circuitry (ADC) |
| $V_{DDD1}$ | 50 | S | power supply input for the digital switching circuitry 1.8 V (ADC) |
| $V_{SSA2}$ | 51 | G | ground return for the analog clock drivers (ADC) |
| $V_{DDA2}$ | 52 | S | power supply input for the analog clock drivers 3.3 V (ADC) |
| $V_{ref(pos)}$ | 53 | O | this is a positive voltage reference for the ADC. It is derived from the internal band gap voltage, VBG, with an on-chip fully differential amplifier. |
| $V_{ref(neg)}$ | 54 | O | this is the negative voltage reference for the ADC. It is derived from the internal band gap voltage, VBG, with an on-chip fully differential amplifier. |
| $V_{DDA3}$ | 55 | S | power supply input for the analog circuits 3.3 V (ADC) |
| $V_{SSA3}$ | 56 | G | ground return for analog circuits (ADC) |
| $V_{IM}$ | 57 | I | negative input to the ADC: this pin is DC biased to half-supply through an internal resistor divider ($2 \times 20$ kΩ resistors). In order to stay in the range of the ADC, $\lvert V_{IP} - V_{IM} \rvert$ should remain between the input range corresponding to the SW register (index 1B – default value = 0.5 V). |
| $V_{IP}$ | 58 | I | positive input to the ADC: this pin is DC biased to half-supply through an internal resistor divider ($2 \times 20$ kΩ resistors). In order to stay in the range of the ADC, $\lvert V_{IP} - V_{IM} \rvert$ should remain between the input range corresponding to the SW register (index 1B – default value = 0.5 V). |
| $V_{SSA3}$ | 59 | G | ground return for analog circuits (ADC) |
| $V_{DDA3}$ | 60 | S | power supply input for the analog circuits 3.3 V (ADC) |
| $V_{CCD(PLL)}$ | 61 | S | power supply for the PLL digital section 1.8 V |
| DGND | 62 | G | ground connection for the PLL digital section |
| PLLGND | 63 | G | ground connection for the PLL analog section |
| $V_{CCA(PLL)}$ | 64 | S | power supply for the PLL analog section 3.3 V |

**Note**

1. All inputs (I) are TTL, 5 V tolerant (except pins XIN, $V_{IP}$ and $V_{IM}$). OD are open-drain outputs, so they must be connected by a pull-up resistor to either $V_{DDD33}$ or $V_{DDD50}$.

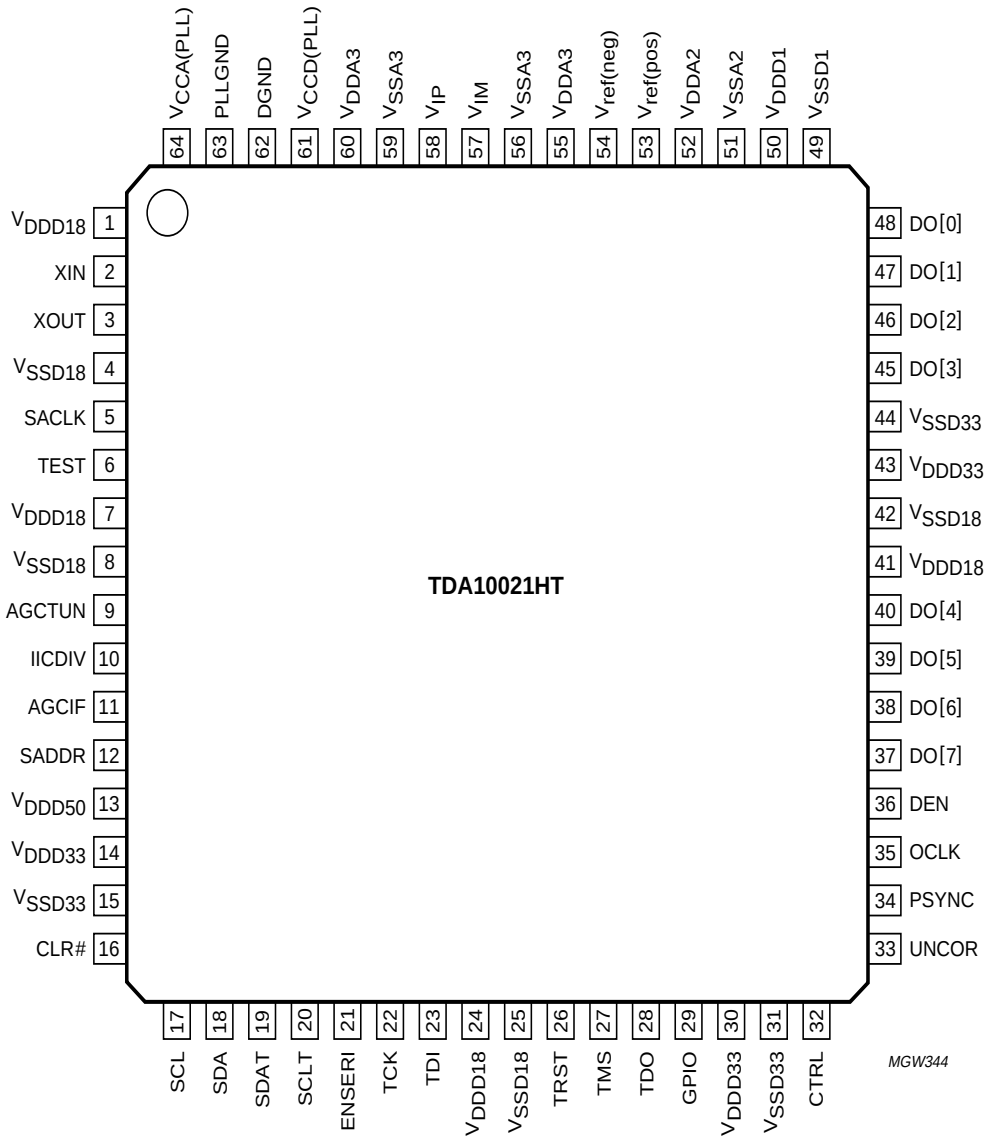



Fig.1 Pin configuration.

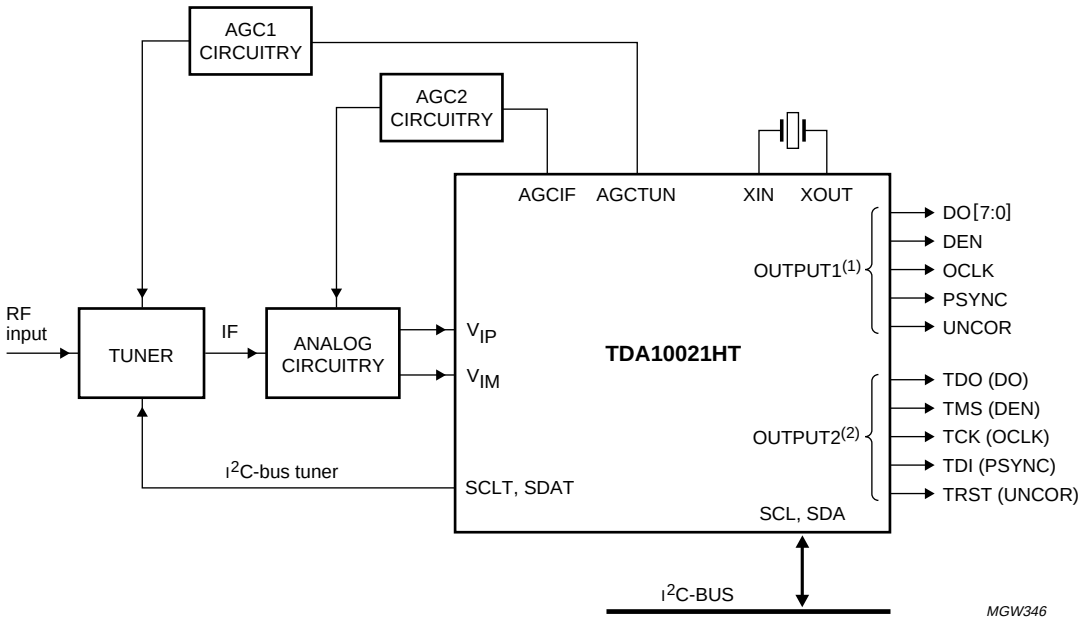
**CHARACTERISTICS**

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{DDD33}$ | digital supply voltage for the pads | $V_{DDD}$ = 3.3 V ±10% | 2.97 | 3.3 | 3.63 | V |
| $V_{DDD18}$ | digital supply voltage for the core | $V_{DDD}$ = 1.8 V ±5% | 1.7 | 1.8 | 1.9 | V |
| $V_{DDD50}$ | digital supply voltage | only for 5 V requirements; note 1 | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | TTL input; note 2 | 2 | – | $V_{DDD50}$ | V |
| $V_{IL}$ | LOW-level input voltage | TTL input | 0 | – | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | note 3 | 2.4 | – | – | V |
| $V_{OL}$ | LOW-level output voltage | | – | – | 0.4 | V |
| $I_{DDD33}$ | digital supply current for the pads | $f_s$ = 28.92 MHz; symbol rate = 7 Mbaud | – | 46 | – | mA |
| $I_{DDD18}$ | digital supply current for the core | $f_s$ = 28.92 MHz; symbol rate = 7 Mbaud | – | 120 | – | mA |
| $P_{tot}$ | total power dissipation | $f_s$ = 28.92 MHz; symbol rate = 7 Mbaud | – | 540 | – | mW |
| $C_i$ | input capacitance | | – | – | 5 | pF |
| $T_{amb}$ | ambient temperature | | 0 | – | 70 | °C |
| **XTAL; pin XIN** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{DDD33}$ | – | $V_{DDD33}$ | V |
| $V_{IL}$ | LOW-level input voltage | | 0 | – | $0.3V_{DDD33}$ | V |
| **PLL** | | | | | | |
| $V_{DDD(PLL)}$ | digital PLL supply voltage | $V_{DDD}$ = 1.8 V ±5% | 1.7 | 1.8 | 1.9 | V |
| $V_{DDA(PLL)}$ | analog PLL supply voltage | $V_{DDA}$ = 3.3 V ±10% | 2.97 | 3.3 | 3.63 | V |
| **ADC** | | | | | | |
| $V_{DDA1}$ | analog ADC supply voltage | $V_{DDA}$ = 1.8 V ±5% | 1.7 | 1.8 | 1.9 | V |
| $V_{DDA2}$,$V_{DDA3}$ | analog ADC supply voltage | $V_{DDA}$ = 3.3 V ±10% | 2.97 | 3.3 | 3.63 | V |
| $V_{IP}$,$V_{IM}$ | analog ADC inputs | | –0.5 | – | $V_{DDA3}$ + 0.5 | V |
| $V_i$ | signal input range | $I_R = V_{IP} - V_{IM}$ | –0.5 to –1.0 | – | +0.5 to +1.0 | V |
| $V_{ref(pos)}$ | positive reference voltage | | 1.95 | 2.15 | 2.35 | V |
| $V_{ref(neg)}$ | negative reference voltage | | 0.95 | 1.15 | 1.35 | V |
| $V_{offset}$ | input offset voltage | | –25 | – | +25 | mV |
| $R_i$ | input resistance ($V_{IP}$ or $V_{IM}$) | | – | 10 | – | kΩ |
| $C_i$ | input capacitance ($V_{IP}$ or $V_{IM}$) | | – | 5 | 10 | pF |
| B | input full power bandwidth | 3 dB bandwidth | 40 | 50 | – | MHz |

**Notes**

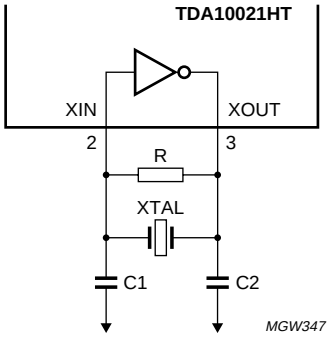
1. The voltage level of the 5 V supply must always exceed or at least equal the voltage level of the 3.3 V supply during power-up and power-down in order to guarantee protection against latch-up.
2. All digital inputs are 5 V tolerant except pin XIN.
3. $I_{OH}$, $I_{OL}$ = ±4 mA for pins SACLK, SCL, SDA, SDAT, SCLT, TCK, TDI, TRST, TMS, TDO, GPIO, UNCOR, PSYNC, OCLK, DEN and DO[7:0]. For all other pins, $I_{OH}$, $I_{OL}$ = ±2 mA.

## APPLICATION INFORMATION



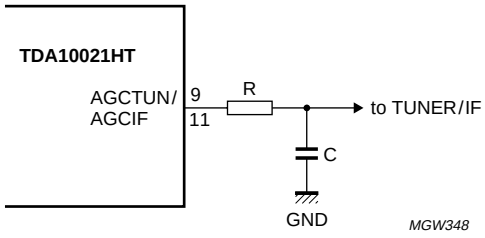

(1) Output 1 can be either a parallel output mode A, a parallel output mode B or a serial output (programmable interface).
(2) Output 2 is a serial output (serial interface).

Fig.2 Front-end receiver schematic.




(1) Typical XTAL is at fundamental frequency (typically 4 Mhz).
(2) Values of passive components are dependant on XTAL manufacturer (typically R = 1 MΩ, C1 = C2 = 56 pF).

Fig.3 Typical XTAL connection.




R and C are chosen to verify $\frac{SR}{1024} < f_c < \frac{XIN}{16}$ with R = 1.5 kΩ and C = 1 nF, $f_c$ = 100 kHz.

Fig.4 External AGC connection.

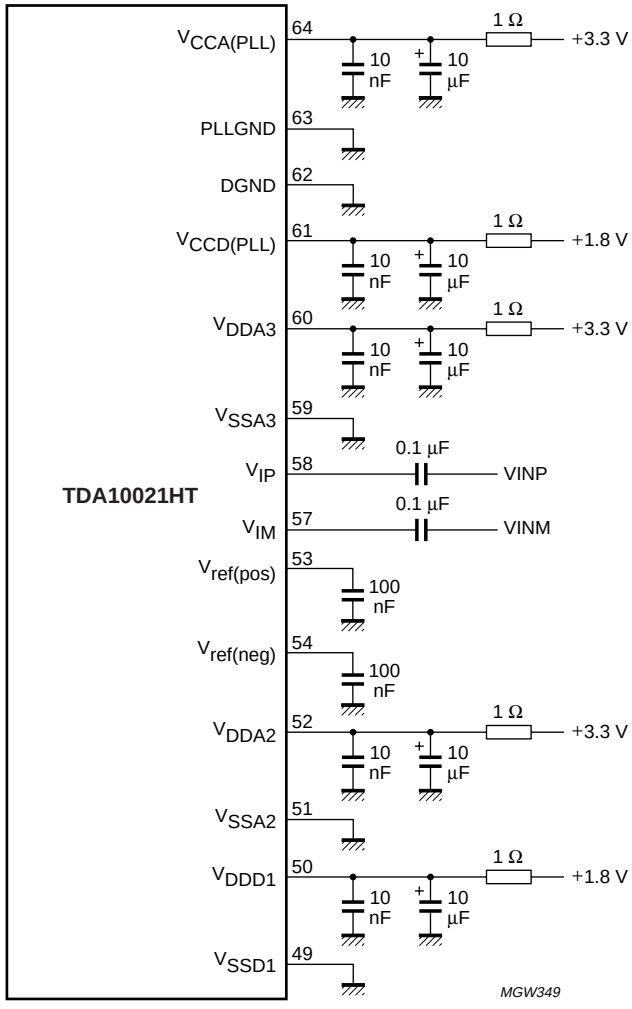
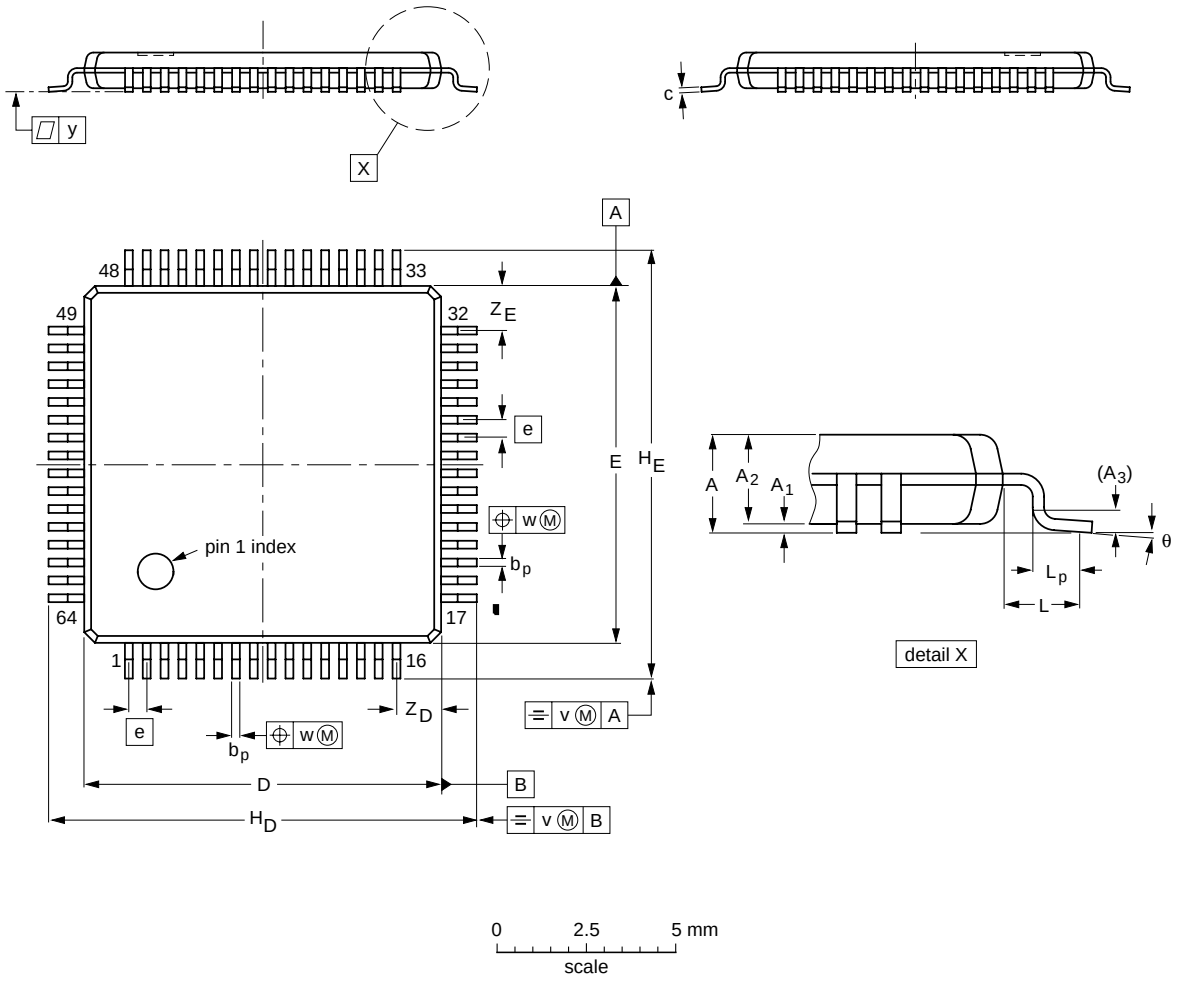



Fig.5 PLL and ADC connections.

**PACKAGE OUTLINE**

**TQFP64: plastic thin quad flat package; 64 leads; body 10 x 10 x 1.0 mm** **SOT357-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.15<br>0.05 | 1.05<br>0.95 | 0.25 | 0.27<br>0.17 | 0.18<br>0.12 | 10.1<br>9.9 | 10.1<br>9.9 | 0.5 | 12.15<br>11.85 | 12.15<br>11.85 | 1.0 | 0.75<br>0.45 | 0.2 | 0.08 | 0.1 | 1.45<br>1.05 | 1.45<br>1.05 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT357-1 | 137E10 | MS-026 | | | | ~~99-12-27~~<br>00-01-19 |

## SOLDERING

### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

**Suitability of surface mount IC packages for wave and reflow soldering methods**

| PACKAGE | SOLDERING METHOD | |
|---|---|---|
| | WAVE | REFLOW(1) |
| BGA, HBGA, LFBGA, SQFP, TFBGA | not suitable | suitable |
| HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS | not suitable(2) | suitable |
| PLCC(3), SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended(3)(4) | suitable |
| SSOP, TSSOP, VSO | not recommended(5) | suitable |

**Notes**

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

**DATA SHEET STATUS**

| DATA SHEET STATUS(1) | PRODUCT STATUS(2) | DEFINITIONS |
|---|---|---|
| Objective specification | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| Product specification | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A. |

**Notes**

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

## DEFINITIONS

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## DISCLAIMERS

**Life support applications** — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes** — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

**ICs with MPEG-2 functionality** — Use of this product in any manner that complies with the MPEG-2 Standard is expressly prohibited without a license under applicable patents in the MPEG-2 patent portfolio, which license is available from MPEG LA, L.L.C., 250 Steele Street, Suite 300, Denver, Colorado 80206.

## PURCHASE OF PHILIPS I²C COMPONENTS


Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

# *Philips Semiconductors – a worldwide company*

**Contact information**

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.



Printed in The Netherlands 753504/04/pp16 Date of release: 2001 Oct 01 Document order number: 9397 750 08497

Let's make things better.

Philips
Semiconductors

PHILIPS