TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC164AP, TC74HC164AF, TC74HC164AFN

8 – BIT SHIFT REGISTER (S – IN, P – OUT)

(Note) The JEDEC SOP (FN) is not available in Japan.

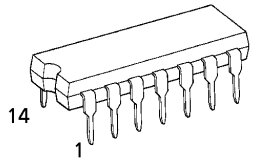
The TC74HC164A is a high speed CMOS 8 - BIT SERIAL - IN PARALLEL - OUT SHIFT REGISTER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

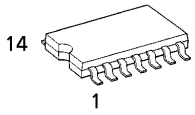
It consists of a serial - in, parallel - out 8 - bit shift register with a CK input and an overriding $\overline{CLR}$ input.

Two serial data inputs (A, B) are provided so that one may be used as a data enable.

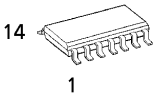
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P (DIP14-P-300-2.54)
Weight : 0.96g (Typ.)



F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)

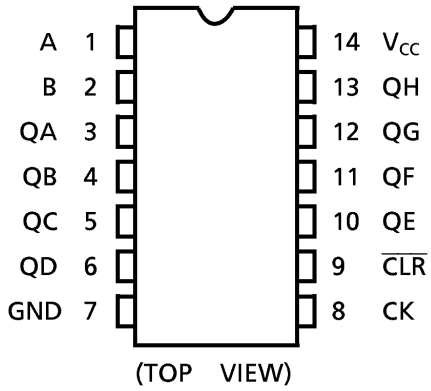


FN (SOL14-P-150-1.27)
Weight : 0.12g (Typ.)

FEATURES :

- High Speed ····· f_{MAX} = 58MHz (typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ···· V_{CC} (opr.) = 2V ~ 6V
- Pin and Function Compatible with 74LS164

PIN ASSIGNMENT



(TOP VIEW)

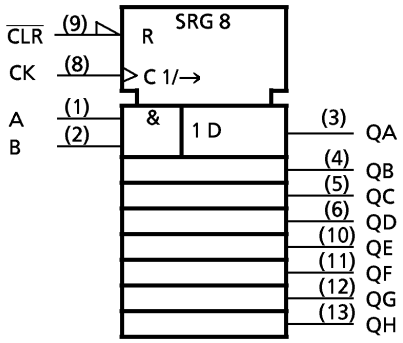
TRUTH TABLE

INPUTS				OUTPUTS			
$\overline{CLR}$	CK	SERIAL IN					
		A	B	QA	QB	···	QH
L	X	X	X	L	L	···	L
H	↓	X	X	NO CHANGE			
H	↑	L	X	L	QA_n	···	QG_n
H	↑	X	L	L	QA_n	···	QG_n
H	↑	H	H	H	QA_n	···	QG_n

X : Don't Care

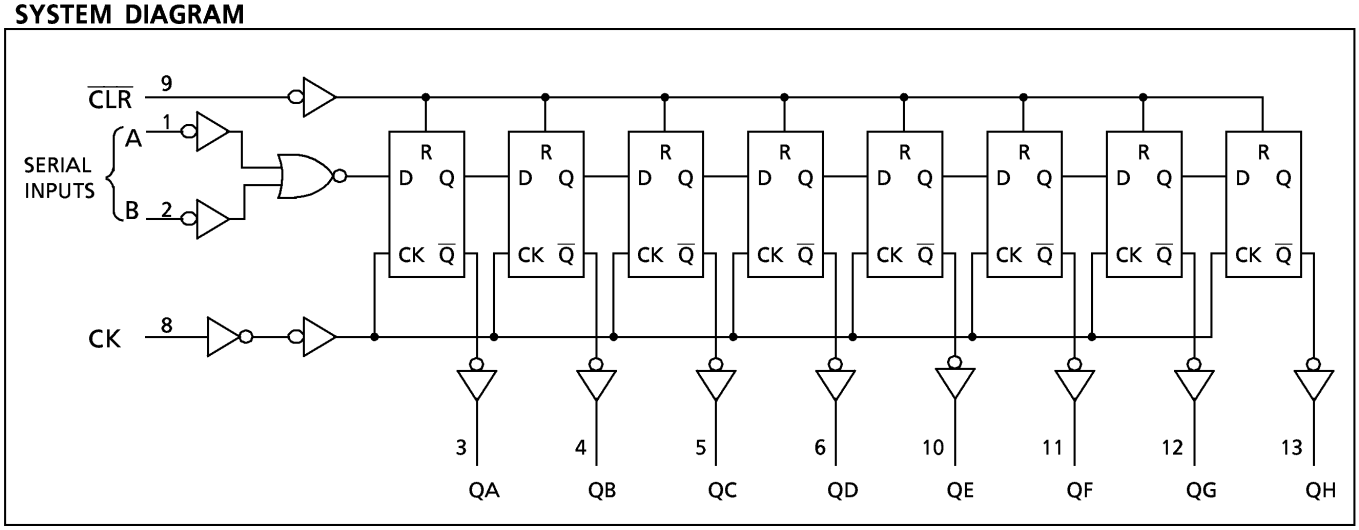
$QA_n \sim QG_n$: The level of QA ~ QG, respectively, before the most recent positive edge of clock.

IEC LOGIC SYMBOL

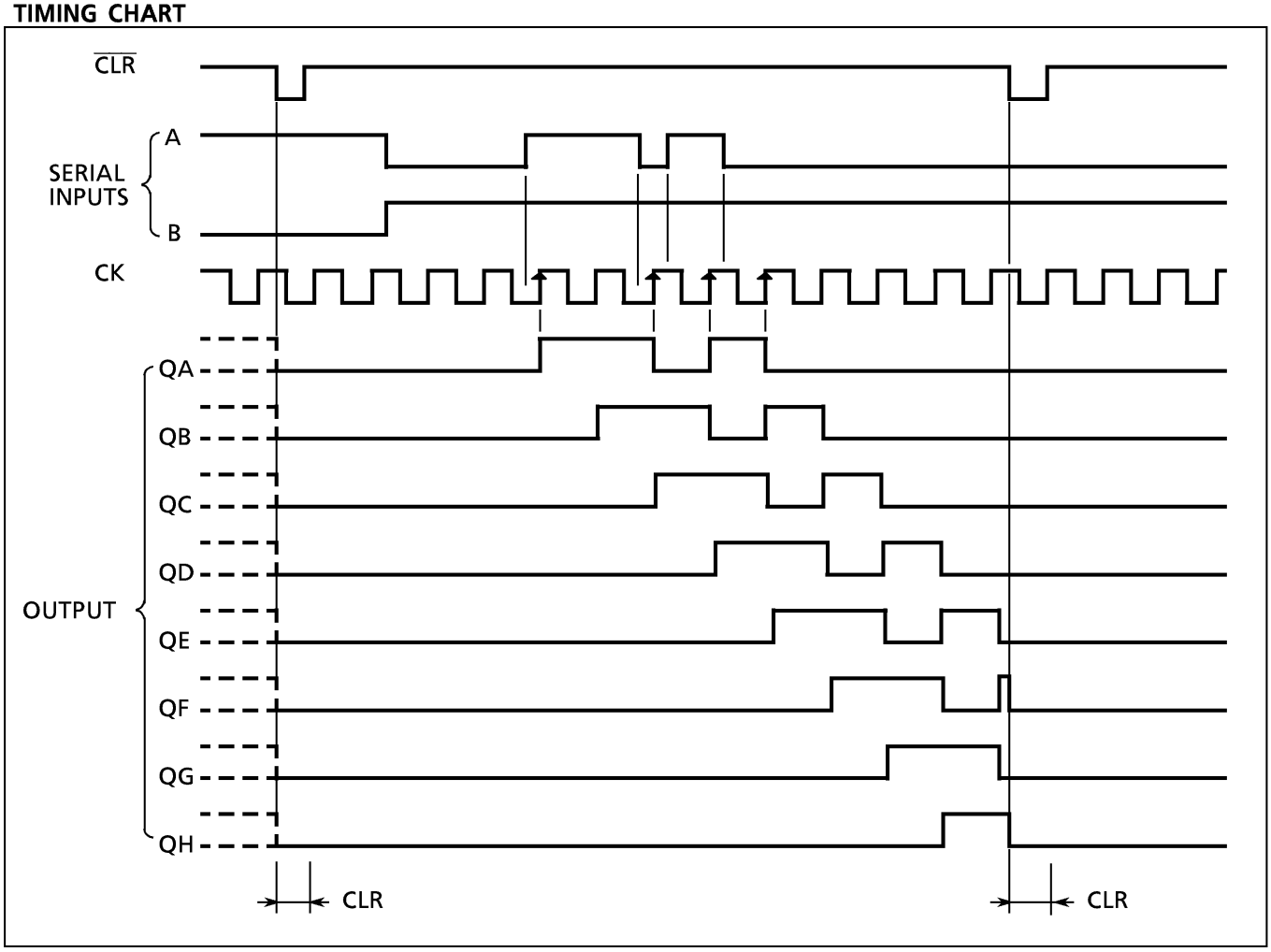


980508EBA2

SYSTEM DIAGRAM



TIMING CHART



980508EBA2'

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} / Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta = −40°C~65°C. From Ta = 65°C to 85 °C a derating factor of −10mW/ °C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	t_r, t_f	0~ 1000 (V_{CC} = 2.0V) 0~ 500 (V_{CC} = 4.5V) 0~ 400 (V_{CC} = 6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
			I_{OH} = −4 mA I_{OH} = −5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I_{OL} = 4 mA I_{OL} = 5.2mA	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C TYP.	Ta = 25°C LIMIT	Ta = −40~85°C LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		2.0 4.5 6.0	− − −	75 15 13	95 19 16	ns
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$		2.0 4.5 6.0	− − −	80 16 14	100 20 17	
Minimum Set−up Time (A, B)	t_s		2.0 4.5 6.0	− − −	50 10 9	65 13 11	
Minimum Hold Time (A, B)	t_h		2.0 4.5 6.0	− − −	5 5 5	5 5 5	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		2.0 4.5 6.0	− − −	5 5 5	5 5 5	
Clock Frequency	f		2.0 4.5 6.0	− − −	6 31 36	5 25 29	MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 15pF$, $V_{CC} = 5V$, Ta = 25°C, Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CK−Qn)	t_{pLH} t_{pHL}		−	15	27	
Propagation Delay Time ($\overline{CLR}$−Qn)	t_{pHL}		−	16	30	
Maximum Clock Frequency	f_{MAX}		33	58	−	MHz

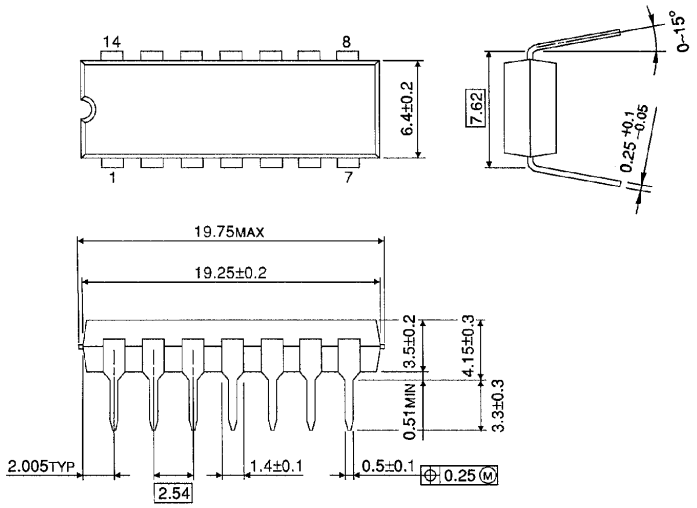
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0 4.5 6.0	− − −	25 7 6	75 15 13	− − −	95 19 16	ns
Propagation Delay Time (CK−Qn)	t_{pLH} t_{pHL}		2.0 4.5 6.0	− − −	57 19 16	160 32 27	− − −	200 40 34	
Propagation Delay Time ($\overline{CLR}$−Qn)	t_{pHL}		2.0 4.5 6.0	− − −	60 20 17	175 35 30	− − −	220 44 37	
Maximum Clock Frequency Frequency	f_{MAX}		2.0 4.5 6.0	6 31 36	18 53 62	− − −	5 25 29	− − −	MHz
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD} (1)			−	107	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

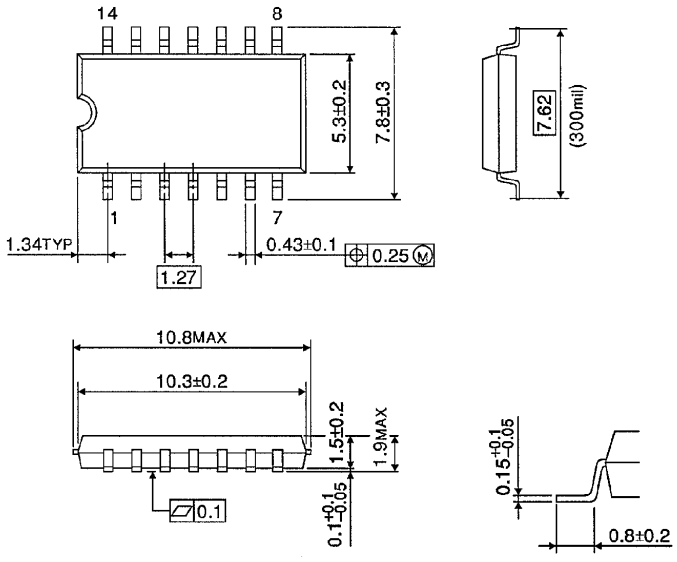
$$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 14PIN OUTLINE DRAWING (DIP14-P-300-2.54) Unit in mm



Weight : 0.96g (Typ.)

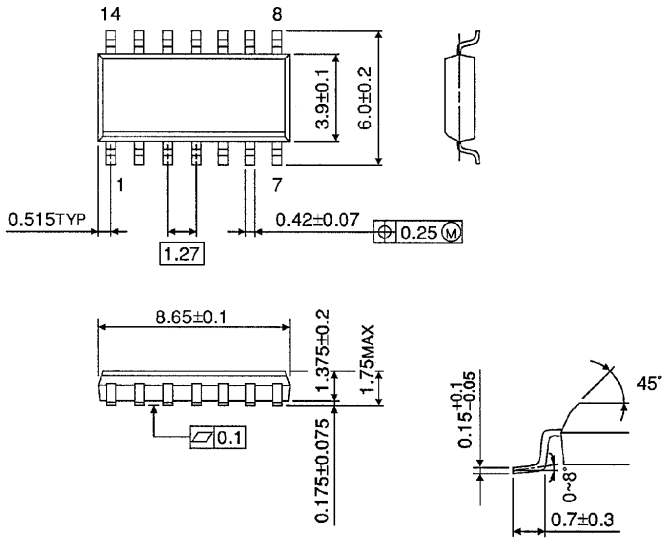
SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150 -1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)