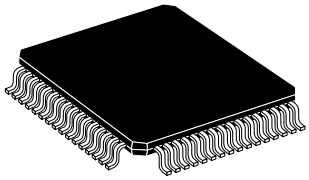
# STV0299B

## QPSK/BPSK LINK IC

- **MULTISTANDARD QPSK AND BPSK DEMODULATION**
- **EASY IMPLEMENTATION WITH LOW COST DIRECT CONVERSION TUNERS**
- **EXTREMELY LOW BER WHEN CO-CHANNEL INTERFERENCE**
- **WIDE CARRIER LOOP TRACKING RANGE TO COMPENSATE FOR DISH FREQUENCY DRIFT**
- **COMMON INTERFACE COMPLIANT**
- **VERY LOW POWER CONSUMPTION**
- INTEGRATED DUAL 6-BIT ANALOG TO DIGITAL CONVERTERS
- DUAL DIGITAL AGC
- DIGITAL NYQUIST ROOT FILTER WITH ROLL-OFF OF 0.35 OR 0.20
- DIGITAL CARRIER LOOP WITH LOCK DETECTOR, ON-CHIP WIDE RANGE DEROTATOR AND TRACKING LOOP (TYP ± 45 MHz)
- DIGITAL TIMING RECOVERY WITH LOCK DETECTOR
- CHANNEL BIT RATE UP TO 90 Mbps AND SYMBOL FREQUENCY RATE FROM 1 TO 50 MSYMBOLS
- INNER DECODER:
  - VITERBI SOFT DECODER FOR CONVOLUTIONAL CODES, M=7, RATE 1/2
  - PUNCTURED CODES 1/2, 2/3, 3/4, 5/6, 6/7 AND 7/8
- SYNCHROWORD EXTRACTION
- CONVOLUTIVE DEINTERLEAVER
- OUTER DECODER:
  - REED-SOLOMON DECODER FOR 16 PARITY BYTES; CORRECTION OF UP TO 8 BYTE ERRORS
  - ENERGY DISPERSAL DESCRAMBLER
- ON-CHIP FLEXIBLE CLOCK SYSTEMS TO ALLOW USE OF EXTERNAL CLOCK SIGNALS IN 4 MHz TO 30 MHz RANGE
- EASY-TO-USE C/N ESTIMATOR WITH 2 TO 18 dB RANGE
- $I^2C$ SERIAL BUS AND REPEATER
- DVB COMMON INTERFACE COMPLIANT PARALLEL OUTPUT FORMAT
- PARALLEL AND SERIAL DATA OUTPUT
- LNB SUPPLY CONTROL WITH STANDARD I/O, 22 KHz TONE AND DISEQC™ MODULATOR WITH TTL OUTPUT
- CMOS TECHNOLOGY: 2.5 V OPERATION; JEDEC (EIA/JESD8-5)



**TQFP64** (10 x 10 x 1.4 mm)
(Thin Plastic Quad Flat Pack)

**ORDER CODE:** STV0299B (**No Slug)**

### APPLICATIONS

- DIGITAL SATELLITE RECEIVER AND SET-TOP BOXES

### DESCRIPTION

The STV0299 Satellite Receiver with FEC is a CMOS single-chip multistandard demodulator for digital satellite broadcasting. It consists of two A/D converters for I-input and Q-input, a multistandard QPSK and BPSK demodulator, and a forward error correction (FEC) unit having both an inner (Viterbi) and outer (Reed-Solomon) decoder.

The FEC unit is compliant with the DVB-S and DSS™ specifications. Processing is fully digital.

It integrates a derotator before the Nyquist root filter, allowing a wide range of offset tracking.

The high sampling rate facilitates the implementation of low-cost, direct conversion tuners.

A variety of configurations and behaviours can be selected through a bank of control/configuration registers via an $I^2C$. The chip outputs MPEG Transport Streams and interfaces seamlessly to the Packet Demultiplexers embedded in ST's ST20-TPx or STi55xx. High sampling frequency (up to 90MHz) considerably reduces the cost of LPF of direct conversion tuners.

The multistandard capability associated with a broad range of input frequency operations makes it easy-to-use. Its low power consumption, small package and optional serial output interface makes it perfect for embedding into a tuner.

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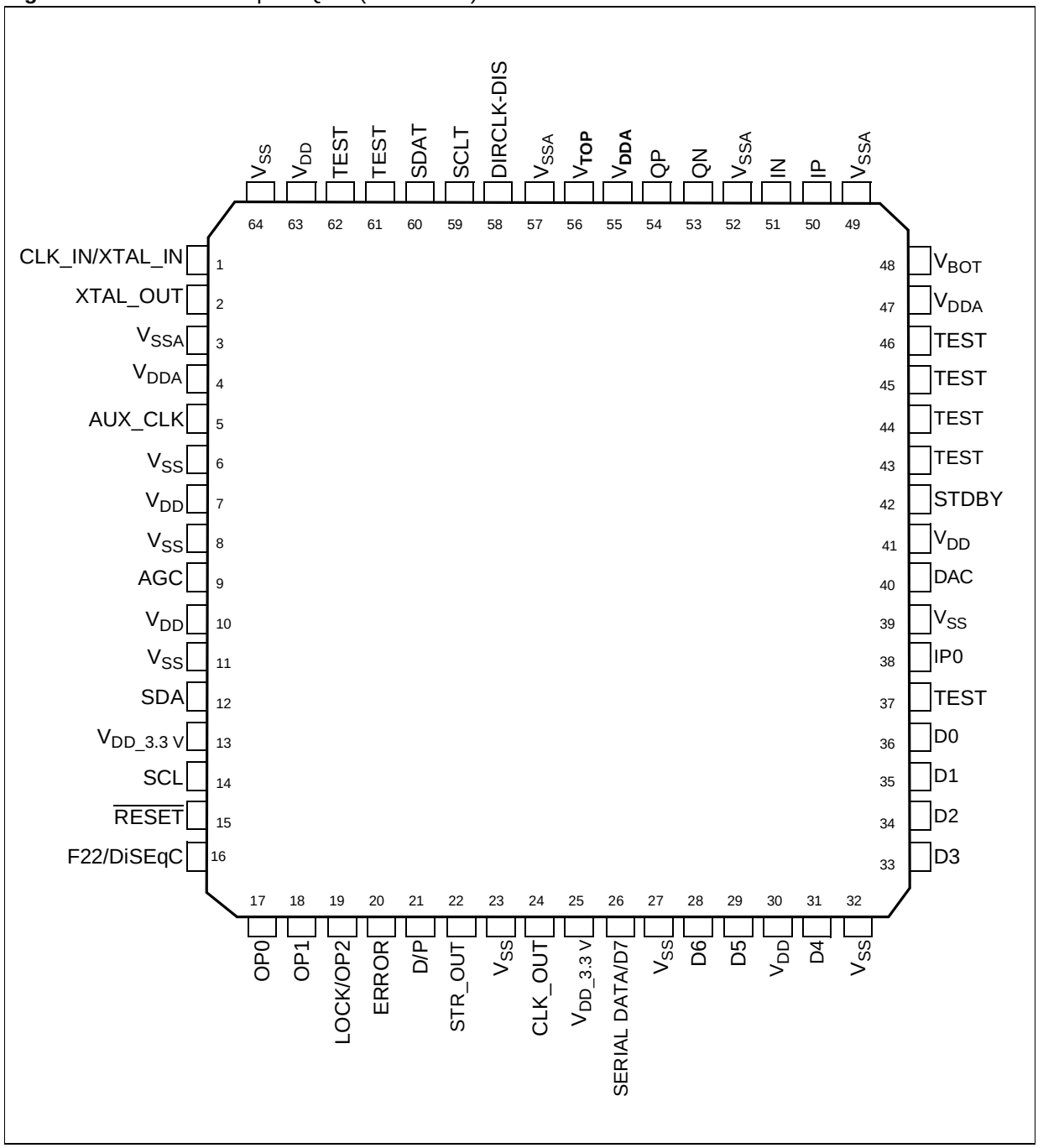
## 1 PIN INFORMATION

### 1.1 Pin Connections

**Figure 1:** Pinout for 64-pin TQFP (10x10 mm)



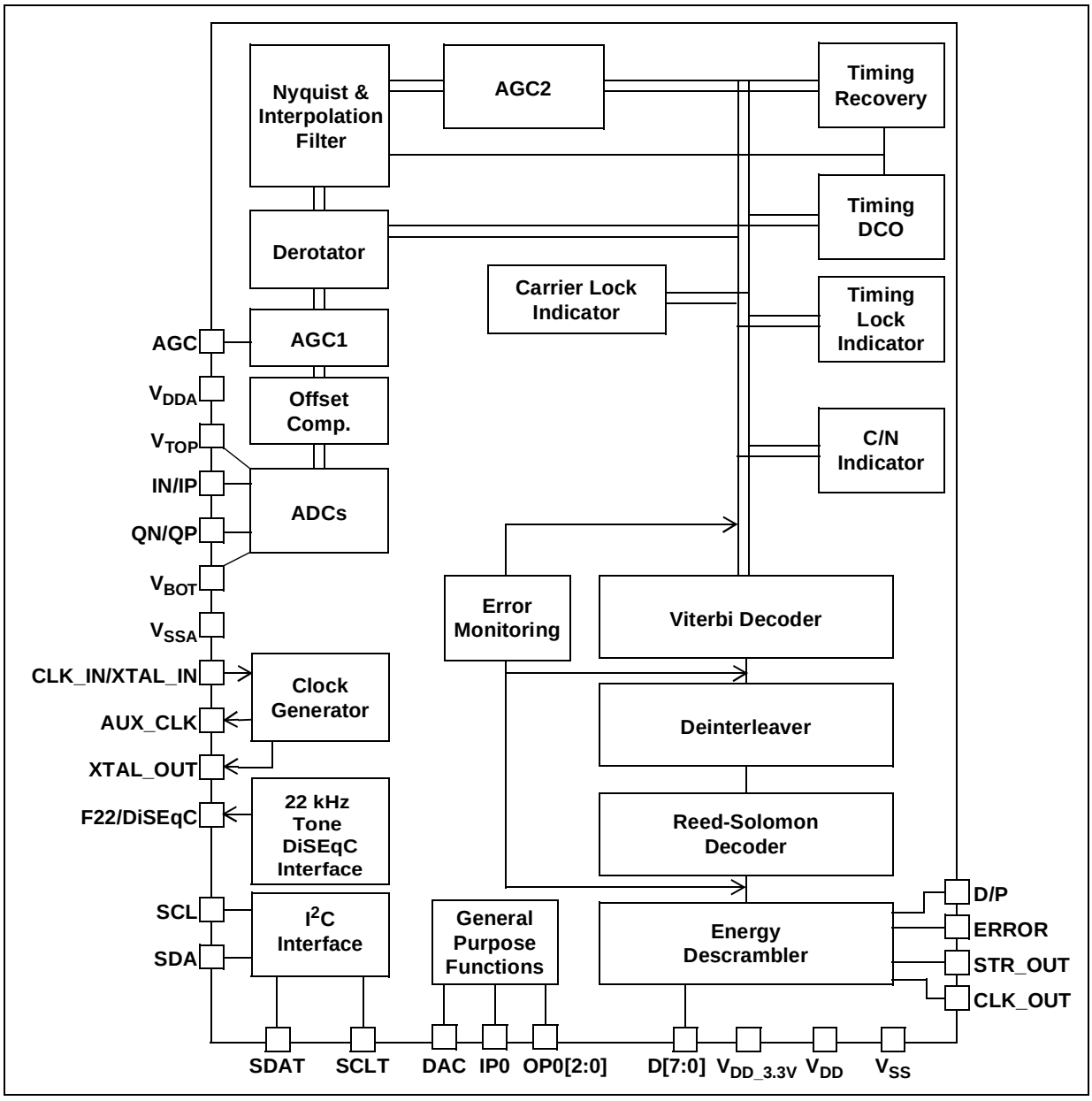
## 1 PIN INFORMATION (continued)

### 1.2 Pinout Description

| Pin Number | Name | I/O[1] | Description |
|---|---|---|---|
| **SIGNAL INPUTS** | | | |
| 50, 51 | IP, IN | I | Analog in Phase Component |
| 53, 54 | QN, QP | I | Analog in Quadrature Component |
| FRONT END CONTROLS | | | |
| 1 | CLK_IN/XTAL IN | I | Crystal Input or CLK_IN |
| 2 | XTAL OUT | O | Crystal Output |
| 9 | AGC | OD[3] | Control Signal to the Tuner |
| 5 | AUX_CLK | O[2] | Programmable Output Port or Programmable Output Clock |
| 17-18 | OP0, OP1 | O[2] | Programmable Output Ports |
| 19 | LOCK/OP2 | O[2] | Carrier Found or Data Found or Output Port |
| 38 | IP0 | I | Input Port |
| **SIGNAL OUPUTS** | | | |
| 26-28-29-31, 33 to 36 | D[7:0] | O[2] | Output Data; D7 is DATA_OUT in Serial Mode |
| 24 | CLK_OUT | O[2] | Output Byte Clock; or Bit Clock in Serial Mode |
| 22 | STR_OUT | O[2] | Output 1st byte Signal (synchro byte clock) |
| 21 | D/$\overline{P}$ | O[2] | Data/Parity Signal |
| 20 | ERROR | O[2] | Output Error Signal. Set in case of uncorrectible packet. |
| $I^2C$ INTERFACE | | | |
| 14 | SCL | I[3] | Serial Clock ($I^2C$ bus) |
| 12 | SDA | I/OD[3] | Serial Data ($I^2C$ bus) |
| **OTHERS** | | | |
| 59 | SCLT | OD[3] | Tuner Serial Clock (repeator) or Output Port |
| 60 | SDAT | I/OD[3] | Tuner Serial Data (repeator) or Input/Output Port |
| 37-43-44-45-46-61-62 | TEST | I | Reserved for manufacturing tests; must be tied to $V_{SS}$ |
| 58 | DIRCLK_DIS | I | Sets the DIRCLK function at power on |
| 3, 49, 52, 57 | $V_{SSA}$ | S | Analog Ground |
| 4, 47, 55 | $V_{DDA}$ | S | Analog 2.5 V Supply |
| 56 | $V_{TOP}$ | S | ADC High Voltage Reference |
| 48 | $V_{BOT}$ | S | ADC Low Voltage Reference |
| 6-8-11-23-27-32-39-64 | $V_{SS}$ | S | Ground |
| 13-25 | $V_{DD\_3.3\ V}$ | S | 3.3 V Supply |
| 7-10-30-41-63 | $V_{DD}$ | S | 2.5 V Supply |
| 15 | $\overline{RESET}$ | I | Reset, active at low level |
| 42 | STDBY | I | Sets STDBY at power on |
| 16 | F22/DiSEqC | O[2] | DiSEqC modulation, 22 kHz Tone, Programmable Output Port |
| 40 | DAC | O[2] | Programmable Digital to Analog Converter Output |

*Note:* *1* The following abbreviations are used: I - Input; O - Output; OD - Open drain output.
*2* 3.3 V output levels.
*3* 5 V tolerant

## 2 BLOCK DIAGRAM




## 3 SYSTEM CHARACTERISTICS

**Performances**

The following given parameters are for indication purposes only.

**Carrier Loop Tracking Range:**

- $\pm f_{M\_CLK}/2$

**Carrier Loop Capture Range (C/N>=4 dB):**

- up to ± 5% fs in less than 100 Ksymbols
- up to ± 2% fs in less than 10 Ksymbols

C/N Threshold (lowest C/N at which capture is possible) = 1 dB.

**Timing Loop Capture Range (C/N>=2 dB):**

- up to ±250 ppm in less than 100 Ksymbols
- conventions used for the above characteristics are:

$f_{sampling} = f_{m\_clk} = f_{master\_clock}$

$f_S = f_{symbol}$

$$C/N = \text{Carrier/Noise} = \frac{Eb}{No} x 2 x PR$$

PR = Puncture Rate

# 4 FUNCTIONAL DESCRIPTION

The STV0299B is a multistandard demodulator and error correction decoder IC for the reception of QPSK and BPSK modulated signals. It is intended for use in digital satellite television applications. The IC can accept two standards of QPSK modulated signals (DVB and DSS) as well as BPSK modulated signals over a wide symbol frequency range (from 1 to 50 Msymbols/s). The signals are digitized via an integrated dual 6-bit analog to digital converter, and interpolated and digitally filtered by a Nyquist root filter (with a settable roll-off value of either 0.35 or 0.20).

There are two built-in digital Automatic Gain Controls (AGCs). The first AGC allows the tuner gain to be controlled by the pulse density modulated output. The second AGC performs power optimization of the digital signal bandwidth (internal to the STV0299B). The digital signal then passes through the digital carrier loop fitted with an on-chip derotator and tracking loop, lock detector, and digital timing recovery.

Forward error correction is integrated by way of an inner Viterbi soft decoder, and an outer Reed-Solomon decoder.

## 4.1 Front End Interfaces

### 4.1.1 I²C Interface

The standard I²C protocol is used whereby the first byte is Hex D0 for a write operation, or Hex D1 for a read operation. The I²C interface operates differently depending on whether it is in normal or standby mode.

### 4.1.2 Write Operation (Normal Mode)

The byte sequence is as follows:

1 The first byte gives the device address plus the direction bit (R/W = 0).
2 The second byte contains the internal address of the first register to be accessed.
3 The next byte is written in the internal register. Following bytes (if any) are written in successive internal registers.
4 The transfer lasts until stop conditions are encountered.
5 The STV0299B acknowledges every byte transfer.

### 4.1.3 Read Operation (Normal Mode)

The address of the first register to read is programmed in a write operation without data, and terminated by the stop condition. Then, another start is followed by the device address and R/W = 1. All following bytes are now data to be read at successive positions starting from the initial address. Figure 2 shows the I²C Normal Mode Write and Read Registers.

### 4.1.4 I²C Interface in Standby Mode

Only three registers can be addressed while in standby mode: RCR (address 01 Hex), MCR (address 02 Hex) and ACR (address 03 Hex). These three registers can be either read or written to (refer to Figure 3).

Only one register may be read or written to per sequence (no increment). While in standby mode, the Serial Clock (SCL) frequency must be lower than one tenth of the CLK_IN frequency ($f_{CLK\_IN}$ / 10).

**Figure 2:** I²C Read and Write Operations in Normal Mode

**Write registers 0 to 3 with AA, BB, CC, DD**

| Start | Device Address, Write D0 | ACK | Register Address 00 | ACK | Data AA | ACK | Data BB | ACK | Data CC | ACK | Data DD | ACK | Stop |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**Read registers 2 and 3**

| Start | Device Address, Write D0 | ACK | Register Address 02 | ACK | Stop |
|---|---|---|---|---|---|

| Start | Device Address, Read D1 | ACK | Data Read CC | ACK | Data Read DD | $\overline{ACK}$ | Stop |
|---|---|---|---|---|---|---|---|

**Figure 3:** I²C Read and Write Operations in Standby Mode

**Write operation**

| Start | Device Address, Write D0 | ACK | Register Address 01, 02 or 03 | ACK | Data | ACK | Stop |
|---|---|---|---|---|---|---|---|

**Read operation**

| Start | Device Address , Read D0 | ACK | Register Address | ACK | Stop |
|---|---|---|---|---|---|

| Start | Device Address, Read D1 | ACK | Reader Data | ACK (or no ACK[1]) | Stop |
|---|---|---|---|---|---|

*Note: 1* ACK is not absolutely necessary after Data

## 4 FUNCTIONAL DESCRIPTION (continued)

### 4.1.5 Specific Concerns about SCL Frequency

For reliable operation in Normal Mode, the SCL frequency must be lower than 1/40 of the Master Clock (M_CLK) frequency. Consequently, care should be taken to observe the following:

1 Before returning to Normal Mode from Standby Mode, the M_CLK frequency must be selected such that $f_{M\_CLK} \geq 40\ f_{SCL}$

2 After Power-on reset signal, the STV0299B operates in Normal Mode. There are two possible cases:

- DIRCLK-DIS (pin 58) is grounded. M_CLK = CLK_IN, the $f_{SCL}$ frequency of the $I^2C$ bus must satisfy: $\mathbf{f_{SCL}} \leq \frac{CLK\_IN}{40}$ .
- DIRCLK-DIS (pin 58) is tied to $V_{DD}$ (where $\mathbf{f_{M\_CLK}} = \frac{100}{16} \cdot \mathbf{f_{CLK\_IN}}$), and the $f_{SCL}$ frequency of the $I^2C$ bus must satisfy: $\mathbf{f_{SCL}} \leq \frac{100}{16 \times 40} \cdot CLK\_IN$ and $\mathbf{f_{SCL}} \leq 400$ kHz. For example, this second operating mode is required when the application features both a 4 MHz XTAL and a 400 kHz $I^2C$ bus.

### 4.1.6 Identification Register

The Identification Register (at address Hex 00) gives the release number of the circuit.

The content of this register at reset is presently A1 (same as STV0299).

### 4.1.7 Sampling Frequency

The STV0299B converts the analog inputs into digital 6-bit I and Q flows. The sampling frequency is $f_{M\_CLK}$ which is derived from an external reference described in Section 4.1.8 *'Clock Generation'*. The maximum value of $f_{M\_CLK}$ is 90 MHz.

The sampling causes the repetition of the input spectrum at each integer multiple of $f_{M\_CLK}$. One has to ensure that no frequency component is folded in the useful signal bandwidth of $f_S(1+\alpha)/2$ where $f_S$ is the symbol frequency, and $\alpha$ is the roll-off value.

### 4.1.8 Clock Generation

An integrated VCO (optimised to run in the range of 300 to 400 MHz) is locked to a reference frequency provided by a crystal oscillator by the following relation:

$$\mathbf{f_{VCO}} = \mathbf{f_{ref}} \cdot \mathbf{4} \cdot (\mathbf{M} + \mathbf{1}) = \mathbf{f_{XTAL}} \cdot \mathbf{4} \cdot \frac{\mathbf{M} + \mathbf{1}}{\mathbf{K} + \mathbf{1}}$$

The VCO's loop filter is optimized for a reference frequency between 4 and 8 MHz.

The VCO generates the following by division:

- The Master Clock (M_CLK)
- An auxiliary clock (AUX_CLK) which may either be in the MHz range or in the 25 Hz to 1500 Hz range for some specific LNB control (for example, 60 Hz).
- A lower frequency, F22, typically 22 KHz, needed for LNB control or DiSEqC™ control.

When DIRCLK_CTRL = 1, the crystal signal is routed directly to M_CLK; the VCO may still be used to generate AUX_CK and/or the F22 (used by the DiSEqC™ interface).

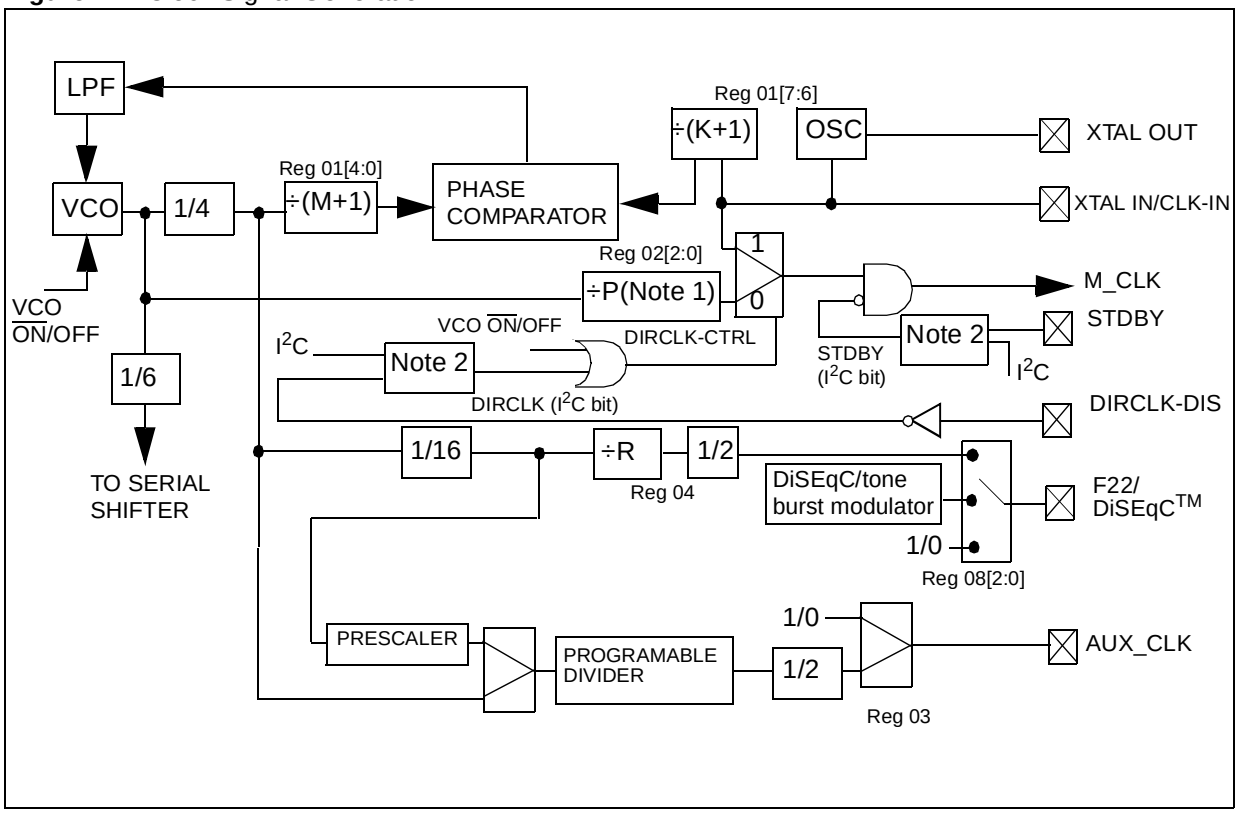
If the internal VCO is not used by any of the dividers, it may be stopped in order to decrease the power consumption and/or radiation emissions. The only guaranteed function in standby mode is the $I^2C$ Write/Read function of the three clock control registers.

There are restrictions on the high and low level durations, and on the crystal (or external clock) frequency when the direct clock is used.

These restrictions are explained in Section 4.1.5 *Specific Concerns about SCL Frequency*.

## 4 FUNCTIONAL DESCRIPTION (continued)

**Figure 4:** Clock Signal Generation




*Note: 1* Refer to the Register List P[2:0] in table 1

*2* At the rising edge of $\overline{\text{RESET}}$ signal (pin 15) the corresponding bit of the $I^2C$ bus register is forced to the status of pin STDBY or to DIRCLK-DIS.

**Table 1:** Divider Programming

| K(1:0) in register | $f_{REF} = f_{XTAL}$ divided by: |
|---|---|
| 00 | 1 |
| 01 | 2 |
| 10 | 3 |
| 11 | 4 |

| M(4:0) in register | $f_{VCO} = f_{REF}$ multiplied by: |
|---|---|
| 00000 | 4 |
| 00001 | 8 |
| 00010 | 12 |
| 00011 | 16 |
| ... | ... |
| 11111 | 128 |

| P(2:0) in register | $f_{M\_CLK} = f_{VCO}$ divided by P: |
|---|---|
| 000 | 4 |
| 001 | 6 |
| 010 | 8 |
| 011 | 12 |
| 100 | 16 |
| 101 | 24 |
| 110 | 32 |
| 111 | 48 |

**Table 2:** Summary of $F_{M\_CLK}$

| | |
|---|---|
| $f_{VCO} = f_{XTAL} \times 4 \cdot \frac{M+1}{K+1}$ | |
| $f_{M\_CLK} = \frac{f_{VCO}}{P}$ | DIRCLK_CTRL = 0 |
| $f_{M\_CLK} = f_{CLK\_IN}$ | DIRCLK_CTRL =1 |
| $f_{M\_CLK} = 0$ | STDBY = 1 |

## 4 FUNCTIONAL DESCRIPTION (continued)

### 4.1.9 Clock Registers

The Reference Clock, Master Clock, Auxiliary Clock and F22 Frequency Registers are in Addresses 01, 02, 03 and 04.

### 4.1.10 $I^2C$ Bus Repeater

In low symbol rate applications, signal pollution generated by the SDA/SCL lines of the $I^2C$ bus may dramatically worsen tuner phase noise. In order to avoid this problem, the STV0299B offers an $I^2C$ bus repeater so that the SDAT and SCLT are active only when necessary and muted once the tuner frequency has settled.

Both SDAT and SCLT pins are set high at reset. When the microprocessor writes a 1 into register bit $I^2CT$, the next $I^2C$ message on SDA and SCL is repeated on the SDAT and SCLT pins respectively, until stop conditions are detected.

To write to the tuner, the external microprocessor must, for each tuner message, perform the following:

- Program 1 in $I^2CT$.
- Send the message to the tuner.

Any size of byte transfers are allowed, regardless of the address, until the stop conditions are detected. Transfers are fully bi-directional.

The $I^2CT$ bit is automatically reset at the stop condition. If not used for the $I^2C$ repeater, both SDAT and SCLT outputs may be used as general purpose output ports.

SDAT status may be read on the DiSEqC register. Configuration is controlled by the $I^2C$ repeater register in Address 0Ah.

In the first version of the STV0299, operation of the repeater was very fast, and often too fast versus the rise time of the SDAT and SCLT signals. In the STV0299B, a programmable delay is implemented to accept a wide range of rise times on SDAT and SCLT. The delay is programmed with Reg.05 [5:4]. In practice, operation of the repeater is ensured in the following case:

- Reg.05 [5:4]: xx
- $f_{M\_CLK} \leq 90$ MHz
- RC$\leq$ 250ns (R: pull-up resistor, C: total capacitance on either SDAT or SCLT).

### 4.1.11 General Purpose $\Sigma\Delta$ DAC

A DAC is available in order to control external analog devices. It is built as a sigma-delta first-order loop, and has 12-bit resolution-it only requires an external low-pass filter (simple RC filter). The clock frequency is derived from the main clock by programmable division. The converter is controlled by two registers-one for clock divider control and 4 MSBs, and the other for the 8 LSBs.

If the DAC is not needed, the DAC output may be used as an output port. The DAC Registers are in Addresses 06 and 07.

### 4.1.12 DiSEqC Interface

This interface allows for the simplification of real time processing of the dialog from microprocessor to LNB. It includes a FIFO that is filled by the microprocessor via the $I^2C$ bus, and then transmitted by modulating the F22 clock adjusted beforehand to 22 kHz.

Two control signals are available on the $I^2C$ bus: FE (FIFO empty) and FF (FIFO full).

A typical byte transfer loop, as seen from the microprocessor, may be the following:

```
While (there is data to transfer)
1  Read the control signals
2  If FF=1, go to 1
3  Write byte to transfer in the FIFO
```

Note, for the above transfer loop, the following:

- At the beginning, the FIFO is empty (FE=1, FF=0). This is the idle state.
- As soon as a byte is written in the FIFO, the transfer will begin.
- After the last transmitted byte, the interface will go into the idle state.

**Modulation**

The output is a gated 22 kHz square signal.

- **In the idle state**, modulation is permanently inactive.
- **In byte transmission**, the byte is sent (MSB first) and is followed by an odd parity bit.
  A byte transmission is therefore a serial 9-bit transmission with an odd number of “1’s”.
  Each bit lasts 33 periods of F22 and the transmission is PWM-modulated.
  - **Transmission of “0’s”**. There are two submodes controlled by PortCtrl(2):
    a) PortCtrl2 = 1: Modulation is active during 22 pulses, then inactive during 11 pulses (2/3 PWM).
    b) PortCtrl2 = 0: Modulation is active during 33 pulses (3/3 PWM).
  - **Transmission of “1’s”**. During transmission of “1’s”, modulation is active during 11 pulses, then inactive during 22 pulses (1/3 PWM).

This is compatible with “Tone Burst” in older LNB protocols.

For the “Modulated Tone Burst”, only one byte (with value Hex FF) is written in the FIFO. The parity bit is 1, and as a result, the output signal is 9 bursts of 0.5 ms, separated by 8 intervals of 1 ms.

For the “Unmodulated Tone Burst” Port CTRL 2 is set to 0 and, only one byte, of value 00h is sent. The parity bit is still 1, and as a result, the signal is a continuous train of 12.5 ms. When the modulation is active, the DiSEqC output is driven alternatively to $V_{DD}$ and $V_{SS}$ levels. The DiSEqC and Lock Control, DiSEqC FIFO and DiSEqC Status Registers are in Addresses 08, 09 and 0Ah.

**Figure 5:** Schematic showing Bit Transmission

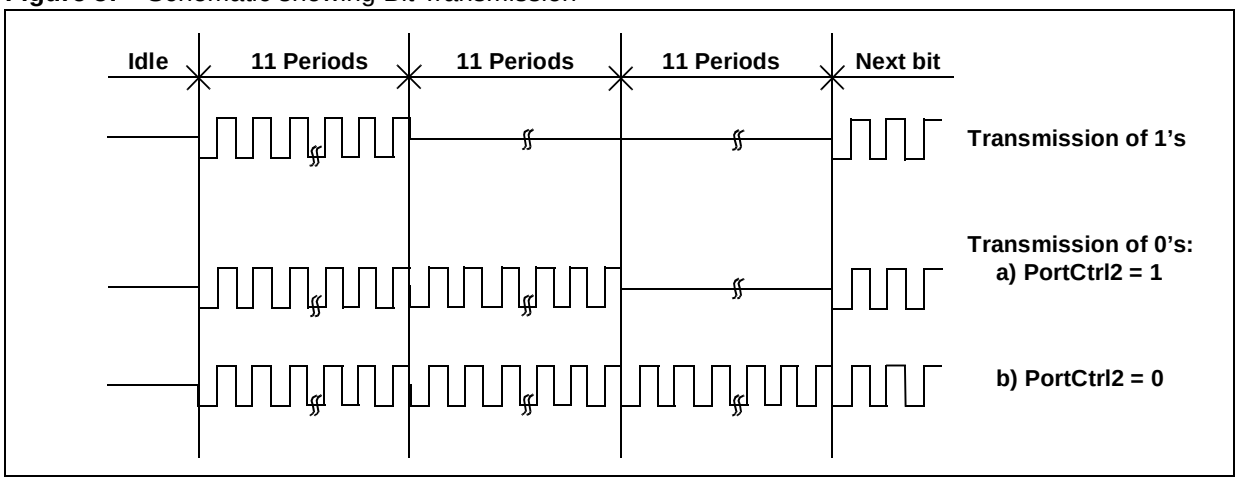



**Table 3:**

| PortCtrl (1:0) | PortCtrl (2) | FIFO | Output |
|---|---|---|---|
| 00 | X | empty | 0 |
| 01 | X | empty | 1 |
| 10 | 0 | DATA = 00 | Unmodulated tone burst |
| | 1 | DATA = FFor00 | Modulated tone burst |
| | 1 | Note 1 | DiSEqC signal |
| 11 | X | XX | Continuous tone |

*Note: 1* Byte to transfer in DiSEqC mode.
*2* In mode PortCtrl (1:0)=10, the $F_{22}$/DiSEqC pin returns to High -2 mode once the transmission is completed.

### 4.1.13 Standby Mode

A low power consumption mode (standby mode) can be implemented (in this mode, $f_{M\_CLK} = 0$). In standby mode, the $I^2C$ decoder still operates, but with some restrictions (see Sections *4.1.4* and *4.1.5*).

Standby mode can be initiated or stopped by $I^2C$ bus commands as described in MCR Register 02.

At power-on, the circuit starts to operate in standby mode when the STDBY pin (pin 42) is tied to $V_{DD}$. This guarantees low power consumption for the stand-alone modules (PCMCIA size front-end modules) before any command is initiated. After the power-on sequence, the standby mode is entirely controlled via MCR Register (02).

## 4 FUNCTIONAL DESCRIPTION (continued)

### 4.2 Signal Processing

#### 4.2.1 I and Q Inputs

The ADC features differential inputs, but in most applications I & Q signals are single-ended. In such applications, I and Q signals from the tuner are fed to the respective IP and QP inputs through a capacitor. The $I_N$ and $Q_N$ pins are DC biased, typically to $V_{BOT}$.The internal biasing of the ADC is done on the circuit at the mid-voltage between $V_{TOP}$ and $V_{BOT}$.

The Input/Output Configuration Register is described in Address 0Ch.

#### 4.2.2 Main AGC (or AGC1)

The modulus of the I/Q input is compared to a programmable threshold, m1, and the difference is integrated. This signal is then converted into a pulse density modulation signal to drive the AGC output. It should be filtered by a simple analog filter to control the gain command of any amplifier before the A to D converter.

The output converter operates at $f_{M\_CLK}/8$ in order to decrease the radiated noise and to simplify the filter design. The output is a 5 V tolerant open drain stage.

The reset value of the coefficient allows an initial settling time of less than 100k master clock periods.

The 8 integrator MSBs may be read or written at any time by the microprocessor. When written, the LSB's are reset and the coefficient may be set to zero by programming (in this case, the AGC is reduced to a programmable 8-bit voltage synthesizer).

The time constant of agc1 is estimated as followed:

$$T_{agc1} = \frac{2^{26-\beta_{agc1}}}{m1} \times T_{M\_CLK}$$

with m1 = AGC1 reference level.

The AGC1 Control, AGC1 Reference and AGC1 Integrator Registers are in Addresses 0D and 0F.

#### 4.2.3 Nyquist Root and Interpolation Filters

Two roll off values are available: 0.35 and 0.20. Refer to the Input/Output Configuration Register in Address 0C.

#### 4.2.4 Offset Cancellation

This device suppresses the residual DC component on I and Q. The compensation may be frozen to its last value by resetting the DC offset compensation bit in the AGC Control Register in Address 0D.

#### 4.2.5 Signal AGC (or AGC2)

The rms value of I and Q is measured after the Nyquist filter and compared to a programmable value, m2, such as that of the main AGC.

The integrated error signal is applied to a multiplier on each I and Q path.

The AGC2 Control Register is in Address 10.

Bits [7:5] give the AGC2 coefficient, which sets beta_agc2, the gain of the integrator. Table 4 shows how beta_agc2 is programmed with AGC2 coefficient (which is related to the time constant of the AGC).

**Table 4:**

| AGC2 Coefficient | beta_agc2 |
|---|---|
| 0 | 0 |
| 1 | 1 |
| 2 | 4 |
| 3 | 16 |
| 4 | 64 |
| 5 | 256 |
| 6 | N/A |
| 7 | N/A |

If AGC2 Coefficient = 0, the gain remains unchanged from its last value.

The time constant is independent of the symbol frequency, however it does depend on the modulus, m1, of the input signal, programmed in AGC1, with the following approximate relation:

$$T_{agc2} = \frac{60 \times 10^3 \cdot T_{M\_CLK}}{m1 \cdot beta\_agc2}$$

The AGC2 Integrator Registers (2 bytes - MSB and LSB) are in Addresses 18 and 19. These values may be read or written by the microprocessor. When written, all the LSB's integrator bits are reset. This value is an image of the signal power in the useful band. Compared with the total power of the signal, the out-of-band power may be computed (noise, or other channel).

## 4 FUNCTIONAL DESCRIPTION (continued)

### 4.3 Timing Recovery

#### 4.3.1 Timing Control

The loop is parametrized by two coefficients: alpha_tmg and beta_tmg. alpha_tmg can take values from 0 to 4, and beta_tmg from 0 to 7 (Register 0E).

When the parameter is 0, the actual coefficient value is zero. The 8 MSBs of the frequency accumulator may be read or written at any time by the $I^2C$ bus—when written, all LSBs are reset.

The Symbol Frequency Registers (MSB, Middle Bits and LSB) are in Addresses 1F, 20 and 21. These must be programmed with the expected symbol frequency.

The units are:

$$\frac{f_{M\_CLK}}{2^{20}}$$

Write mode is effective when writing the Middle Bit Register. The MSB Register must be loaded before the Middle Bit Register.

The value of the Timing Frequency Register, when the system is locked, is an image of the frequency offset. The unit is $f_S/2^{19}$ (approx. 2 ppm). It should be as close as possible to 0 (by adjusting symbol frequency register value) in order to have a symmetrical capture range. Reading it allows for optimal trimming of the timing range (Register 1A).

The actual symbol frequency is:

$$f_{S_{act}} = \frac{(f_{M\_CLK} \cdot f_{s\_reg}) + (2 \cdot f_s \cdot T_{mg\_reg})}{2^{20}}$$

where $f_{s\_reg}$ is the content of the symbol frequency register and $T_{mg\_reg}$ the content of the timing frequency register.

#### 4.3.2 Loop Equation

The timing loop may be considered as a second order loop. The natural frequency and the damping factor may be calculated using the following formula:

$$f_n = 5.2 \cdot 10^{-6} f_S \sqrt{m2 \cdot \beta}$$

where, $f_S$ is the symbol frequency, m2 is the AGC2 reference level and $\beta$ is programmed by the timing register:

$$\beta = 2^{beta\_tmg}$$

The damping factor is:

$$\xi = \frac{0.134 \cdot \sqrt{m2} \cdot 2^{alpha\_tmg}}{\sqrt{2^{beta\_tmg}}}$$

where m2 is the reference level of the AGC2 register.

Table 5 shows the natural frequency in DVB, with nominal reference level m2 = 20, for different values of beta_tmg and alpha_tmg, without noise.

#### 4.3.3 Timing Lock Indicator

The timing lock indicator reports a value dependent upon the signal-to-noise ratio and on the signal lock state.

With an AGC2 Reference level m2 = 20, if the timing lock indicator is above 48, the timing is locked; if it is above 42, this shows that a QPSK signal is present, either locked with low C/N (<3.6 dB) or unlocked with higher C/N; the ambiguity may be solved by changing on purpose the timing frequency of 1%; if it was locked before, the indicator should be now under 42.

The indicator needs 30K symbols for stabilization from unlock to lock after a frequency change.

The timing lock registers - the Timing Lock Setting Register and the Timing Lock Indicator Register - are in Addresses 11 and 17.

**Table 5:**

| | **alpha_tmg** | **1** | **2** | **3** | **4** |
|---|---|---|---|---|---|
| **beta_tmg** | **Natural Frequency for $f_S$ = 20 Mbaud** | **Damping Factor** | | | |
| 1 | 0.66 kHz | 0.85 | 1.70 | 3.38 | 6.77 |
| 2 | 0.93 kHz | 0.60 | 1.20 | 2.40 | 4.80 |
| 3 | 1.32 kHz | 0.42 | 0.85 | 1.70 | 3.38 |
| 4 | 1.86 kHz | 0.30 | 0.60 | 1.20 | 2.40 |
| 5 | 2.63 kHz | 0.21 | 0.42 | 0.85 | 1.70 |
| 6 | 3.72 kHz | 0.15 | 0.30 | 0.60 | 1.20 |
| 7 | 5.26 kHz | 0.10 | 0.21 | 0.42 | 0.85 |

## 4 FUNCTIONAL DESCRIPTION (continued)

### 4.4 Carrier Recovery and Derotator Loop

The tracking range of the derotator is $\pm f_{M\_CLK}/2$ ($\pm f_{sampling}/2$). The initial frequency search may therefore be performed on several MHz ranges without reprogramming the tuner.

Three phase detectors are selectable using software:

- Phase detector algorithm 0: This algorithm should only be used for BPSK reception.
- Phase detector algorithm 1: This algorithm is used with QPSK reception, over a small range of capture phases and with a channel noise value over 4.5 dB.
- Phase detector algorithm 2: For QPSK reception, it is used after locking, to minimize the bit error rate in low channel noise conditions. Algorithm 2 is recommended for most applications.

The loop is controlled through $\alpha$ and $\beta$ parameters.

The carrier loop control registers (the Alpha Carrier Register, the Beta Carrier Register and the Carrier Frequency Register) are in Addresses 13, 14, 22 and 23.

#### 4.4.1 Loop Parameters

Like the timing loop, the carrier loop is a second-order system where two parameters, $\alpha$ and $\beta$, may be programmed with alpha_car and beta_car respectively.

The natural frequency ($f_n$) is:

$$f_n = 7 \cdot 10^{-6} \cdot f_{M\_CLK} \sqrt{(m2 \cdot \beta) \frac{f_S}{f_{M\_CLK}}}$$

The damping factor is:

$$\xi = 22 \cdot 10^{-6} \cdot \alpha \sqrt{\frac{m2}{\beta} \frac{f_S}{f_{M\_CLK}}}$$

where $\alpha = (2+a) \cdot 2^b \cdot 2^{14}$, with $b \geq 1$, and $\beta = (4+2c+d) \cdot 2^e$, with $e \geq 1$. m2 is the reference level in the AGC2 register.

#### 4.4.2 Carrier Lock Detector

The carrier lock detector provides an indicator with a high value when the carrier is locked, dependent on the channel noise. When the carrier is not locked, the indicator value is low.

The indicator value is compared to a programmable 8-bit threshold (Register 15h). The result of this comparison (1 if greater than the threshold, else 0 if not) is written as the Carrier Found flag (CF), and may be read in the status register. The CF signal may be permanently routed on the output LOCK (see Register 08h).

The Lock Detector Threshold Register and Lock Detector Value Register are in Addresses 15 and 1C.

#### 4.4.3 Derotator Frequency

The derotator frequency can be either measured (read operation) or forced (write operation).

$$(freq)_{kHz} = \frac{Derot\_freq}{2^{16}} \cdot (f_{M\_CLK})_{kHz}$$

Derot_freq is a 16-bit signed value.

The Derot_freq Registers are Registers 22 and 23.

#### 4.4.4 Carrier Frequency Offset Detector

The carrier recovery loop features a carrier frequency offset detector and two phase detectors. When the carrier frequency offset detector is enabled, the central loop frequency is modified proportionally to the carrier offset. The gain and time constants of the detector are set by CFD[6:4] and CFD[3:2] respectively. When the carrier loop is about to “phase lock” with the carrier, the frequency detector stops automatically and the phase lock is ensured by the selected phase detector. This switchover point is determined by the threshold CFD [1:0].

For stability reasons, the gain CFD [6:4] should not exceed the coefficient e[3:0] of Register BCLC.

The carrier frequency offset detector is in Address 12.

### 4.5 Noise Indicator

The noise indicator may be used to facilitate the antenna pointing or to give an idea of the RF signal quality and of the front-end installation (dish, LNB, cable, tuner or ADC).

A simple C/N estimator can be easily implemented by comparing the current indications with a primarily-recorded look-up table.

The time constant ranges from 4 k to 256 k symbols. The 16 MSB of the result may be read by the microprocessor (Registers 24 and 25).

## 4 FUNCTIONAL DESCRIPTION (continued)

### 4.6 Forward Error Correction

#### 4.6.1 FEC Modes

Since the STV0299B is a multistandard decoder, several combinations are possible, at different levels:

- The demodulator may accept either QPSK or BPSK signals - the only impact is on the carrier algorithm choice (refer to Chapter 4.4).
  The algorithm choice also affects the carrier lock detector and the noise evaluation.
- There two primary options concerning the FEC operation - between DVB, DSS and Reserved Mode.
- There are two options concerning the FEC feeding. The first is IQ flow, which is the usual case in QPSK modes DVB or DSS. The second mode is I-only flow, used for BPSK.

The FEC Mode Register is in Address 28.

In Modes DVB and DSS, data is fed to the Viterbi decoder. Other parts of the decoding (such as the Convolutional Deinterleaver) may be bypassed.

#### 4.6.2 Viterbi Decoder and Synchronization

The convolutive codes are generated by the polynomial $G_x$ = 171 octets and $G_y$ = 133 octets in modes DVB or DSS.

The Viterbi decoder computes for each symbol the metrics of the four possible paths, proportional to the square of the Euclidian distance between the received I and Q and the theoretical symbol value.

The puncture rate and phase are estimated on the error rate basis. Several rates are allowed and may be enabled/disabled through register programming:

- 1/2, 2/3, 3/4, 5/6, 7/8 in DVB.
- 1/2, 2/3, 3/4, 5/6 and 6/7 in DSS.

For each enabled rate, the current error rate is compared to a programmable threshold. If it is greater than this threshold, another phase (or another rate) is tried until the right rate is obtained.

A programmable hysteresis is added to avoid losing the phase during short term perturbation.

The rate may also be imposed by external software, and the phase is incremented only upon request by the microprocessor. The error rate may be read at any time in order to use an algorithm other than that implemented.

The Viterbi decoder produces an absolute decoding. The decoder is controlled via several Viterbi Threshold Registers (Registers 29, 2A, 2B, 2C and 2D). For each Viterbi Threshold Register, bits 6 to 0 represent an error rate threshold - the average number of errors occurring during 256-bit periods. The maximum programmable value is 127/256 (higher error rates are of no practical use).

The Puncture Rate and Synchro Register is in Address 31.

The automatic rate research is only done through the enabled rates (see the corresponding bit set in the Puncture and synchro register). In DSS, the puncture rate 6/7 replaces the puncture rate 7/8. In DSS, it is recommended that you disable puncture rates 3/4 and 5/6 in order to save time in the synchronization process.

The VSEARCH Register is in Address 32. VSEARCH bit 7 (A/M) and bit 6 (F) programs the automatic/manual (or computer aided) search mode as follows:

- If A/M =0 and F=0, automatic mode is set. Successive enabled punctured rates are tried with all possible phases, until the system is locked and the block synchro found. This is the default (reset) mode.
- If A/M=0 and F=1, the current puncture rate is frozen. If no sync is found, the phase is incremented, but not the rate number. This mode allows shortening of the recovery time in case of noisy conditions. The puncture rate is not supposed to change in a given channel. In a typical computer-aided implementation, the research begins in automatic mode. The microprocessor reads the error rate or the PRF flag in order to detect the capture of a signal, then it switches F to 1, until a new channel is requested by the remote control.
- If AM=1 manual mode is set. In this case, only one puncture rate should be validated - the system is forced to this rate, on the current phase, ignoring the time-out register and the error rate. In this mode, each 0 to 1 transition of the bit F leads to a phase incrementation, allowing full control of the operation by an external microprocessor by choosing the lowest error rate.

The reset values are A/M=0, and F=0 (automatic search mode).

The VERROR Register (a read only register) is in Address 26. The last value of the error rate may be read at any time in the register. Unlike the VTH, the possible range is from 0 to 255/256.

The VSTATUS Register (a read only register) is in Address 1B.

## 4 FUNCTIONAL DESCRIPTION (continued)

### 4.6.3 Synchronization

In DVB, the packet length after inner decoding is 204. The sync word is the first byte of each packet. Its value is Hex 47, but this value is complemented every 8 packets. In DSS, the packet length is 147 and the sync word is Hex 1D.

An Up/Down Sync counter counts whenever a sync word is recognized with the correct timing, and counts down during each missing sync word. This counter is bounded by a programmable maximum - when this value is reached, the LK bit ("locked") is set in the VSTATUS register. When the event counter counts down to until 0, this flag is reset.

### 4.6.4 Error Monitoring

A 16-bit counter, ERRCNT, allows the counting of errors at different levels. ERRCNT is fed either by:

- the input QPSK bit errors (that are corrected by the Viterbi decoder), or,
- the bit, or,
- the byte error (that are corrected by the Reed-Solomon decoder), or,
- the packet error (not corrigible, leading to a pulse at the ERROR output).

The content of ERRCNT may be transferred to the read only registers ERRCNT_LOW (LSB) and ERRCNT_HIGH (MSB).

Two functional modes are proposed, depending on a control register bit:

1 Error Mode = 0. This is an error rate measure, that tells the number of errors occurring within a specified number of output bytes, NB. NB has four possible values given in the Error Control Register in Address 34. Every NB bytes, the state of the error counter is transferred to a 16-bit register, then the error counter is reset. The Error Count Registers in Addresses 1D and 1E may be read by the microprocessor via $I^2C$ bus. Two ways of reading may be used: 16-bit reading, starting with MSB, or 8-bit reading (LSB only or MSB only).

2 Error Mode = 1. The error counter just counts the error; the $I^2C$ register permanently copies the content of the error counter. When the MSB byte is read, the error counter is reset. In both modes, the 16-bit counter is saturated to its maximum value.

### 4.6.5 Convolutional Deinterleaver

In DVB, the convolutional deinterleaver is 17 x 12. The periodicity of 204 bytes per sync byte is retained. In DSS, the convolutional deinterleaver is 146 x 13, and there is also a periodicity of 147 bytes per sync byte. The deinterleaver may be bypassed - for details, see Section 4.6.6 *'Reed-Solomon Decoder and Descrambler'*.

### 4.6.6 Reed-Solomon Decoder and Descrambler

The input blocks are 204-byte long with 16 parity bytes in DVB. The synchro byte is the first byte of the block. Up to 8 byte errors may be fixed.

The Code Generator polynomial is:

$$\mathbf{g}(\mathbf{x}) = (\mathbf{x} - \boldsymbol{\omega}^{\mathbf{0}})(\mathbf{x} - \boldsymbol{\omega}^{\mathbf{1}})(\ldots)(\mathbf{x} - \boldsymbol{\omega}^{\mathbf{15}})$$

over the Galois Field generated by:

$$\mathbf{x^8 + x^4 + x^3 + x^2 + 1 = 0}$$

Energy dispersal descrambler and output energy dispersal descrambler generator:

$$\mathbf{x^{15} + x^{14} + 1}$$

The polynomial is initialized every eight blocks with the sequence 100101010000000.

The synchro words are unscrambled and the scrambler is reset every 8 packets.

The output interface may be forced into high impedance mode by setting bit 0 of Address 28. Doing this affects the D[7:0], CLK_OUT, STR_OUT, D/P and ERROR pins. This also allows for board testing, and "OR" wiring several link circuits (for example, cable links). The output stream is either parallel (byte stream) or serial (bit stream) depending on bit 1 of Address 28.

The outputs are controlled by the RS Control Register in Address 33.

### 4.6.7 Parallel Output Interface

A schematic diagram of the parallel output interface is shown in Figure 7. The parallel output format is compliant with the DVB common interface protocol.

When the SYNC is not found (LK = 0 in the status register), D/P (corresponding to the MiVAL signal of the DVB common interface standard) remains at a low level.

CLK_OUT has a duty cycle between 40 and 60%.

## 4 FUNCTIONAL DESCRIPTION (continued)

### 4.6.8 Serial Output Interface

The serial output interface is shown in Figure 6. The serial bit stream is available on D7, where MSB is first to reconstruct the original order. If RS0 = 0, then the parity bits are output (Register 33). If RS0 = 1, the data is null during the parity time slots.

STR_OUT is only high during the first bit of each packet, instead of during the first byte in parallel mode.

ERROR has the same function as in parallel mode.

CLK_OUT is the serial bit clock; it is derived from either the master clock, M_CLK, (if SerClk = 0 in Registers 02 and B3), or from the internal VCO frequency divided by 6, (if SerClk = 1), by skipping some pulses to accommodate the frequency difference.

All of the outputs are synchronous of the same master clock edge.

D0, STR_OUT, D/P and ERROR may be properly sampled externally by the rising edge of CLK_OUT, if RS1 = 0, or by the falling edge of CLK_OUT if RS1 = 1. This clock runs continuously, even during parity data, whatever the value of RS0.

The first bit detected in a valid packet may be decoded if it is found on the appropriate edge of CLK_OUT, where STR_OUT = 1, ERROR = 0, D/P = 1. The following bits only require the assertion of D/P (while D/P = 1,...).

Outputs D0 to D6 remain at low level in serial mode.

**Figure 6:** Serial Output Interface

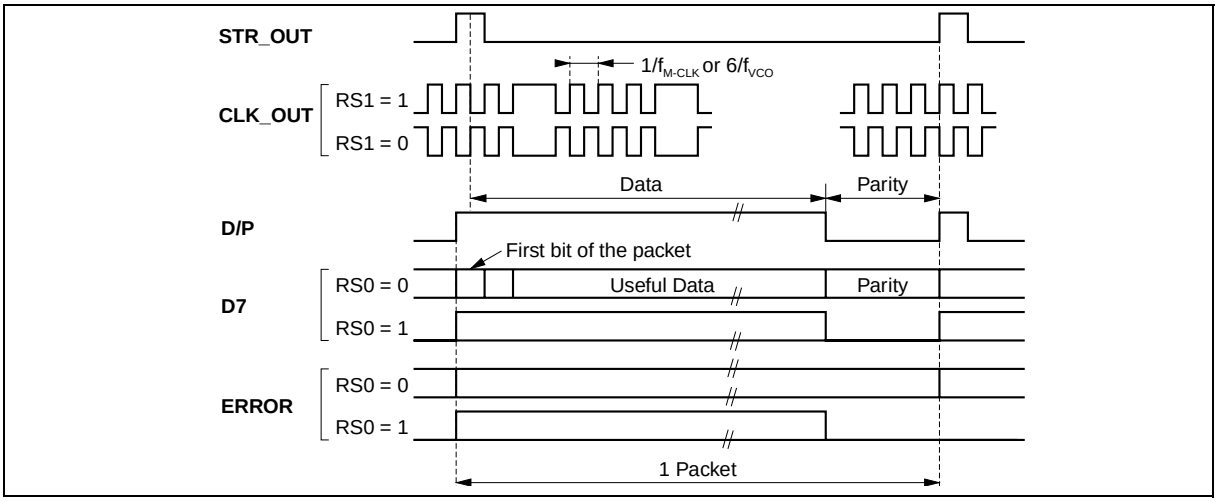



**Figure 7:** Parallel Output Interface

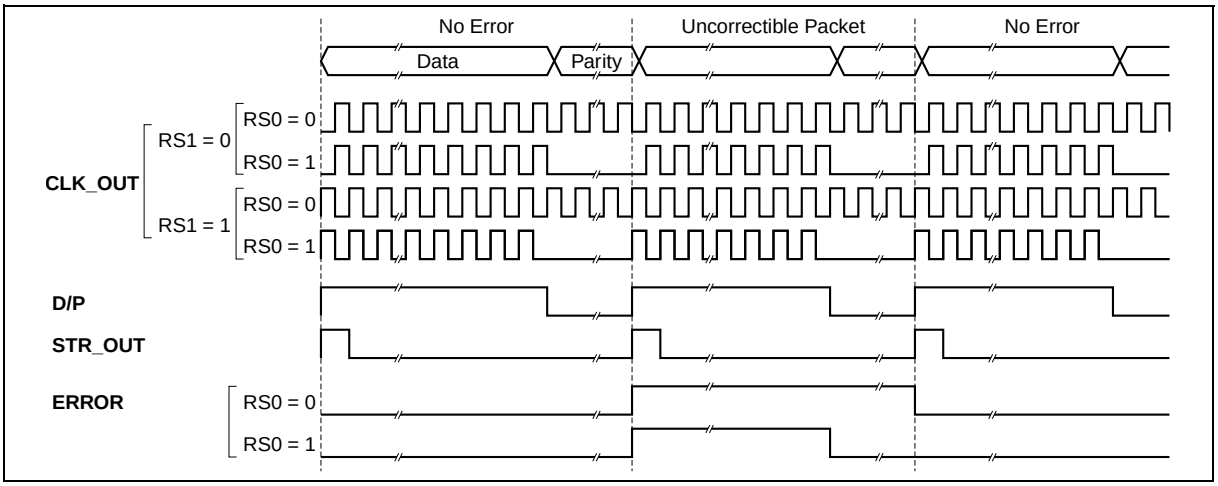


**Table 6: Functional I²C Register Map**

| Name | Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|---|---|
| ID | $00(r/w) | Chip identification number | | | | Release number | | | |
| RCR * | $01(w) | K(1:0) | | dirclk | M(4:0) | | | | |
| MCR * | $02(w) | stdby | VCO off | | | serclock | P(2:0) | | |
| ACR * | $03(w) | prescaler | | | divider | | | | |
| F22FR | $04(w) | frequency register f_reg(7:0) | | | | | | | |
| 12CRPT | $05(w) | 12CT | | T- constant | T- constant | | SCLT value | | SDAT value |
| DACR1 | $06(w) | DAC mode | | | | DAC(11:8) | | | |
| DACR2 | $07(w) | DAC(7:0) | | | | | | | |
| DiSEqC | $08(w) | LOCK output | | LOCK conf | | | DiSEqC | DiSEqC mode | |
| DiSEqC FIFO | $09(w) | DiSE1C FIFO1(7:0) | | | | | | | |
| DiSEqC Status | $0A(r) | IP | SDAT input status | | | | | FE | FF |
| IOCFG | $0C(w) | OP1_ opdrain | OP1_1 | OP0_ opdrain | OP01 | | Nyquist filter | | I/Q conv |
| AGC1C | $0D(w) | DCadj | | | | | beta_agc1(2:0) | | |
| RTC | $0E(w) | | alpha_tmg(2:0) | | | | beta_tmg(2:0) | | |
| AGC1R | $0F(w) | Iagc | | Reference Value | | | | | |
| ACG2O | $10(w) | AGC2 coeff(2:0) | | | ACG2_Ref | | | | |
| TLSR | $11(w) | step_minus(3:0) | | | | step_plus(3:0) | | | |
| CFD | $12(w) | FD on/off | beta_fd | | | FDTC | | LDL | |
| ACLC | $13(w) | derot on/off | | noise_TC | | alpha_car | | | |
| BCLC | $14(w) | Ph_detect_algo | | beta_car | | | | | |
| CLDT | $15(w) | Lock detector threshold | | | | | | | |
| AGC1I | $16(r/w) | AGC integrator value | | | | | | | |
| TL1R | $17(w) | Timing lock indicator(7:0) | | | | | | | |
| ACG2I1 | $18(r/w) | ACG2 integrator MSB | | | | | | | |
| ACG2I2 | $19(r/w) | ACG2 integrator LSB | | | | | | | |
| RTF | $1A(r/w) | Timing loop frequency(7:0) | | | | | | | |
| VSTATUS | $1B(r) | CF | | | PRF | LK | PR(2:0) | | |
| CLDI | $1C(r) | Lock detector integrator | | | | | | | |
| ECNTH | $1D(r) | Error count MSBs | | | | | | | |
| ECNTL | $1E(r) | Error count LSBs | | | | | | | |
| SFRH | $1F(w) | Symb_freq(19:12) | | | | | | | |
| SFRM | $20(w) | Symb_freq(11:4) | | | | | | | |
| SFRL | $21(w) | Symb_freq(3:0) | | | | | | | |
| CFRM | $22(r/w) | Carrier frequency register MSB | | | | | | | |
| CFRL | $23(r/w) | Carrier frequency register LSB | | | | | | | |
| NIRH | $24(r) | Noise indicator MSBs | | | | | | | |
| NIRL | $25(r) | Noise indicator LSBs | | | | | | | |
| VERROR | $26(r) | Error value | | | | | | | |
| FECM | $28(w) | FEC mode | | | | | | out type | out imp |
| VTH0 | $29(w) | | t0[6:0] | | | | | | |
| VTH1 | $2A(w) | | t1[6:0] | | | | | | |
| VTH2 | $2B(w) | | t2[6:0] | | | | | | |
| VTH3 | $2C(w) | | t3[6:0] | | | | | | |
| VTH4 | $2D(w) | | t4[6:0] | | | | | | |
| PR | $31(w) | | | | E4 | E3 | E2 | E1 | E0 |
| $V_{SEARCH}$ | $32(w) | A/M | F | SN(1:0) | | TO(1:0) | | H(1:0) | |
| RS | $33(w) | deint | sync | RS | descram | err bit | MPEG | clk pol | clk cfg |
| ERRCNT | $34(w) | Errmode | tsters | Error source | | | | NoE | |

## 5 REGISTER LIST

*Note:* All register addresses are hexadecimal values. Signed registers are 2's complement. All registers are read/write registers except those specifically flagged as read-only (RO). All registers not listed in the below table, between 0 and 4E, should be programmed to 0.

| Name | HEX Address | Reset Value | Bit Position | Signal Description |
|---|---|---|---|---|
| **IDENTIFICATION REGISTER (Read Only)** (refer to *Section 4.1.6* **on page 8**) | | | | |
| ID | 00 | A1 | [7:0] | Gives the release number of the circuit in order to ensure software compatibility. |
| **REFERENCE CLOCK REGISTER** (refer to *Section 4.1.8* **on page 8**) | | | | |
| RCR | 01 | 18 or 38 | [7:6] | **K[1:0]** |
| | | | 5 | **DIRCLK** (Reset value depends on the polarity of DIRCLK-DIS pin). |
| | | | [4:0] | **M[4:0]** |
| **MASTER CLOCK REGISTER** (refer to *Section 4.1.8* **on page 8**) | | | | |
| MCR | 02 | 34 or B4 | 7 | **STDBY** (Reset value depends on the polarity of STDBY pin). |
| | | | 6 | **VCO ON/OFF**<br>0: ON<br>1: OFF |
| | | | [5:4] | These bits must be programmed to one. |
| | | | 3 | **SERCLK**<br>0: Maximum instantaneous SERCL = Master Clock<br>1: Maximum instantaneous SERCL = $\frac{F_{VCO}}{6}$ |
| | | | [2:0] | **P[2:0]**<br>VC0 to M_CLK divider |

## 5 REGISTER LIST (continued)

| Name | HEX Address | Reset Value | Bit Position | Signal Description |
|---|---|---|---|---|

**AUXILIARY CLOCK REGISTER** (refer to *Section 4.1.8* **on page 8**)

ACR | 03 | 2A | [7:0]

**ACR Prescaler and Divider**

This register is made up of the ACR [7:5] Prescaler field and the ACR [4:0] Divider field. The values in these fields configure the auxiliary clock function, the prescalar value, the clock signal frequency.
The frequency range is given for $f_{VCO}$ = 400 MHz.

| ACR [7:0] | Function | Prescaler | Signal Frequency | Range |
|---|---|---|---|---|
| 000XXXX0 | Output Port | N/A | output port = 0 | N/A |
| 000XXXX1 | Output Port | N/A | output port = 1 | N/A |
| 001XXXXX | HF generator | 1 | $f_{VCO}$/8/ACR[4:0] | 1.6 to 50 MHz |
| 010XXXXX | LF generator | 64 | $f_{VCO}$/8192/(32+ACR[4:0]) | 775 to 1525 Hz |
| 011XXXXX | LF generator | 128 | $f_{VCO}$/16384/(32+ACR[4:0]) | 388 to 762 Hz |
| 100XXXXX | LF generator | 256 | $f_{VCO}$/32768/(32+ACR[4:0]) | 194 to 381 Hz |
| 101XXXXX | LF generator | 512 | $f_{VCO}$/65536/(32+ACR[4:0]) | 97 to 190 Hz |
| 110XXXXX | LF generator | 1024 | $f_{VCO}$/131072/(32+ACR[4:0]) | 49 to 95 Hz |
| 111XXXXX | LF generator | 2048 | $f_{VCO}$/262144/(32+ACR[4:0]) | 24 to 47 Hz |

In the LF generator, the programmable division factor is 32 + ACR[4:0]. In the HF generator, it is simply ACR[4:0]. This allows the building of any frequency from 24 Hz to 1.1 kHz (within ±1.5%) in the full operating range. The output signal is square in all cases. When the auxiliary register is written, the prescaler and the programmable divider are reset.

**F22 FREQUENCY REGISTER** (refer to *Section 4.1.8* **on page 8**)

F22FR | 04 | 8E | [7:0] | The actual frequency is $f_{VCO}$/(128 R[7:0]). When this register is accessed, the divider by 16 (also common to AUX_CLK) and the divider by R[7:0] are initialized.

**$I^2C$RPT REGISTER** (refer To *Section 4.1.10* **on page 10**)

| | | | | |
|---|---|---|---|---|
| $I^2C$RPT | 05 | 0F | 7 | **$I^2C$T**<br>1: $I^2C$ repeater<br>0: Output port |
| | | | [6] | Must be programmed to zero. |
| | | | [5:4] | Repeater response time; value does not matter if the external time constant ≤ 250ns. |
| | | | [3] | Must be programmed to zero. |
| | | | 2 | **SCLT Port value** |
| | | | 1 | This bit must be programmed to zero. |
| | | | 0 | **SDAT Port value** |

## 5 REGISTER LIST (continued)

| Name | HEX Address | Reset Value | Bit Position | Signal Description |
|---|---|---|---|---|
| **DAC REGISTERS** (refer to *Section 4.1.11* **on page 10**) | | | | |
| DACR1 (MSB) | 06 | A2 | [7:5] | **DAC Mode**<br>This field controls the DAC:<br>**000**: Functions as output port. The DAC output permanently 0.<br>**001**: Functions as output port. DAC output permanently 1.<br>**010**: High impedance mode.<br>**100**: Functions as DAC. Duty cycle modulated at $f_{CLK}/16$.<br>**101**: Functions as DAC. Duty cycle modulated at $f_{CLK}/4$.<br>**110**: Functions as DAC. Duty cycle modulated at $f_{CLK}$.<br>**Other**: Reserved functions. |
| | | | 4 | This bit must be programmed to zero. |
| | | | [3:0] | **DAC: 4 MSB** |
| DACR2 (LSB) | 07 | 00 | [7:0] | **DAC: 8 LSB** |
| **DISEQC AND LOCK CONTROL REGISTER** (refer to *Section 4.1.12* **on page 10**) | | | | |
| DiSEqC | 08 | 60 | [7:6] | **Lock Output**<br>00: 0<br>01: 1<br>10: CF<br>11: LK |
| | | | 5 | **Lock Configuration**<br>1: Open drain<br>0: Push-pull |
| | | | [4:3] | These bits must be programmed to zero. |
| | | | 2 | **DiSEqC/Unmodulated Burst** |
| | | | [1:0] | **DiSEqC Mode** |
| **DISEQC FIFO** (refer to *Section 4.1.12* **on page 10**) | | | | |
| DiSEqC FIFO | 09 | 00 | [7:0] | **FIFO byte** |
| **DISEQC STATUS** (refer to *Section 4.1.12* **on page 10**) | | | | |
| DiSEqC Status | 0A | R0 | 7 | **Input Port**: This bit gives the input level on the pin IP0. It is an input port for general use purposes. |
| | | | 6 | **SDAT Input State** |
| | | | [5:2] | Not relevant. |
| | | | 1 | **FIFO empty** |
| | | | 0 | **FIFO full** |
| **RESERVED** | | | | |
| | 0B | | | **Reserved** |

## 5 REGISTER LIST (continued)

| Name | HEX Address | Reset Value | Bit Position | Signal Description |
|---|---|---|---|---|
| **INPUT/OUTPUT CONFIGURATION REGISTER** (refer to *Section 4.2.1* **on page 12**) | | | | |
| IOCFG | 0C | F0 | 7 | **OP1 control**<br>1: Open drain<br>0: Normal |
| | | | 6 | **OP1 value** |
| | | | 5 | **OP0 control**<br>1: Open drain<br>0: Normal |
| | | | 4 | **OP0 value** |
| | | | 3 | This bit must be programmed to zero. |
| | | | [2:1] | **Nyquist Filter**<br>These bits determine Nyquist filter settings:<br>00 = raised cosine at 35%<br>01 = raised cosine at 20%<br>10 = reserved<br>11 = reserved |
| | | | 0 | Bit 0 when set, multiplies the data on the Q input by -1 in order to accommodate QPSK modulation with another convention of rotation sense. This is equivalent to a permutation of I and Q inputs, or a spectral symmetry. This permutation is performed after derotation. |
| **AGC1 CONTROL REGISTER** (refer to *Section 4.2.2* **on page 12**) | | | | |
| AGC1C | 0D | 81 | 7 | **DC offset compensation:**<br>1: On<br>0: Off |
| | | | [6:3] | These bits must be programmed to zero. |
| | | | [2:0] | **beta_agc1** |
| **TIMING LOOP REGISTER** (refer to *Section 4.3.1* **on page 13**) | | | | |
| RTC | 0E | 23 | 7 | This bit must be programmed to zero. |
| | | | [6:4] | **alpha_tmg** |
| | | | 3 | This bit must be programmed to zero. |
| | | | [2:0] | **beta_tmg** |
| **AGC1 REFERENCE REGISTER** (refer to *Section 4.2.2* **on page 12**) | | | | |
| AGC1R | 0F | 54 | 7 | **Iagc**<br>1: Invert<br>0: Normal<br>If Iagc is set, the output signal is complemented (i.e. a high value for the AGC voltage will cause a high gain in the tuner). |
| | | | 6 | This bit must be programmed to zero. |
| | | | [5:0] | **AGC1 Reference Value (m1).** Refer to page 12. |
| **AGC2 AND OFFSET CONTROL REGISTER** (refer to *Section 4.2.5* **on page 12**) | | | | |
| AGC2O | 10 | 74 | [7:5] | **AGC2 Coefficient** |
| | | | [4:0] | **AGC2_Ref (m2)** |

## 5 REGISTER LIST (continued)

| Name | HEX Address | Reset Value | Bit Position | Signal Description |
|---|---|---|---|---|
| **TIMING LOCK SETTING REGISTER** (refer to ) | | | | |
| TLSR | 11 | 88 | [7:4] | Must be programmed to 8 (to be confirmed) |
| | | | [3:0] | Must be programmed to 4 (to be confirmed) |
| **CARRIER FREQUENCY DETECTOR REGISTER** (refer to *Chapter 4.4* **on page 14**) | | | | |
| CFD | 12 | F7 | 7 | 1: Carrier Frequency Offset Detector coupled to Carrier recover loop<br>0: Carrier Frequency Offset Detector disabled |
| | | | [6:4] | Gain for Carrier Frequency Offset Detector |
| | | | [3:2] | Time constant for Carrier Frequency Offset Detector |
| | | | [1:0] | **Lock Detector threshold to disable the Carrier Frequency Offset Detector:**<br>00: -16<br>01: -32<br>10: -48<br>11: -64 |
| **ALPHA CARRIER AND NOISE ESTIMATOR REGISTER** (refer to *Chapter 4.5* **on page 14**) | | | | |
| ACLC | 13 | 88 | 7 | **Derotator On/Off**<br>1: On<br>0: Off |
| | | | 6 | This bit must be programmed to zero. |
| | | | [5:4] | **Noise Estimator Time Constant**<br>00: 4 k symbols<br>01: 16 k symbols<br>10: 64 k symbols<br>11: 256 k symbols |
| | | | [3:0] | **alpha_car**<br>Bits 3, 2 and 1: b[2:0]<br>Bit 0: a |
| **BETA CARRIER REGISTER** (refer to *Chapter 4.4* **on page 14**) | | | | |
| BCLC | 14 | 5C | [7:6] | **phase_detector_algo**<br>Phase detector algorithm:<br>00: Algorithm 0 (BPSK application)<br>01: Algorithm 1 (QPSK application)<br>10: Algorithm 2 (QPSK application)<br>11: Reserved |
| | | | [5:0] | **beta_car**<br>Bits 5 to 2: e[3:0]<br>Bit 1: c<br>Bit 0: d |
| **CARRIER LOCK DETECTOR THRESHOLD REGISTER** (refer to *Section 4.4.2* **on page 14**) | | | | |
| CLDT | 15 | 14 | [7:0] | Signed Number |
| **AGC1 INTEGRATOR REGISTER** (refer to *Section 4.2.2* **on page 12)** | | | | |
| AGC1I | 16 | | [7:0] | **AGC Integrator Value** (Signed Number) |
| **TIMING LOCK INDICATOR REGISTER** (refer to *Section 4.3.3* **on page 13**) | | | | |
| TLIR | 17 | R0 | [7:0] | (Not Signed) |

## 5 REGISTER LIST (continued)

| Name | HEX Address | Reset Value | Bit Position | Signal Description |
|---|---|---|---|---|
| **AGC2 INTEGRATOR REGISTERS** (refer to *Section 4.2.5* **on page 12**) | | | | |
| AGC2I1 (MSB) | 18 | | [7:0] | **AGC2 Integrator MSB Bits** (Not Signed) |
| AGC2I2 (LSB) | 19 | | [7:0] | **AGC2 Integrator LSB Bits** (Not Signed) |
| **TIMING FREQUENCY REGISTER** (refer to *Section 4.3.1* **on page 13**) | | | | |
| RTF | 1A | | [7:0] | Signed Number |
| **VSTATUS REGISTER (Read Only)** (refer to *Section 4.6.3* **on page 16**) | | | | |
| VSTATUS | 1B | RO | 7 | **Carrier Found Flag**<br>When the Carrier Found (CF) flag (see *Chapter 4.4* on page 14) is set, it indicates that a QPSK signal is present at the input of the Viterbi decoder. |
| | | | [6:5] | Not relevant. |
| | | | 4 | **Puncture Rate Found**<br>The Puncture Rate Found (PRF) bit indicates the state of the puncture rate research: 0 for searching and 1 when found. This bit is irrelevant in manual mode. |
| | | | 3 | **Locked/Searching Sync Word**<br>The LK bit indicates the state of the sync word search: 0 for searching and 1 when found. |
| | | | [2:0] | **Current Puncture Rate, PR[2:0]**<br>The Current Puncture Rate (CPR) bits hold the current puncture rate indices, as follows:<br>100: Basic 1/2 (modes DVB and DSS) or Punctured 1/2 (reserved mode)<br>000: Punctured 2/3<br>001: Punctured 3/4<br>010: Punctured 5/6<br>011: Punctured 7/8 (modes DVB and DSS) or 6/7 (reserved mode) |
| **CARRIER LOCK DETECTOR VALUE REGISTER** (refer to *Section 4.4.2* **on page 14**) | | | | |
| CLDI | 1C | | [7:0] | Signed Number |
| **ERROR COUNT REGISTERS** (refer to *Section 4.6.4* **on page 16**) | | | | |
| ERRCNT_HIGH | 1D | | [7:0] | MSB byte (Not Signed) |
| ERRCNT_LOW | 1E | | [7:0] | LSB byte (Not Signed) |
| **SYMBOL FREQUENCY REGISTERS** (refer to *Section 4.3.1* **on page 13**) | | | | |
| SFRH | 1F | 80 | [7:0] | **Symb_freq** (MSBs)<br>The reset value of Hex 800000 corresponds to $f_{M\_CLK}/2$. |
| SFRM | 20 | 00 | [7:0] | **Symb_freq** (Middle $SB_S$) |
| SFRL | 21 | 00 | [7:4] | **Symb_freq** ($LSB_S$) |
| | | | [3:0] | These bits must be programmed to zero. |
| **CARRIER FREQUENCY REGISTER** (refer to *Chapter 4.4* **on page 14**) | | | | |
| CFRM | 22 | | [7:0] | **Derotator Frequency (MSB) (signed value)** |
| CFRL | 23 | | [7:0] | **Derotator Frequency (LSB) (signed value)** |
| **NOISE INDICATOR REGISTERS (Read Only)** (refer to *Chapter 4.5* **on page 14**) | | | | |
| NIRH | 24 | RO | [7:0] | **Noise Indicator (MSB)** (Not Signed) |
| NIRL | 25 | RO | [7:0] | **Noise Indicator (LSB)** (Not Signed) |

## 5 REGISTER LIST (continued)

| Name | HEX Address | Reset Value | Bit Position | Signal Description |
|---|---|---|---|---|
| **VERROR REGISTER (Read Only)** (refer to *Section 4.6.2* **on page 15**) | | | | |
| VERROR | 26 | RO | [7:0] | **Error Rate** (Not Signed) |
| **FEC MODE REGISTER** (refer to *Section 4.6.1* **on page 15**) | | | | |
| FECM | 28 | 01 | [7:4] | **FEC Mode**<br>This field indicates the FEC Operation mode and the FEC feeding.<br>0000: DVB (QPSK), FEC feeding IQ/IQ/IQ/IQ<br>0001: DVB (BPSK extension), FEC feeding IX/IX/IX/IX<br>001X: Reserved<br>0100: DSS, FEC feeding IQ/IQ/IQ/IQ<br>1XXX: Reserved |
| | | | [3:2] | These bits must be programmed to zero. |
| | | | 1 | **Output Type**<br>1: Serial<br>0: Parallel |
| | | | 0 | **Output Impedance**<br>1: High Impedance<br>0: Normal Impedance |
| **VITERBI THRESHOLD REGISTERS** (refer to *Section 4.6.2* **on page 15**) | | | | |
| VTH0 | 29 | 1E | [7:0] | **Rate = 1/2 Threshold.** |
| VTH1 | 2A | 14 | [7:0] | **Rate = 2/3 Threshold.** |
| VTH2 | 2B | 0F | [7:0] | **Rate = 3/4 Threshold.** |
| VTH3 | 2C | 09 | [7:0] | **Rate = 5/6 Threshold.** |
| VTH4 | 2D | 05 | [7:0] | **Rate = 7/8 or 6/7 Threshold.** |
| **PUNCTURE RATE AND SYNCHRO REGISTER** (refer to *Section 4.6.2* **on page 15**) | | | | |
| PR | 31 | 1F | [7:6:5] | These bits must be programmed to zero. |
| | | | 4 | Enable punctured rates 7/8 (in DVB) or 6/7 (in DSS). |
| | | | 3 | Enable punctured rate 5/6. |
| | | | 2 | Enable punctured rate 3/4. |
| | | | 1 | Enable punctured rate 2/3. |
| | | | 0 | Enable basic or punctured rate 1/2. |

## 5 REGISTER LIST (continued)

| Name | HEX Address | Reset Value | Bit Position | Signal Description |
|---|---|---|---|---|
| **VITERBI AND SYNCHRO SEARCH REGISTER** (refer to *Section 4.6.2* **on page 15**) | | | | |
| VSEARCH | 32 | 19 | 7 | **0: Automatic search mode**<br>**1: Manual search mode** |
| | | | 6 | Freeze |
| | | | [5:4] | **SN[1:0]**<br>This is the averaging period. The field gives the number of bits required to calculate the rate error.<br>00 = 1024<br>01 = 4096<br>10 = 16384<br>11 = 65536<br>Reset Value: SN = 01 (4096 bits) |
| | | | [3:2] | **TO[1:0]**<br>This is the time out value (given in 1024-bit periods). This field is used to program the maximum duration of the synchro word research in automatic mode. If no sync is found within this duration, and if bit RS6 (Sync Enable) is set in the Reed-Solomon register, another phase or puncture rate is tried. If RS6 = 0, the time-out has no effect.<br>00 = 16<br>01 = 32<br>10 = 64<br>11 = 128<br>Reset Value: TO = 10 (64k bit periods) |
| | | | [1:0] | **H[1:0]**<br>This is the hysteresis value. This field is used to program the maximum value of the Sync counter. The unit is the block duration (204 bytes in DVB, 147 in DSS).<br>00: 16<br>01: 32<br>10: 64<br>11: 128<br>Reset Value: H = 01 (32 blocks) |

## 5 REGISTER LIST (continued)

| Name | HEX Address | Reset Value | Bit Position | Signal Description |
|---|---|---|---|---|
| **RS CONTROL REGISTER** (refer to *Section 4.6.6* **on page 16**) | | | | |
| RS | 33 | F8 | 7 | **RS7** - Deinterleaver Enable<br>1: The input flow is deinterleaved.<br>0: The input flow is not affected. |
| | | | 6 | **RS6** - Synchro Enable<br>1: The synchro is processed.<br>0: The synchro word search is disabled. The bit-to-byte conversion remains in its current phase regardless of whether the synchro word is recognized or not. This allows the use of the STV0299BB with inner convolutional coding only. |
| | | | 5 | **RS5** - Reed-Solomon Enable<br>1: The input code is corrected.<br>0: No correction happens, all the data is fed to the descrambler. The error signal remains inactive. |
| | | | 4 | **RS4** - Descrambler Enable<br>1: The output flow from Reed-Solomon decoder is descrambled.<br>0: The descrambler is disactivated. |
| | | | 3 | **RS3** - Write Error Bit<br>1: If an uncorrectible error happens in DVB, the MSB of the first byte following the sync byte is forced to 1 after descrambling.<br>0: The output flow is unchanged. |
| | | | 2 | **RS2** - Block Synchro<br>1: The first byte of each packet is forced to Hex 47 in mode A.<br>0: The first byte is the one that is received. In DVB, it should be the synchro byte, complemented every 8th packet. |
| | | | 1 | **RS1** - Output Clock Polarity<br>1: The data and control signals are clocked during the high-to-low transition of CLK_OUT.<br>0: The data and control signals are clocked during the low-to-high transition of CLK_OUT. |
| | | | 0 | **RS0** - Output Clock Signal Configuration during Parity Bytes<br>1: D[7:0] and ERROR are null during the parity bytes. If the packet contains more than 8 errors, ERROR only remains high during the data transmission. In parallel mode, CLK_OUT remains low during the parity bytes. In serial mode, the output bit clock is always running.<br>0: CLK_OUT is continuous and the parity bytes are transmitted. If the packet contains more than 8 errors, ERROR remains high during the entire packet. |

## 5 REGISTER LIST (continued)

| Name | HEX Address | Reset Value | Bit Position | Signal Description |
|---|---|---|---|---|
| **ERROR CONTROL REGISTER** (refer to *Section 4.6.4* **on page 16**) | | | | |
| ERRCNT | 34 | 01 | 7 | **Error Mode**<br>1: Error count<br>0: Error rate |
| | | | 6 | This bit must be programmed to zero. |
| | | | [5:4] | **Error Source**<br>The error sources are as follows:<br>00: QPSK bit errors<br>01: Viterbi bit errors<br>10: Viterbi byte errors<br>11: Packet errors. |
| | | | [3:2] | These bits must be programmed to zero. |
| | | | [1:0] | **NOE**<br>The NOE bits represent the Count Period in bytes (NB):<br>00: $2^{12}$ bytes<br>01: $2^{14}$ bytes<br>10: $2^{16}$ bytes<br>11: $2^{18}$ bytes |

# 6 ELECTRICAL CHARACTERISTICS

## 6.1 Absolute Maximum Ratings

Maximum limits indicate where permanent device damages occur. Continuous operation at these limits is not intended, and should be limited to those conditions specified in Section 6.3 *'DC Electrical Characteristics'*.

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD\_3.3\ V}$ | Pad Power Supply Voltage | 4.0 | V |
| $V_{DD}$ | Core Level Power Supply Voltage | 3.0 | V |
| $V_{I}$(1) | Voltage on Input Pins | -0.5, $V_{DD\_3.3\ V}$ + 0.5 | V |
| $V_{O}$(1) | Voltage on Output Pins | -0.5, $V_{DD\_3.3\ V}$ + 0.5 | V |
| $T_{stg}$ | Storage Temperature | -40, +150 | °C |
| $T_{oper}$ | Operating Ambient Temperature | -10, +70 | °C |
| $T_{j}$ | Junction Temperature | +125 | °C |

*Note: 1* Except for AGC, SDA, SCL, SDAT, SCLT pin, which can be connected to 5 V +10% via a resistor.

## 6.2 Thermal Data

| Symbol | Parameter | Max. Value | Unit |
|---|---|---|---|
| $R_{th(j-a)}$ | Junction-ambient Thermal Resistance | 70(4)<br>45(5) | °C/W |
| $R_{th(j-c)}$ | Junction-case Thermal Resistance | 11 | °C/W |

*Note: 2* Single-layer PCB.
*Note: 3* Multi-layer PCB.

## 6.3 DC Electrical Characteristics

$V_{DD}$ = 2.5 V, $V_{DD\_3.3\ V}$ = 3.3 V and $T_{amb}$ = 25°C unless otherwise specified.

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD\_3.3\ V}$ | Operating Voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{DD\_core}$ | Operating Voltage | | 2.3 | 2.5 | 2.7 | V |
| $V_{DDA}$ | Operating Voltage | Circuit in stand-by | 2.2 | 2.5 | 2.6 | V |
| $V_{DD\_STDBY}$ | Operating Voltage | Circuit in stand-by | 2.3 | 2.5 | 2.7 | V |
| $I_{DD}$ 30M | Average $V_{DD\_2.5V}$ Current | $V_{DD=2.7V}$ = 76MHz | | | 200 | mA |
| $I_{DDA}$ 30M | Average $V_{DDA}$ Current | $V_{DD=2.6V}$ = 76MHz | | | 50 | mA |
| $I_{DD}$ 45M | Average $V_{DD\_2.5V}$ Current | $V_{DD=2.7V}$ = 88MHz | | | 240 | mA |
| $I_{DDA}$ 45M | Average $V_{DDA}$ Current | $V_{DD=2.6V}$ = 88MHz | | | 50 | mA |
| $I_{DDsb}$ | Average Current in Standby Mode | VCO stopped | | 0.5 | 4 | mA |
| $V_{IL}$<br>$V_{IH}$ | Low Level Input Voltage<br>High Level Input Voltage | | <br>2.0 | | 0.8 | V<br>V |
| $I_{LK}$ | Input Leakage Current | 3.6 V | | | 1 | µA |
| $V_{OL}$<br>$V_{OH}$ | High Level Output Voltage<br>Low Level Output Voltage | $V_{DD\_3.3\ V}$ = 3.3 V - 10%<br>$I_{SOURCE}$ = 1.6 mA | 2.4 | | <br>0.4 | V<br>V |

## 6 ELECTRICAL CHARACTERISTICS (continued)

### 6.3 DC Electrical Characteristics (continued)

$V_{DD}$ = 2.5 V, $V_{DD\_3.3\,V}$ = 3.3 V and $T_{amb}$ = 25°C unless otherwise specified.

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **RESET** | | | | | | |
| $V_{ILT}$<br>$V_{IHT}$ | Low Level Threshold Falling Input<br>High Level Threshold Falling Input | | 0.8 | | <br>2.0 | V<br>V |
| **CLK_IN** | | | | | | |
| $V_{IL}$<br>$V_{IH}$ | Low Level Input Voltage<br>High Level Input Voltage | | 0.8 | | <br>2.0 | V<br>V |
| $C_{IN}$ | Input Capacitance | | | 3 | | pF |
| **AGC/SDA/SCL/SDAT/SCLT** | | | | | | |
| $V_{OIL}$ | Low Level Output Voltage | $I_{SINK}$ = 2 mA | | | 0.4 | V |
| $I_{LK}$ | Input Leakage Current | $V_{AGC}$ = 5.5 V | | | 4.0 | µA |
| **A/D CONVERTER** | | | | | | |
| $V_{in}$ | Differential Input Voltage | | 0.4 | 0.5 | 0.8 | $V_{pp}$ |
| $V_{TOP}$ | High Voltage Reference | | | 1.5 | | V |
| $V_{BOT}$ | Low Voltage Reference | | | 1 | | V |
| $R_{in}$ | DC Input Resistance | I/Q Inputs | | $10^6$ | ∞ | Ω |
| $C_{in}$ | Input Capacitance | I/Q Inputs | | 5 | | pF |
| INL | Integral Non-Linearity | | -1.5 | | +1.5 | LSB |
| DNL | Differential Non-Linearity | | -0.8 | | +0.8 | LSB |
| SNR | Signal to Noise Ratio | | 30 | 33 | 36 | dB |
| $N_{eff}$ | Effective Number of bits(1) | | 5.0 | 5.5 | 6.0 | bits |

*Note: 1* Test conditions: $F_{clock}$ = 52MHz, $F_{IN}$ = 8MHz, $V_{IN}$ = 0.5 Vpp

## 6 ELECTRICAL CHARACTERISTICS (continued)

### 6.4 Timing Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{VCO}$ | Internal VCO frequency | 300 | | 400 | MHz |
| $f_{CLK\_IN}$ | CLK_IN or XTAL frequency | 4 | | 30 | MHz |
| **PARALLEL OUTPUT D[7:0], D/P, CLK_OUT, STR_OUT, ERROR OUTPUT CHARACTERISTICS** | | | | | |
| Bit RS1 = 1 in RS CONTROL REGISTER (Address 33). Refer to Figure 8 | | | | | |
| $t_{CLK\_duty}$ | CLK_OUT duty cycle | 40 | 50 | 60 | % |
| $t_{CKSU}$ | D[7:0], D/P, STR_OUT, ERROR stable before CLK_OUT Falling Edge | 2*Tm(1) | | | ns |
| $t_{CKH}$ | D[7:0], D/P, STR_OUT, ERROR stable after CLK_OUT Falling Edge | 2*Tm(1) | | | ns |
| Bit RS1 = 0 in RS CONTROL REGISTER (Address 33). Refer to Figure 9 | | | | | |
| $t_{CKSU}$ | D[7:0], D/P, STR_OUT, ERROR stable before CLK_OUT Falling Edge | 2*Tm(1) | | | ns |
| $t_{CKH}$ | D[7:0], D/P, STR_OUT, ERROR stable after CLK_OUT Falling Edge | 2*Tm(1) | | | ns |
| **SERIAL OUTPUT D7, D/P, CLK_OUT, STR_OUT, ERROR OUTPUT CHARACTERISTICS** | | | | | |
| Bit RS1 = 1 in RS CONTROL REGISTER (Address 33). fM.CLK = 90MHz. Refer to Figure 10 | | | | | |
| $t_{CKSU}$ | D7, D/P, STR_OUT, ERROR stable before CLK_OUT Falling Edge | 3.5 | | | ns |
| $t_{CKH}$ | D7, D/P, STR_OUT, ERROR stable after CLK_OUT Falling Edge | 3 | | | ns |
| Bit RS1 = 0 in RS CONTROL REGISTER (Address 33). fM.CLK = 90MHz. Refer to Figure 11 | | | | | |
| $t_{CKSU}$ | D7, D/P, STR_OUT, ERROR stable before CLK_OUT Falling Edge | 3.5 | | | ns |
| $t_{CKH}$ | D7, D/P, STR_OUT, ERROR stable after CLK_OUT Falling Edge | 2 | | | ns |

*Note: 1* Tm = Master clock period in ns

**Figure 8:**

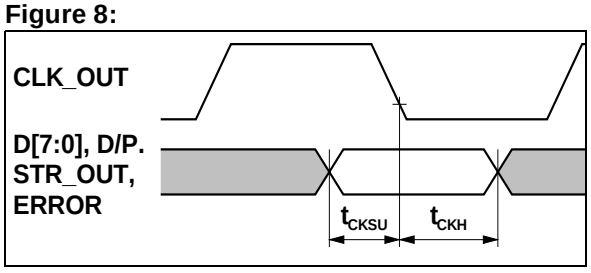



**Figure 9:**

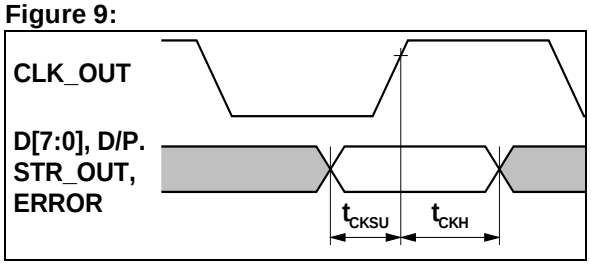



**Figure 10:**

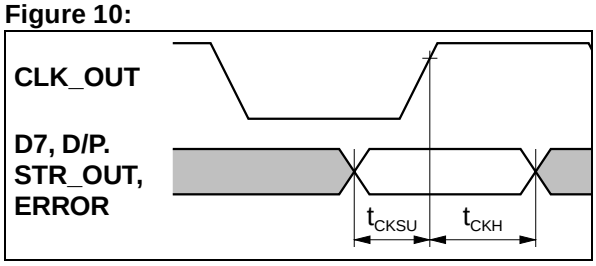
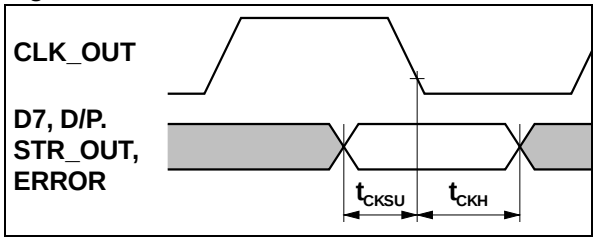



**Figure 11:**

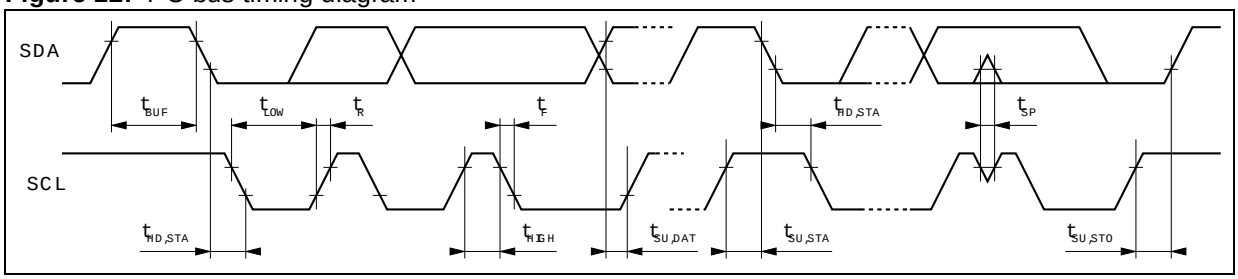


## 6 ELECTRICAL CHARACTERISTICS (continued)

### 6.5 I²C Bus Characteristics

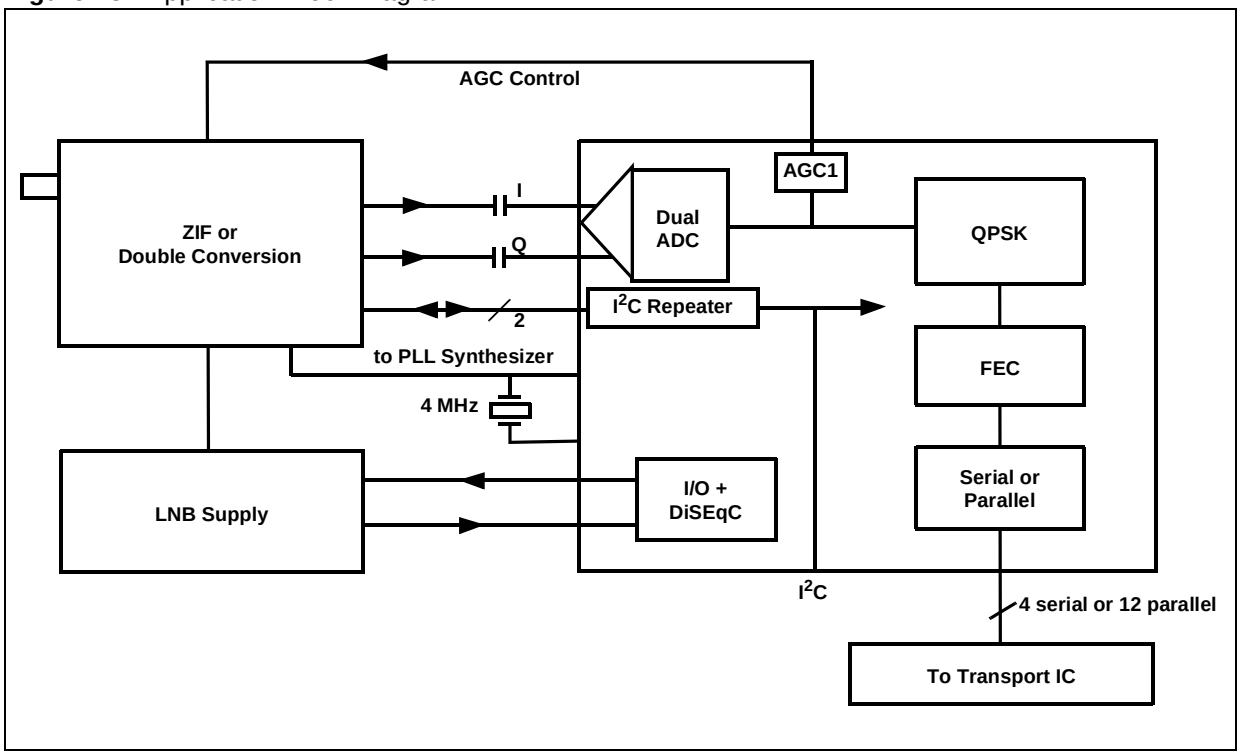
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$<br>$V_{IH}$ | Low Level Input Voltage<br>High Level Input Voltage | Pull up to 5 V ±10% | -0.5<br>2.0 | | 0.8<br>5.5 | V<br>V |
| $V_{OH}$<br>$V_{OL}$ | High Level Output Voltage<br>Low Level Output Voltage | Pull up to 5 V ±10% | | | 5.5<br>0.4 | V<br>V |
| $I_{LK}$ | Input Leakage Current | $V_{IN}$ = 0 V to 5 V | -10 | | 10 | µA |
| $C_{IN}$ | Input Capacitance | 0 | | 3.5 | | pF |
| $I_{OL}$ | Output Sink Current | $V_{OL}$ = 0.5 V | | 10 | | mA |
| $f_{SCLN}$<br>$f_{SCLS}$ | SCL Clock Frequency | Normal Mode<br>Standby Mode | 0<br>0 | | $f_{M\_CLK}/40$<br>$f_{CLK\_IN}/10$ | -<br>- |
| $t_{BUF}$ | Bus Free Time between a STOP and START Condition | | 1.3 | | | µs |
| $t_{HD, STA}$ | Hold Time (repeated) START Condition. After this period, the first clock pulse is generated. | | 0.6 | | | µs |
| $t_{LOW}$<br>$t_{HIGH}$ | Low Period of the SCL Clock<br>High Period of the SCL Clock | | 1.3<br>0.6 | | | µs<br>µs |
| $t_{SU, STA}$ | Setup Time for a repeated START Condition | | 0.6 | | | µs |
| $t_{SU, STO}$ | Setup Time for STOP Condition | | 0.6 | | | µs |
| $t_{SU, DAT}$ | Data Setup Time | | 100 | | | ns |
| $t_R$, $t_F$ | Rise and Fall Time of both SDA and SCL signals | | | | 300 | ns |
| $C_B$ | Capacitive Load for each Bus Line | | | | 400 | pF |

**Figure 12:** I²C bus timing diagram



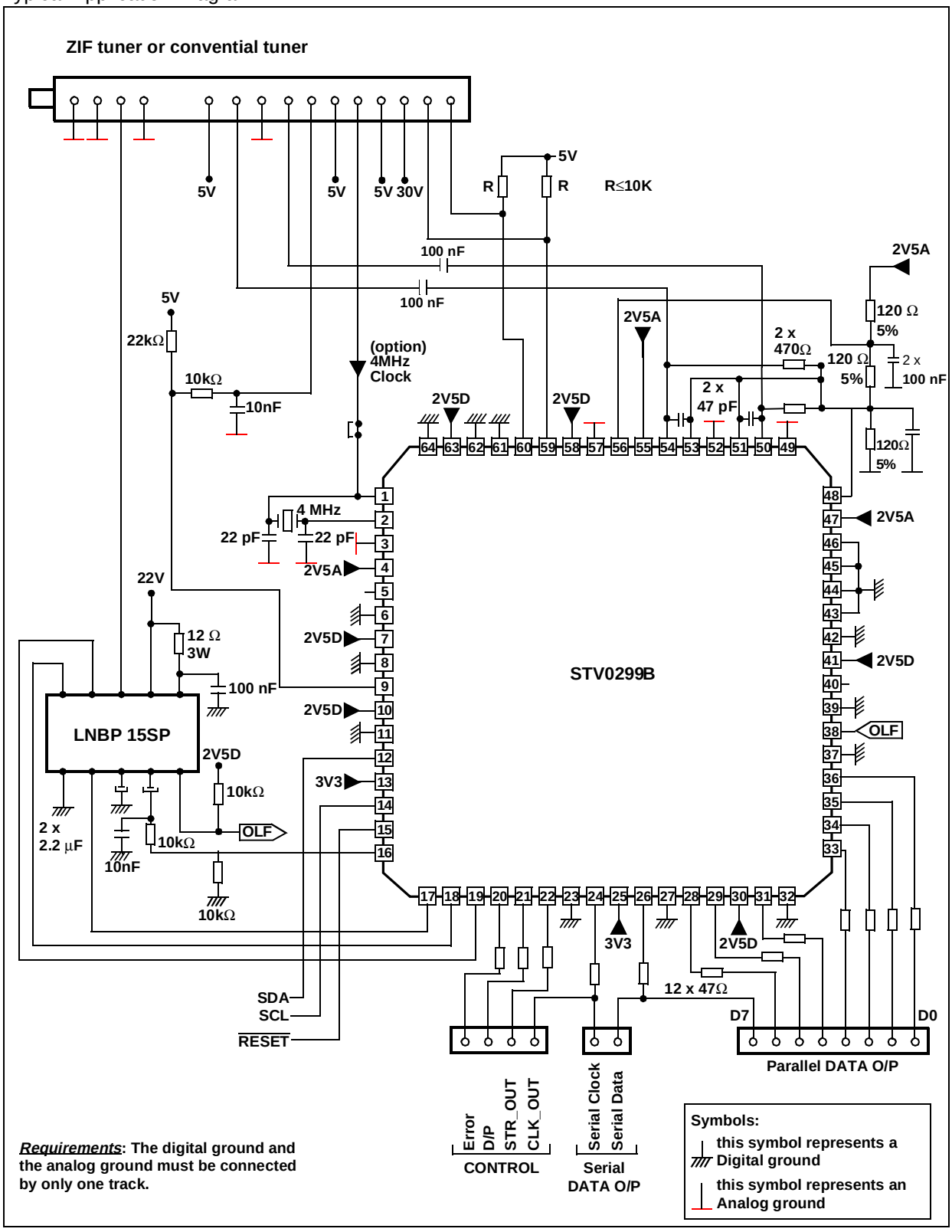
## 7 APPLICATION BLOCK DIAGRAMS

**Figure 13:** Application Block Diagram



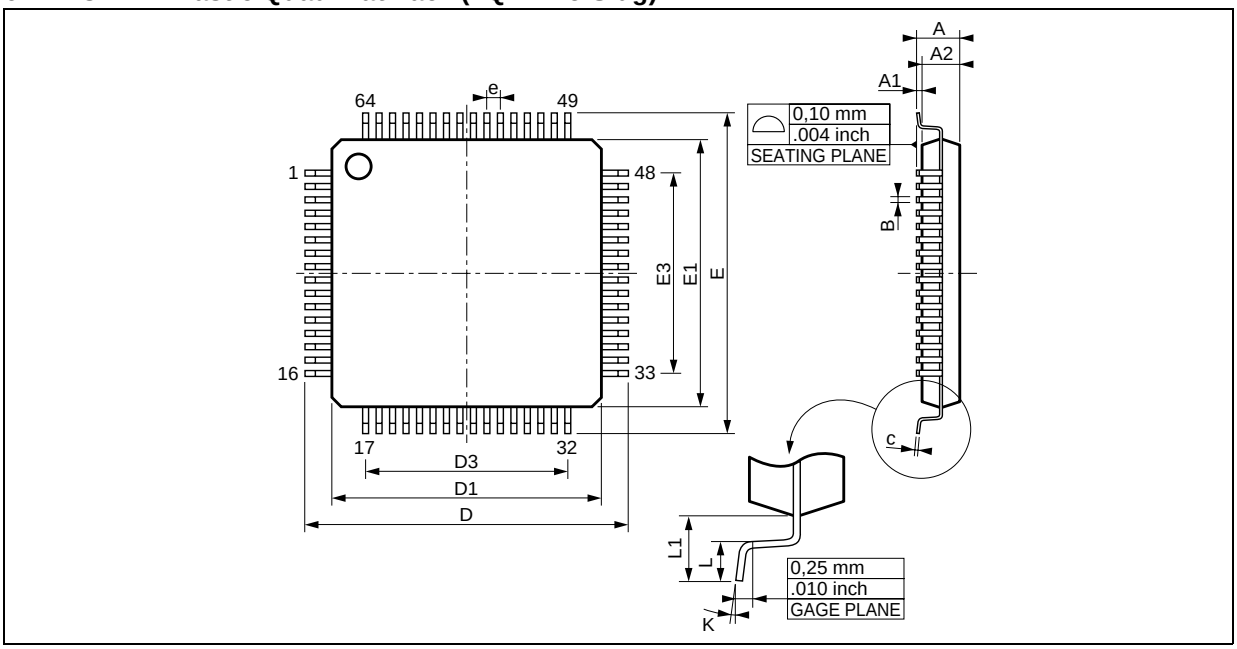
## 7 APPLICATION BLOCK DIAGRAMS (continued)

Typical Application Diagram



## 8 PACKAGE MECHANICAL DATA

### 64 Pins Thin Plastic Quad Flat Pack (TQFP No Slug)




| Dimensions | Millimeters | | | Inches | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 1.60 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| B | 0.17 | 0.22 | 0.27 | 0.007 | 0.009 | 0.011 |
| C | 0.09 | | 0.20 | 0.004 | | 0.008 |
| D | | 12.00 | | | 0.472 | |
| D1 | | 10.00 | | | 0.394 | |
| D3 | | 7.50 | | | 0.295 | |
| e | | 0.50 | | | 0.0197 | |
| E | | 12.00 | | | 0.472 | |
| E1 | | 10.00 | | | 0.394 | |
| E3 | | 7.50 | | | 0.295 | - |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | | 1.00 | | | 0.039 | |
| K | 0° (Min.), 7° (Max.) | | | | | |