EPSON

SED1565 Series

Dot Matrix LCD Driver

■ DESCRIPTION

The SED1565 Series is a series of single-chip dot matrix liquid crystal display drivers that can be connected directly to a microprocessor bus. 8-bit parallel or serial display data sent from the microprocessor is stored in the internal display data RAM and the chip generates a liquid crystal drive signal independent of the microprocessor. Because the chips in the SED1565 Series contain 65 × 132 bits of display data RAM and there is a 1-to-1 correspondence between the liquid crystal panel pixels and the internal RAM bits, these chips enable displays with a high degree of freedom.

The SED1565 Series chips contain 65 common output circuits and 132 segment output circuits, so that a single chip can drive a 65 × 132 dot display (capable of displaying 8 columns × 4 rows of a 16 × 16 dot kanji font). The SED1567 Series chips contain 33 common output circuits and 132 segment output circuits, so that a single chip can drive 33 × 132 dot display (capable of displaying 8 columns × 2 rows of 16 × 16 dot kanji fonts). Moreover, the capacity of the display can be extended through the use of master/slave structures between chips.

The chips are able to minimize power consumption because no external operating clock is necessary for the display data RAM read/write operation. Furthermore, because each chip is equipped internally with a low-power liquid crystal driver power supply, resistors for liquid crystal driver power voltage adjustment and a display clock CR oscillator circuit, the SED1565 Series chips can be used to create the lowest power display system with the fewest components for high-performance portable devices.

■ FEATURES

- Direct display of RAM data through the display data RAM.
  RAM bit data: "1" Non-illuminated
  "0" Illuminated
  (during normal display)
- RAM capacity
  65 × 132 = 8580 bits
- Display driver circuits
  SED1565***: 65 common output and 132 segment outputs
  SED1566***: 49 common output and 132 segment outputs
  SED1567***: 33 common outputs and 132 segment outputs
  SED1568***: 55 common outputs and 132 segment outputs
  SED1569***: 53 common outputs and 132 segment outputs
- High-speed 8-bit MPU interface (The chip can be connected directly to the both the 80×86 series MPUs and the 68000 series MPUs)
  /Serial interfaces are supported.
- Abundant command functions
  Display data Read/Write, display ON/OFF, Normal/Reverse display mode, page address set, display start line set, column address set, status read, display all points ON/OFF, LCD bias set, electronic volume, read/modify/write, segment driver direction select, power saver, static indicator, common output status select, V_5 voltage regulation internal resistor ratio set.
- Static drive circuit equipped internally for indicators. (1 system, with variable flashing speed.)
- Low-power liquid crystal display power supply circuit equipped internally.
  Booster circuit (with Boost ratios of Double/Triple/Quad, where the step-up voltage reference power supply can be input externally)
  High-accuracy voltage adjustment circuit (Thermal gradient –0.05%/°C or –0.2%/°C or external input)
  V_5 voltage regulator resistors equipped internally, V_1 to V_4 voltage divider resistors equipped internally, electronic volume function equipped internally, voltage follower.
- CR oscillator circuit equipped internally (external clock can also be input)

- Extremely low power consumption
  Operating power when the built-in power supply is used (an example)
  SED1565D0B /SED1565DBB: 81 µA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$ = 3.0 V, Quad voltage, $V_5 – V_{DD}$ = –11.0 V)
  SED1566D0B /SED1566DBB: 43 µA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$ = 3.0 V, Triple voltage, $V_5 – V_{DD}$ = –8.0 V)
  SED1567D0B /SED1567DBB: 29 µA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$ = 3.0 V, Triple voltage, $V_5 – V_{DD}$ = –8.0 V)
  SED1568D0B /SED1568DBB /SED1569D0B /SED1569DBB: 46 µA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$ = 3.0 V, Triple voltage, $V_5 – V_{DD}$ = –8.0 V)
  Conditions: When all displays are in white and the normal mode is selected.
- Power supply
  Operable on the low 1.8 voltage
  Logic power supply $V_{DD} – V_{SS}$ = 1.8 V to –5.5 V
  Boost reference voltage: $V_{DD} – V_{SS2}$ = 1.8 V to –6.0 V
  Liquid crystal drive power supply: $V_{DD} – V_5$ = –4.5 V to –16.0 V
- Wide range of operating temperatures: –40 to 85°C
- CMOS process
- Shipping forms include bare chip and TCP.
- These chips not designed for resistance to light or resistance to radiation.

■ SERIES SPECIFICATIONS

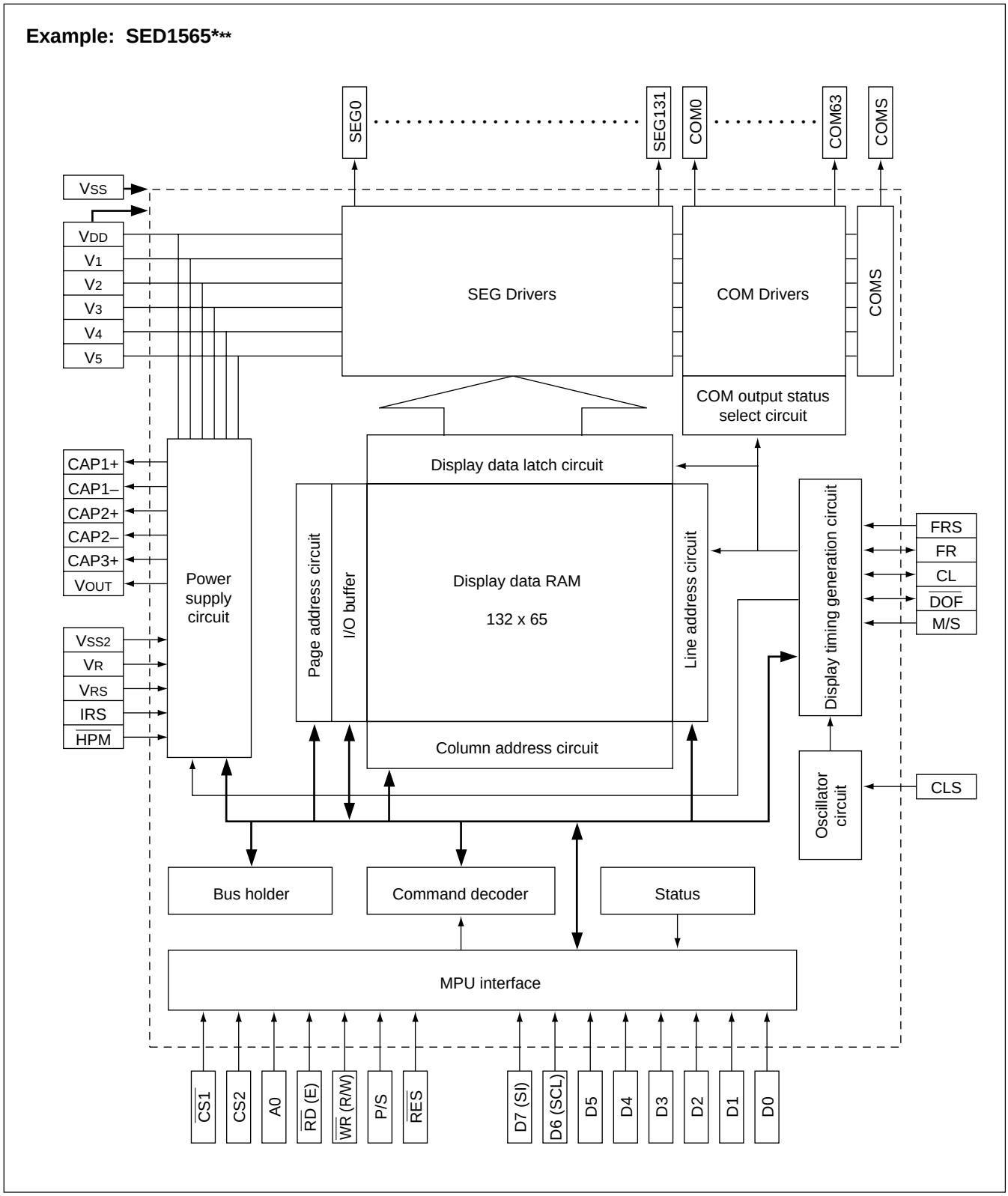
Product Name	Duty	Bias	SED Dr	COM Dr	V_{REG} Temperature Gradient	Shipping Forms
SED1565D0B /SED1565DBB	1/65	1/9, 1/7	132	65	–0.05%/°C	Bare Chip
SED1565T0*	1/65	1/9, 1/7	132	65	–0.05%/°C	TCP
* SED1565D1B	1/65	1/9, 1/7	132	65	–0.2%/°C	Bare Chip
* SED1565T1*	1/65	1/9, 1/7	132	65	–0.2%/°C	TCP
SED1565D2B	1/65	1/9, 1/7	132	65	External Input	Bare Chip
SED1565T2*	1/65	1/9, 1/7	132	65	External Input	TCP
SED1566D0B /SED1566DBB	1/49	1/8, 1/6	132	49	–0.05%/°C	Bare Chip
SED1566T0*	1/49	1/8, 1/6	132	49	–0.05%/°C	TCP
SED1566D1B	1/49	1/8, 1/6	132	49	–0.2%/°C	Bare Chip
* SED1566T1*	1/49	1/8, 1/6	132	49	–0.2%/°C	TCP
SED1566D2B	1/49	1/8, 1/6	132	49	External Input	Bare Chip
* SED1566T2*	1/49	1/8, 1/6	132	49	External Input	TCP
SED1567D0B /SED1567DBB	1/33	1/6, 1/5	132	33	–0.05%/°C	Bare Chip
SED1567T0*	1/33	1/6, 1/5	132	33	–0.05%/°C	TCP
SED1567D1B	1/33	1/6, 1/5	132	33	–0.2%/°C	Bare Chip
* SED1567T1*	1/33	1/6, 1/5	132	33	–0.2%/°C	TCP
SED1567D2B	1/33	1/6, 1/5	132	33	External Input	Bare Chip
* SED1567T2*	1/33	1/6, 1/5	132	33	External Input	TCP
SED1568D0B /SED1568DBB	1/55	1/8, 1/6	132	55	-0.05%/°C	Bare Chip
SED1569D0B /SED1569DBB	1/53	1/8, 1/6	132	53	–0.05%/°C	Bare Chip
SED1569T0*	1/53	1/8, 1/6	132	53	–0.05%/°C	TCP

Note: The circuit for the V_{REG} temperature gradient –0.2%/°C and the external input is under preparation.

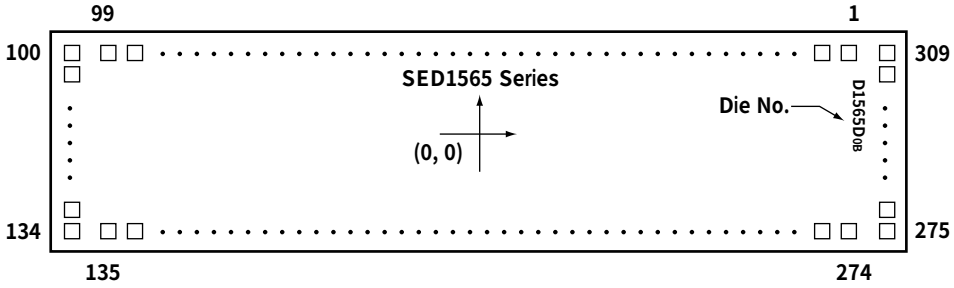
* : Under development

■ BLOCK DIAGRAM

Example: SED1565***



■ PAD LAYOUT



Chip Size	10.82 mm × 2.81 mm	
Bump Pitch	71 μm (Min.)	
Bump Size	PAD #1~24	85 μm × 85 μm
	PAD #25~82	64 μm × 85 μm
	PAD #83~99	85 μm × 85 μm
	PAD #100	85 μm × 73 μm
	PAD #101~133	85 μm × 47 μm
	PAD #134	85 μm × 73 μm
	PAD #135	73 μm × 85 μm
	PAD #136~273	47 μm × 85 μm
	PAD #274	73 μm × 85 μm
	PAD #275	86 μm × 73 μm
	PAD #276~308	85 μm × 47 μm
	PAD #309	85 μm × 73 μm
Bump Height	17 μm (Typ.)	

■ PIN DESCRIPTIONS

● Power Supply Pins

Pin Name	I/O	Function	# of Pins
V_{DD}	Power Supply	Shared with the MPU power supply terminal V_{CC}.	13
V_{SS}	Power Supply	This is a 0 V terminal connected to the system GND.	9
V_{SS2}	Power Supply	This is the reference power supply for the step-up voltage circuit for the liquid crystal drive.	4
V_{RS}	Power Supply	This is the externally-input VREG power supply for the LCD power supply voltage regulator. These are only enabled for the models with the V_{REG} external input option.	2
V_1, V_2, V_3, V_4, V_5	Power Supply	This is a multi-level power supply for the liquid crystal drive. The voltage applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on V_{DD}, and must maintain the relative magnitudes shown below. V_{DD} (= V_0) ≥ V_1 ≥ V_2 ≥ V_3 ≥ V_4 ≥ V_5 Master operation: When the power supply turns ON, the internal power supply circuits produce the V_1 to V_4 voltages shown below. The voltage settings are selected using the LCD bias set command.	10

	SED1565***		SED1566***		SED1567***		SED1569***	
V_1	1/9 • V_5	1/7 • V_5	1/8 • V_5	1/6 • V_5	1/6 • V_5	1/5 • V_5	1/8 • V_5	1/6 • V_5
V_2	2/9 • V_5	2/7 • V_5	2/8 • V_5	2/6 • V_5	2/6 • V_5	2/5 • V_5	2/8 • V_5	2/6 • V_5
V_3	7/9 • V_5	5/7 • V_5	6/8 • V_5	4/6 • V_5	4/6 • V_5	3/5 • V_5	6/8 • V_5	4/6 • V_5
V_4	8/9 • V_5	6/7 • V_5	7/6 • V_5	5/6 • V_5	5/6 • V_5	4/5 • V_5	7/8 • V_5	5/6 • V_5

● LCD Power Supply Circuit Pins

Pin Name	I/O	Function	# of Pins
CAP1+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.	2
CAP1–	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.	2
CAP2+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.	2
CAP2–	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal.	2
CAP3–	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.	2
V_{OUT}	O	DC/DC voltage converter. Connect a capacitor between this terminal and V_{SS}.	2
V_R	I	Output voltage regulator terminal. Provides the voltage between V_{DD} and V_5 through a resistive voltage divider. These are only enabled when the V_5 voltage regulator internal resistors are not used (IRS = “L”). These cannot be used when the V_5 voltage regulator internal resistors are used (IRS = “H”).	2

● **System Bus Connection Terminals**

Pin Name	I/O	Function	# of Pins
D7 to D0 (SI) (SCL)	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S = "L"), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance. When the chip select is inactive, D0 to D7 are set to high impedance.	8
A0	I	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = "H": Indicates that D0 to D7 are display data. A0 = "L": Indicates that D0 to D7 are control data.	1
$\overline{RES}$	I	When $\overline{RES}$ is set to "L," the settings are initialized. The reset operation is performed by the $\overline{RES}$ signal level.	1
$\overline{CS1}$ CS2	I	This is the chip select signal. When $\overline{CS1}$ = "L" and CS2 = "H," then the chip select becomes active, and data/command I/O is enabled.	2
$\overline{RD}$ (E)	I	• When connected to an 8080 MPU, this is active LOW. This pin is connected to the $\overline{RD}$ signal of the 8080 MPU, and the SED1565 series data bus is in an output status when this signal is "L". • When connected to a 6800 Series MPU, this is active HIGH. This is the 68000 Series MPU enable clock input terminal.	1
$\overline{WR}$ (R/$\overline{W}$)	I	• When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU $\overline{WR}$ signal. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal. • When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When R/$\overline{W}$ = "H": Read. When R/$\overline{W}$ = "L": Write.	1
C86	I	This is the MPU interface switch terminal. C86 = "H": 6800 Series MPU interface. C86 = "L": 8080 MPU interface.	1
P/S	I	This is the parallel data input/serial data input switch terminal. P/S = "H": Parallel data input. P/S = "L": Serial data input. The following applies depending on the P/S status: **P/S** / **Data/Command** / **Data** / **Read/Write** / **Serial Clock** "H" / A0 / D0 to D7 / $\overline{RD}$, $\overline{WR}$ / "L" / A0 / SI (D7) / Write only / SCL (D6) When P/S = "L", D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open. $\overline{RD}$ (E) and $\overline{WR}$ (P/$\overline{W}$) are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported.	1
CLS	I	Terminal to select whether or enable or disable the display clock internal oscillator circuit. CLS = "H": Internal oscillator circuit is enabled CLS = "L": Internal oscillator circuit is disabled (requires external input) When CLS = "L", input the display clock through the CL terminal.	1

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th># of Pins</th></tr>
<tr><td>M/S</td><td>I</td><td>This terminal selects the master/slave operation for the SED1565 Series chips. Master operation outputs the timing signals that are required for the LCD display, while slave operation inputs the timing signals required for the liquid crystal display, synchronizing the liquid crystal display system.
M/S = “H”: Master operation
M/S = “L”: Slave operation
The following is true depending on the M/S and CLS status:
<table>
<tr><th>M/S</th><th>CLS</th><th>Oscillator Circuit</th><th>Power Supply Circuit</th><th>CL</th><th>FR</th><th>FRS</th><th>DOF</th></tr>
<tr><td>“H”</td><td>“H”
“L”</td><td>Enabled
Disabled</td><td>Enabled
Enabled</td><td>Output
Input</td><td>Output
Output</td><td>Output
Output</td><td>Output
Output</td></tr>
<tr><td>“L”</td><td>“H”
“L”</td><td>Disabled
Disabled</td><td>Disabled
Disabled</td><td>Input
Input</td><td>Input
Input</td><td>Output
Output</td><td>Input
Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>This is the display clock input terminal
The following is true depending on the M/S and CLS status.
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th></tr>
<tr><td>“H”</td><td>“H”
“L”</td><td>Output
Input</td></tr>
<tr><td>“L”</td><td>“H”
“L”</td><td>Input
Input</td></tr>
</table>When the SED1565 Series chips are used in master/slave mode, the various CL terminals must be connected.</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>This is the liquid crystal alternating current signal I/O terminal.
M/S = “H”: Output
M/S = “L”: Input
When the SED1565 Series chip is used in master/slave mode, the various FR terminals must be connected.</td><td>1</td></tr>
<tr><td>$\overline{\text{DOF}}$</td><td>I/O</td><td>This is the liquid crystal display blanking control terminal.
M/S = “H”: Output
M/S = “L”: Input
When the SED1565 Series chip is used in master/slave mode, the various $\overline{\text{DOF}}$ terminals must be connected.</td><td>1</td></tr>
<tr><td>FRS</td><td>O</td><td>This is the output terminal for the static drive.
This terminal is only enabled when the static indicator display is ON when in master operation mode, and is used in conjunction with the FR terminal.</td><td>1</td></tr>
<tr><td>IRS</td><td>I</td><td>This terminal selects the resistors for the V5 voltage level adjustment.
IRS = “H”: Use the internal resistors
IRS = “L”: Do not use the internal resistors. The V5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal.
This pin is enabled only when the master operation mode is selected.
It is fixed to either “H” or “L” when the slave operation mode is selected.</td><td>1</td></tr>
<tr><td>$\overline{\text{HPM}}$</td><td>I</td><td>This is the power control terminal for the power supply circuit for liquid crystal drive.
$\overline{\text{HPM}}$ = “H”: Normal mode
$\overline{\text{HPM}}$ = “L”: High power mode
This pin is enabled only when the master operation mode is selected.
It is fixed to either “H” or “L” when the slave operation mode is selected.</td><td>1</td></tr>
</table>

● Liquid Crystal Drive Pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th># of Pins</th></tr>
<tr><td>SEG0
to
SEG131</td><td>O</td><td>These are the liquid crystal segment drive outputs. Through a combination of the contents of the display RAM and with the FR signal, a single level is selected from V_{DD}, V_2, V_3, and V_5.
<table>
<tr><th>RAM DATA</th><th>FR</th><th colspan="2">Output Voltage</th></tr>
<tr><td></td><td></td><td>Normal Display</td><td>Reverse Display</td></tr>
<tr><td>H</td><td>H</td><td>V_{DD}</td><td>V_2</td></tr>
<tr><td>H</td><td>L</td><td>V_5</td><td>V_3</td></tr>
<tr><td>L</td><td>H</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>L</td><td>V_3</td><td>V_5</td></tr>
<tr><td>Power save</td><td>—</td><td colspan="2">V_{DD}</td></tr>
</table></td><td>132</td></tr>
<tr><td>COM0
to
COM31</td><td>O</td><td>These are the liquid crystal common drive outputs.
<table>
<tr><th>Part No.</th><th>COM</th></tr>
<tr><td>SED1565*** </td><td>COM 0 to COM 63</td></tr>
<tr><td>SED1566*** </td><td>COM 0 to COM 47</td></tr>
<tr><td>SED1567*** </td><td>COM 0 to COM 31</td></tr>
<tr><td>SED1568*** </td><td>COM 0 to COM 53</td></tr>
<tr><td>SED1569*** </td><td>COM 0 to COM 51</td></tr>
</table>
<table>
<tr><th>Part No.</th><th></th></tr>
<tr><td>SED1565*** </td><td>64</td></tr>
<tr><td>SED1566*** </td><td>48</td></tr>
<tr><td>SED1567*** </td><td>32</td></tr>
<tr><td>SED1568*** </td><td>54</td></tr>
<tr><td>SED1569*** </td><td>52</td></tr>
</table>
Through a combination of the contents of the scan data and with the FR signal, a single level is selected from V_{DD}, V_1, V_4, and V_5.
<table>
<tr><th>Scan Data</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td>H</td><td>H</td><td>V_5</td></tr>
<tr><td>H</td><td>L</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>H</td><td>V_1</td></tr>
<tr><td>L</td><td>L</td><td>V_4</td></tr>
<tr><td>Power Save</td><td>—</td><td>V_{DD}</td></tr>
</table></td><td>64</td></tr>
<tr><td>COMS</td><td>O</td><td>These are the COM output terminals for the indicator. Both terminals output the same signal.
Leave these open if they are not used.
When in master/slave mode, the same signal is output by both master and slave.</td><td>2</td></tr>
</table>

● Test Terminals

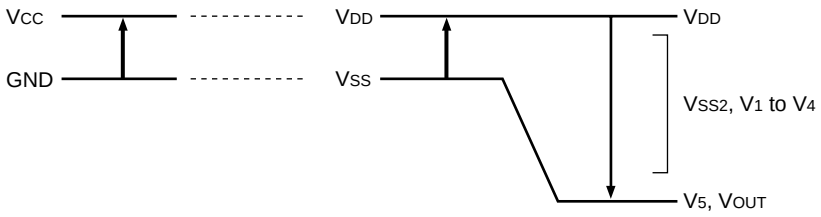
Pin Name	I/O	Function	No. of Pins
TEST0 to 9	I/O	These are terminals for IC chip testing. They are set to OPEN.	14

Total: 288 pins for the SED1565***.
272 pins for the SED1566***.
256 pins for the SED1567***.
276 pins for the SED1569***.

■ ABSOLUTE MAXIMUM RATINGS

Unless otherwise noted, V_{SS} = 0 V

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		V_{DD}	–0.3 to +7.0	V
Power supply voltage (2) (V_{DD} standard)	With Triple step-up With Quad step-up	V_{SS2}	–7.0 to +0.3 –6.0 to +0.3 –4.5 to +0.3	V
Power supply voltage (3) (V_{DD} standard)		V_5, V_{OUT}	–18.0 to +0.3	V
Power supply voltage (4) (V_{DD} standard)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	–0.3 to V_{DD} + 0.3	V
Output voltage		V_O	–0.3 to V_{DD} + 0.3	V
Operating temperature		T_{OPR}	–40 to +85	°C
Storage temperature	TCP Bare chip	T_{STR}	–55 to +100 –55 to +125	°C



Notes and Cautions

1. The V_{SS2}, V_1 to V_5 and V_{OUT} are relative to the V_{DD} = 0V reference.
2. Insure that the voltage levels of V_1, V_2, V_3, and V_4 are always such that $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

■ DC CHARACTERISTICS

Unless otherwise specified, V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, Ta = –40 to 85°C

Item		Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Units	Applicable Pin
Operating Voltage (1)	Recommended Voltage	V_{DD}			2.7	—	3.3	V	V_{DD}*1
	Possible Operating Voltage				1.8	—	5.5	V	V_{DD}*1
Operating Voltage (2)	Recommended Voltage	V_{SS2}	(Relative to V_{DD})		–3.3	—	–2.7	V	V_{SS2}
	Possible Operating Voltage	V_{SS2}	(Relative to V_{DD})		–6.0	—	–1.8	V	V_{SS2}
Operating Voltage (3)	Possible Operating Voltage	V_5	(Relative to V_{DD})		–16.0	—	–4.5	V	V_5 *2
	Possible Operating Voltage	V_1, V_2	(Relative to V_{DD})		0.4 × V_5	—	V_{DD}	V	V_1, V_2
	Possible Operating Voltage	V_3, V_4	(Relative to V_{DD})		V_5	—	0.6 × V_5	V	V_3, V_4
High-level Input Voltage Low-level Input Voltage		V_{IHC} V_{ILC}			0.8 × V_{DD} V_{SS}	— —	V_{DD} 0.2 × V_{DD}	V V	*3 *3
High-level Output Voltage Low-level Output Voltage		V_{OHC} V_{OLC}	I_{OH} = –0.5 mA I_{OL} = 0.5 mA		0.8 × V_{DD} V_{SS}	— —	V_{DD} 0.2 × V_{DD}	V V	*4 *4
Input leakage current Output leakage current		I_{LI} I_{LO}	V_{IN} = V_{DD} or V_{SS}		–1.0 –3.0	— —	1.0 3.0	µA µA	*5 *6
Liquid Crystal Driver ON Resistance		R_{ON}	Ta = 25°C (Relative To V_{DD})	V_5 = –14.0 V V_5 = –8.0 V	— —	2.0 3.2	3.5 5.4	KΩ KΩ	SEGn COMn *7
Static Consumption Current Output Leakage Current		I_{SSQ} I_{5Q}	V_5 = –18.0 V (Relative To V_{DD})		— —	0.01 0.01	5 15	µA µA	V_{SS}, V_{SS2} V_5
Input Terminal Capacitance		C_{IN}	Ta = 25°C f = 1 MHz		—	5.0	8.0	pF	
Oscillator Frequency	Internal Oscillator	f_{OSC}	Ta = 25°C		18	22	26	kHz	*8
	External Input	f_{CL}	SED1565★**/1567★**		18	22	26	kHz	CL
	Internal Oscillator	f_{OSC}	Ta = 25°C		27	33	39	kHz	*8
	External Input	f_{CL}	SED1566★**/1569★**		14	17	20	kHz	CL
Internal Power	Input voltage	V_{SS2} V_{SS2}	With Triple (Relative To V_{DD}) With Quad (Relative To V_{DD})		–6.0 –4.5	— —	–1.8 –1.8	V V	V_{SS2} V_{SS2}
	Supply Step-up output voltage Circuit	V_{OUT}	(Relative to V_{DD})		–18.0	—	—	V	V_{OUT}
	Voltage regulator Circuit Operating Voltage	V_{OUT}	(Relative to V_{DD})		–18.0	—	–6.0	V	V_{OUT}
	Voltage Follower Circuit Operating Voltage	V_5	(Relative to V_{DD})		–16.0	—	–4.5	V	V_5 *9
	Base Voltage	V_{REG0} V_{REG1}	Ta = 25°C (Relative to V_{DD})	–0.05%/°C –0.2%/°C	–2.16 –5.15	–2.10 –4.9	–2.04 –4.65	V V	*10 *10

- Dynamic Consumption Current (1), During Display, with the Internal Power Supply OFF Current consumed by total ICs when an external power supply is used.

Display Pattern OFF

Ta = 25°C

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
SED1565★**	I_{DD} (1)	V_{DD} = 5.0 V, $V_5 - V_{DD}$ = –11.0 V	—	18	30	µA	*11
		V_{DD} = 3.0 V, $V_5 - V_{DD}$ = –11.0 V	—	16	27		
SED1566★**		V_{DD} = 3.0 V, $V_5 - V_{DD}$ = –11.0 V	—	13	22		
		V_{DD} = 5.0 V, $V_5 - V_{DD}$ = –8.0 V	—	11	19		
		V_{DD} = 3.0 V, $V_5 - V_{DD}$ = –8.0 V	—	9	15		
SED1567★**		V_{DD} = 5.0 V, $V_5 - V_{DD}$ = –8.0 V	—	8	13		
		V_{DD} = 3.0 V, $V_5 - V_{DD}$ = –8.0 V	—	7	12		
SED1568★**/SED1569★**		V_{DD} = 5.0 V, $V_5 - V_{DD}$ = –8.0 V	—	12	20		
		V_{DD} = 3.0 V, $V_5 - V_{DD}$ = –8.0 V	—	10	17		

Display Pattern Checker

Ta = 25°C

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
SED1565★**	I_{DD} (1)	V_{DD} = 5.0 V, $V_5 - V_{DD}$ = –11.0 V	—	23	38	µA	*11
		V_{DD} = 3.0 V, $V_5 - V_{DD}$ = –11.0 V	—	21	35		
SED1566★**		V_{DD} = 3.0 V, $V_5 - V_{DD}$ = –11.0 V	—	17	29		
		V_{DD} = 5.0 V, $V_5 - V_{DD}$ = –8.0 V	—	14	24		
		V_{DD} = 3.0 V, $V_5 - V_{DD}$ = –8.0 V	—	12	20		
SED1567★**		V_{DD} = 5.0 V, $V_5 - V_{DD}$ = –8.0 V	—	11	18		
		V_{DD} = 3.0 V, $V_5 - V_{DD}$ = –8.0 V	—	10	17		
SED1568★**/SED1569★**		V_{DD} = 5.0 V, $V_5 - V_{DD}$ = –8.0 V	—	15	25		
		V_{DD} = 3.0 V, $V_5 - V_{DD}$ = –8.0 V	—	13	22		

- Dynamic Consumption Current (2), During Display, with the Internal Power Supply ON

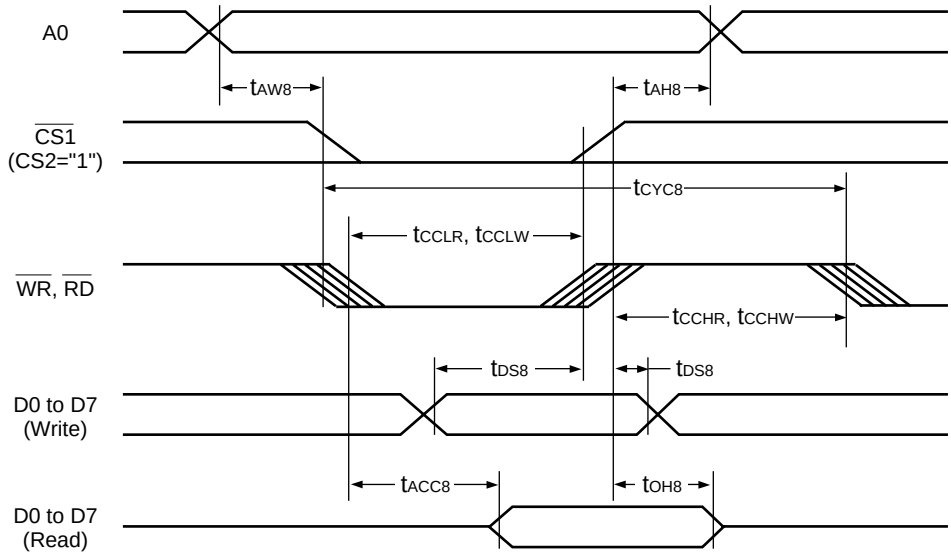
Display Pattern OFF

Ta = 25°C

Item	Symbol	Condition		Rating			Units	Notes
				Min.	Typ.	Max.		
SED1565★**	I_{DD} (2)	V_{DD} = 5.0 V, Triple step-up voltage. $V_5 - V_{DD}$ = –11.0 V	Normal Mode	—	67	112	µA	*12
			High-Power Mode	—	114	190		
		V_{DD} = 3.0 V, Quad step-up voltage. $V_5 - V_{DD}$ = –11.0 V	Normal Mode	—	81	135		
			High-Power Mode	—	138	230		
SED1566★**		V_{DD} = 5.0 V, Double step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	35	59		
			High-Power Mode	—	64	107		
		V_{DD} = 3.0 V, Triple step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	43	72		
			High-Power Mode	—	84	140		
		V_{DD} = 3.0 V, Quad step-up voltage. $V_5 - V_{DD}$ = –11.0 V	Normal Mode	—	72	121		
			High-Power Mode	—	128	214		
SED1567★**		V_{DD} = 5.0 V, Double step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	26	44		
			High-Power Mode	—	60	100		
		V_{DD} = 3.0 V, Triple step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	29	49		
			High-Power Mode	—	73	122		
SED1568★** / SED1569★**		V_{DD} = 5.0 V, Double step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	37	62		
			High-Power Mode	—	67	112		
		V_{DD} = 3.0 V, Triple step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	46	77		
			High-Power Mode	—	87	145		

■ TIMING CHARACTERISTICS

● System Bus Read/Write Characteristics 1 (for the 8080 Series MPU)



(VDD = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t_{AH8}	—	0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time	A0	t_{CYC8}	—	166	—	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}	—	30	—	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		70	—	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		30	—	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		30	—	ns
Data setup time	D0 to D7	t_{DS8}	—	30	—	ns
Address hold time		t_{DH8}		10	—	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100 pF	—	70	ns
Output disable time		t_{OH8}		5	50	ns

(VDD = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t_{AH8}	—	0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time	A0	t_{CYC8}	—	300	—	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}	—	60	—	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		120	—	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		60	—	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		60	—	ns
Data setup time	D0 to D7	t_{DS8}	—	40	—	ns
Address hold time		t_{DH8}		15	—	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100 pF	—	140	ns
Output disable time		t_{OH8}		10	100	ns

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

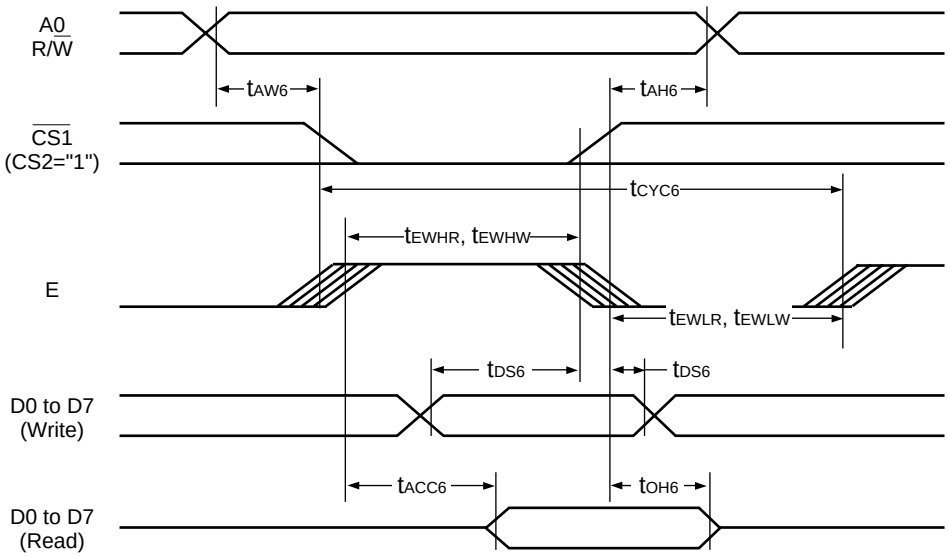
Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t_{AH8}	—	0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time	A0	t_{CYC8}	—	1000	—	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}	—	120	—	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		240	—	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		120	—	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		120	—	ns
Data setup time	D0 to D7	t_{DS8}	—	80	—	ns
Address hold time		t_{DH8}		30	—	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100 pF	—	280	ns
Output disable time		t_{OH8}		10	200	ns

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≤ ($t_{CYC8} – t_{CCLW} – t_{CCHW}$) for ($t_r + t_f$) ≤ ($t_{CYC8} – t_{CCLR} – t_{CCHR}$) are specified.

*2 All timing is specified using 20% and 80% of V_{DD} as the reference.

*3 t_{CCLW} and t_{CCLR} are specified as the overlap between $\overline{CS1}$ being "L" (CS2 = "H") and $\overline{WR}$ and $\overline{RD}$ being at the "L" level.

● System Bus Read/Write Characteristics 2 (6800 Series MPU)



(V_{DD} = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min	Max	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}	—	0 0	— —	ns ns
System cycle time		A0	t_{CYC6}	—	166	—	ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}	—	30 10	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	C_L = 100 pF	— 10	70 50	ns ns
Enable H pulse time	Read Write	E	t_{CCLW} t_{CCLR}	—	70 30	— —	ns ns
Enable L pulse time	Read Write	E	t_{CCHW} t_{CCHR}	—	30 30	— —	ns ns

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min	Max	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}	—	0 0	— —	ns ns
System cycle time		A0	t_{CYC6}	—	300	—	ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}	—	40 15	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	C_L = 100 pF	— 10	140 100	ns ns
Enable H pulse time	Read Write	E	t_{CCLW} t_{CCLR}	—	120 60	— —	ns ns
Enable L pulse time	Read Write	E	t_{CCHW} t_{CCHR}	—	60 60	— —	ns ns

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

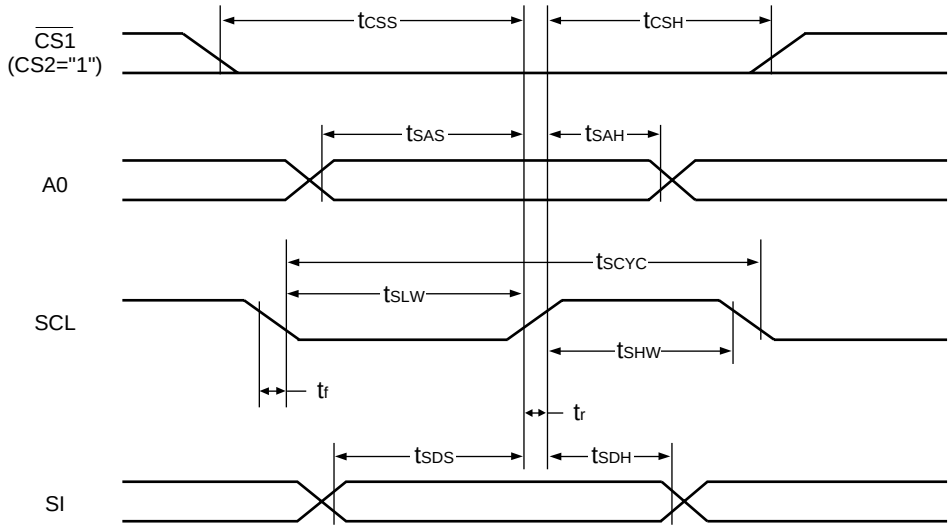
Item		Signal	Symbol	Condition	Rating		Units
					Min	Max	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}	—	0 0	— —	ns ns
System cycle time		A0	t_{CYC6}	—	1000	—	ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}	—	80 30	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	C_L = 100 pF	— 10	280 200	ns ns
Enable H pulse time	Read Write	E	t_{CCLW} t_{CCLR}	—	240 120	— —	ns ns
Enable L pulse time	Read Write	E	t_{CCHW} t_{CCHR}	—	120 120	— —	ns ns

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≤ ($t_{CYC6} – t_{EWLW} – t_{EWHW}$) for ($t_r + t_f$) ≤ ($t_{CYC6} – t_{EWLR} – t_{EWHR}$) are specified.

*2 All timing is specified using 20% and 80% of V_{DD} as the reference.

*3 t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being “L” (CS2 = “H”) and E.

● **Serial Interface**



(VDD = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Serial Clock Period	SCL	t_{SCYC}	—	200	—	ns
SCL “H” pulse width		t_{SHW}		75	—	ns
SCL “L” pulse width		t_{SLW}		75	—	ns
Address setup time	A0	t_{SAS}	—	50	—	ns
Address hold time		t_{SAH}		100	—	ns
Data setup time	SI	t_{SDS}	—	50	—	ns
Data hold time		t_{SDH}		50	—	ns
CS-SCL time	CS	t_{CSS}	—	100	—	ns
		t_{CSH}		100	—	ns

(VDD = 2.7 V to 4.5 V, Ta = –40 to 85°C)

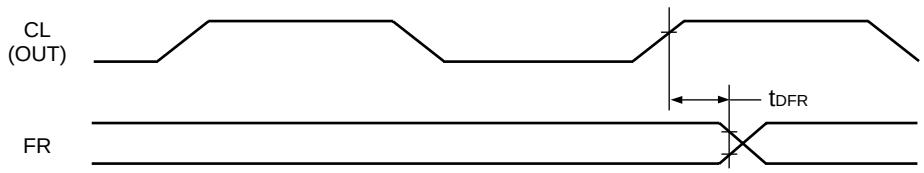
Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Serial Clock Period	SCL	t_{SCYC}	—	250	—	ns
SCL “H” pulse width		t_{SHW}		100	—	ns
SCL “L” pulse width		t_{SLW}		100	—	ns
Address setup time	A0	t_{SAS}	—	150	—	ns
Address hold time		t_{SAH}		150	—	ns
Data setup time	SI	t_{SDS}	—	100	—	ns
Data hold time		t_{SDH}		100	—	ns
CS-SCL time	CS	t_{CSS}	—	150	—	ns
		t_{CSH}		150	—	ns

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Serial Clock Period	SCL	t_{SCYC}	—	400	—	ns
SCL “H” pulse width		t_{SHW}		150	—	ns
SCL “L” pulse width		t_{SLW}		150	—	ns
Address setup time	A0	t_{SAS}	—	250	—	ns
Address hold time		t_{SAH}		250	—	ns
Data setup time	SI	t_{SDS}	—	150	—	ns
Data hold time		t_{SDH}		150	—	ns
CS-SCL time	CS	t_{CSS}	—	250	—	ns
		t_{CSH}		250	—	ns

*1 The input signal rise and fall time (t_r, t_f) are specified at 15 ns or less.
*2 All timing is specified using 20% and 80% of V_{DD} as the standard.

● Display Control Output Timing



(V_{DD} = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time	FR	t_{DFR}	C_L = 50 pF	—	10	40	ns

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

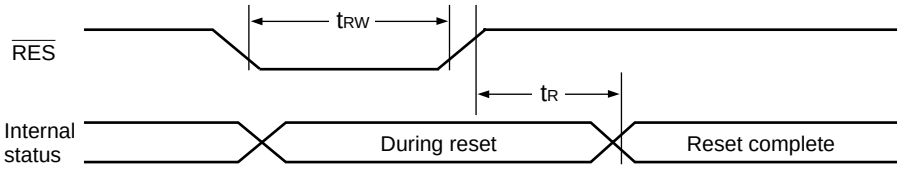
Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time	FR	t_{DFR}	C_L = 50 pF	—	20	80	ns

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time	FR	t_{DFR}	C_L = 50 pF	—	50	200	ns

*1 Valid only when the master mode is selected.
*2 All timing is based on 20% and 80% of V_{DD}.

● Reset Timing



(VDD = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time		t_R	—	—	—	0.5	µs
Reset "L" pulse width	RES	t_{RW}		0.5	—	—	µs

(VDD = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time		t_R	—	—	—	1	µs
Reset "L" pulse width	RES	t_{RW}		1	—	—	µs

(VDD = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time		t_R	—	—	—	1.5	µs
Reset "L" pulse width	RES	t_{RW}		1.5	—	—	µs

*1 All timing is specified with 20% and 80% of VDD as the standard.

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION
IC Marketing & Engineering Group

ED International Marketing Department I (Europe, U.S.A)
421-8 Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: 042-587-5812 FAX: 042-587-5564

ED International Marketing Department II (ASIA)
421-8 Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: 042-587-5814 FAX: 042-587-5110

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