19-2481; Rev 0; 6/02

MAX3952 Evaluation Kit

Evaluates: MAX3952

General Description

The MAX3952 evaluation kit (EV kit) is an assembled surface-mount demonstration board that provides easy evaluation of the MAX3952 10Gbps 16:1 serializer with clock synthesis.

Features

- **+3.3V Single Supply**
- **Jumper-Enabled 2^7 - 1 On-Chip PRBS Generation**
- **Selectable Reference Clock Frequencies (644.53MHz, 161.1MHz, 155.52MHz, 622.08MHz)**
- **Fully Assembled and Tested**

Component List

DESIGNATION	QTY	DESCRIPTION
C1–C8, C10, C25–C29, C32, C33, C34, C42, C55	19	0.1µF ±10% ceramic capacitors (0402)
C11–C21, C23, C24, C30, C31, C35–C41, C43–C54	34	DO NOT INSTALL
C9, C22	2	10µF tantalum capacitors ±10% AVX TAJB106K010
R3–R6	4	DO NOT INSTALL
R12–R17, R19, R22, R23, R27, R54, R56	12	0Ω resistors (0402)
R7, R43	2	768Ω ±1% resistors (0402)
R2, R57	2	30kΩ ±5% resistors (0402)
R8–R11, R18, R20, R21, R24, R25, R26, R28–R42, R44–R52	34	2kΩ ±1% resistors (0402)
R53, R55	2	25.5kΩ ±1% resistors (0402)
R1	1	100Ω ±5% resistor (0201)
L1, L2, L3	3	56 nH inductors Coilcraft0603CS-56NXJBW
D1, D2	2	Red LEDs
J1–J6, J27, J28	8	SMA connectors, edgemount, tab centers EFJohnson 142-0701-851
J9–J20, J22–J25, J29–J48	36	SMB connectors EFJohnson 131-1701-201
JU10, JU36, JU39, JU40	4	1×2 pin headers, 0.1” centers
JU1–JU9, JU11–JU14, JU17–JU35, JU37, JU38, JU41, JU45, JU56	34	1×3 pin headers, 0.1” centers
JU2–JU9, JU11–JU14, JU17–JU35, JU37, JU38, JU41, JU45, JU56	34	1×1 pin headers, 0.1” centers
JU1–JU12, JU17, JU21, JU25, JU41, JU45, JU53, JU54, JU55	31	shunts Digi-Key S9000-ND
U1	1	MAX3952EGK 68-pin QFN
U2	1	MAX4429ESA 8-pin SO
J7, J8, J21, J26	4	Test points Digi-Key 5000K-ND
–	1	MAX3952 evaluation kit
–	1	MAX3952 data sheet

Ordering Information

PART	TEMP RANGE	IC PACKAGE
MAX3952EVKIT	-40°C to +85°C	68 QFN-EP

MAX3952 Evaluation Kit

Quick Start

1) This quick start assumes that the board has the shunts removed from all the jumpers.
2) With JU38 open, the MAX3952 operates with a 622.08MHz reference clock. Refer to Table 1 in the MAX3952 data sheet to configure the board for other reference clock frequencies.
3) Apply a 622.08MHz reference clock to the REFCLK± inputs at J1 and J2.
4) Connect the PCLKO± outputs at J27 and J28 to the PCLKI± inputs. Ensure that polarities match.
5) Enable the on-chip pattern generator by using JU56 to connect PRBSEN to V_{CC}.
6) Connect the SDO± and SCLK± outputs at connectors J3–J6 to a high-speed, 50Ω terminated oscilloscope. Use matched cable lengths for accurate timing measurements and best performance.
7) Enable the serial output clock using JU1 to connect SCLKEN to V_{CC}. Connect the middle pin of JU14 to GND for normal operation. Place a shunt at JU36 to connect FIFO_ERROR to FIFO_RESET.
8) Power up the MAX3952 by placing +3.3V on J7 and GND to J8. J21 and J26 are used only if the LVDS inputs are AC-coupled and a separate common mode voltage is required.

Component Suppliers

SUPPLIER	PHONE	FAX
AVX	843-444-2863	843-626-3123
Coilcraft	847-639-6400	847-639-1469
Murata	415-964-6321	415-964-8165

Note: *Please indicate that you are using the MAX3952 when ordering from these suppliers*

Adjustment and Control Descriptions (see Quick Start first)

COMPONENT	NAME	FUNCTION
JU1	SCLKEN	Connect to V_{CC} to enable serial clock.
JU56	PRBSEN	Enables the internal 2^7 - 1 PRBS generator. Connect to V_{CC} to enable, to GND to disable.
JU38	CKSET	Open ⇒ 622 MHz V_{CC} ⇒ 644MHz GND ⇒ 155MHz 30kΩ to GND ⇒161MHz See Figure 4, or refer to in Table 1 in the MAX3952 data sheet
JU36	FIFO_ERROR	Shunt to Connect FIFO_ERROR to FIFO_RESET.
JU13	FIFO_RESET	Connecting FIFO_RESET to V_{CC} resets the FIFO. Placing a shunt at JU36 and leaving JU13 open is recommended for normal operation.
JU10	Common-Mode Voltage (CMV)	Place a shunt at JU10 for normal operation. This connects the CMV to GND through 25.5kΩ.
JU39, JU40	Connect PCLKI± to CMV	Connects the PCLKI± inputs to the CMV through 2.0kΩ. Leave open for normal operation.
Jumpers on PDI_± Inputs	Allows for Static Inputs	When parallel inputs are not available, use these jumpers to set static levels on the 16 LVDS Data inputs. See Figures 1 and 2 for instructions.

Detailed Description

The MAX3952 EV kit simplifies evaluation of the MAX3952. The EV kit operates from a +3.3V single supply and includes all the external components necessary to interface with LVDS, CML, and LVPECL inputs/outputs of the MAX3952. The LVPECL inputs (REFCLK±) are externally terminated with 100Ω resistors. The LVDS inputs (PDI±, PCLKI±) are internally terminated with 100Ω differential input resistance and therefore do not require external termination. Ensure that LVDS devices driving these inputs are not redundantly terminated. The CML outputs (SDO±, SCLKO±) are optimized to drive a 50Ω load. PCLKO±, SDO±, SCLKO±, and REFCLK± are AC-coupled with 0.1µF capacitors. The LVDS data and clock inputs are DC-coupled, but the lines can be cut and pads are available to allow the placement of AC-coupling capacitors. (See Figure 2)

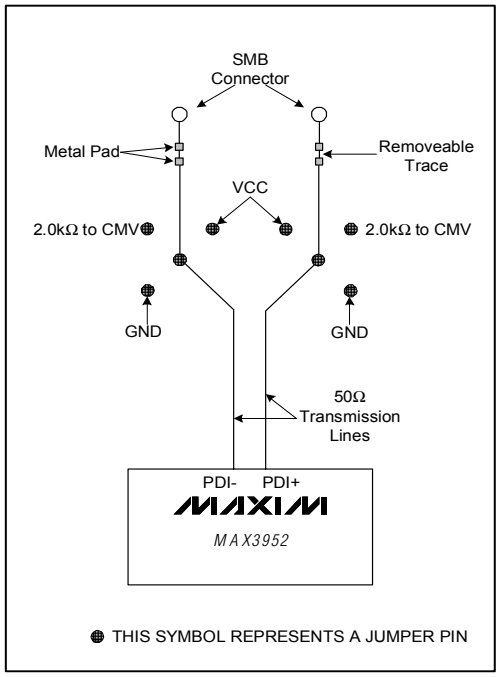

Figure 1. Detail of PDI± Inputs

Setting Static inputs with jumpers

To set static levels on the parallel data inputs, refer to Figures 1 and 2. For example, to place a static "1" on PDI0, the inverted input must be connected to GND, and the non-inverted connected to V_{CC}.

Driving AC-Coupled Signals for PDI_±

1) Follow the quick start on page 2.
2) Ensure that no shunt is installed at JU10.
3) Cut the removable traces for all of the PDI_± and PCLKI± inputs and install 0.1µF capacitors. (See Figure 2)
4) Place shunts at JU39 and JU40.
5) For all PDI_± inputs, place a shunt in the 2.0kΩ to CMV position. (See Figure 2)
6) Place 1.2V (the common mode voltage) at J21 and ground at J26.

Recommendations for Interconnect Between the MAX3952EV Kit and an Oscilloscope:

Use a high-bandwidth sampling oscilloscope. Maxim recommends the Tektronix CSA8000 mainframe with an 80E01 50GHz sampling head. The 80E03 and 80E04 20GHz sampling heads are not recommended.

The total path length from the EV kit to the oscilloscope should to be minimized. If cables must be used, 0.141in semi-rigid 50Ω coaxial cable with high quality SMA connectors are recommended. Example: Tektronix part # 015-1015-00

Exposed Pad Package

The exposed pad (EP) 68-pin QFN incorporates features that provide a very low thermal resistance path for heat removal from the IC, either to a PC board or to an external heat sink. The MAX3952's EP must be soldered directly to a ground plane with good thermal conductance.

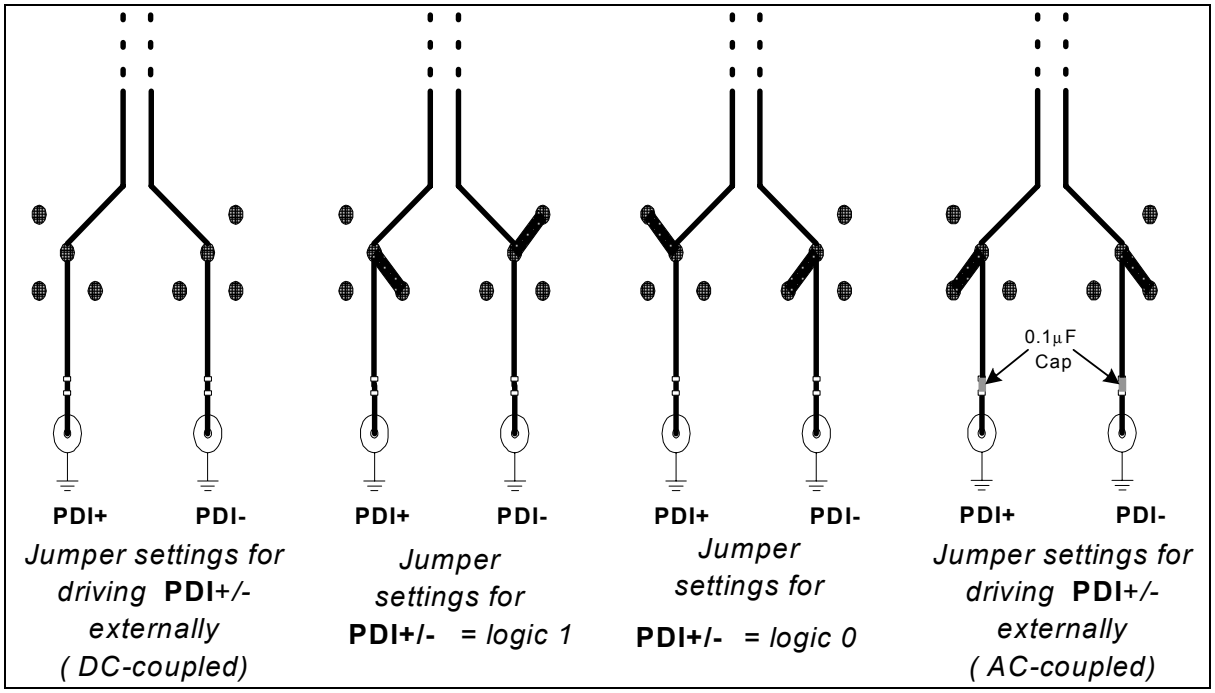

Figure 2. PDI± Jumper Settings

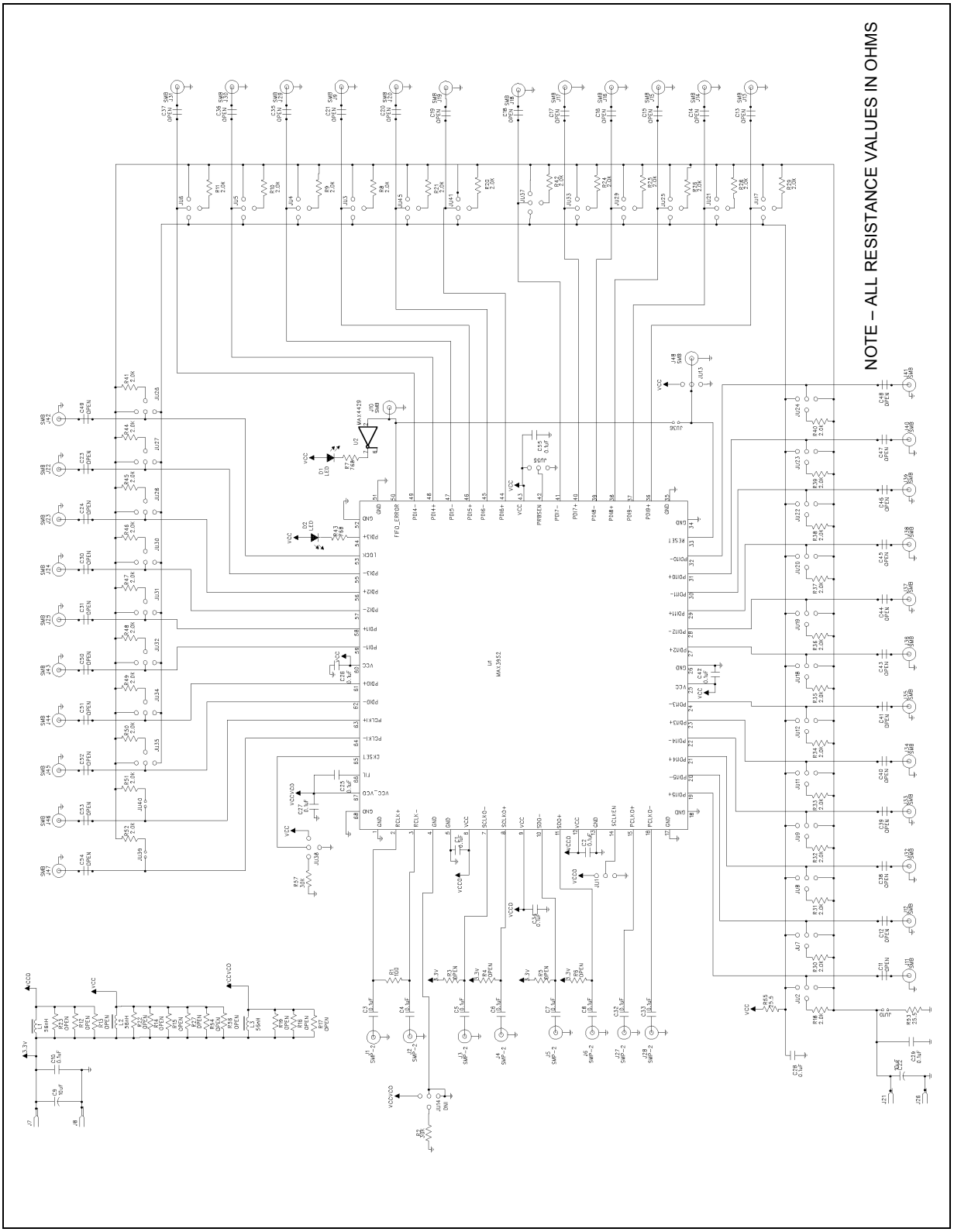

Figure 3. MAX3952 EV Kit Schematic

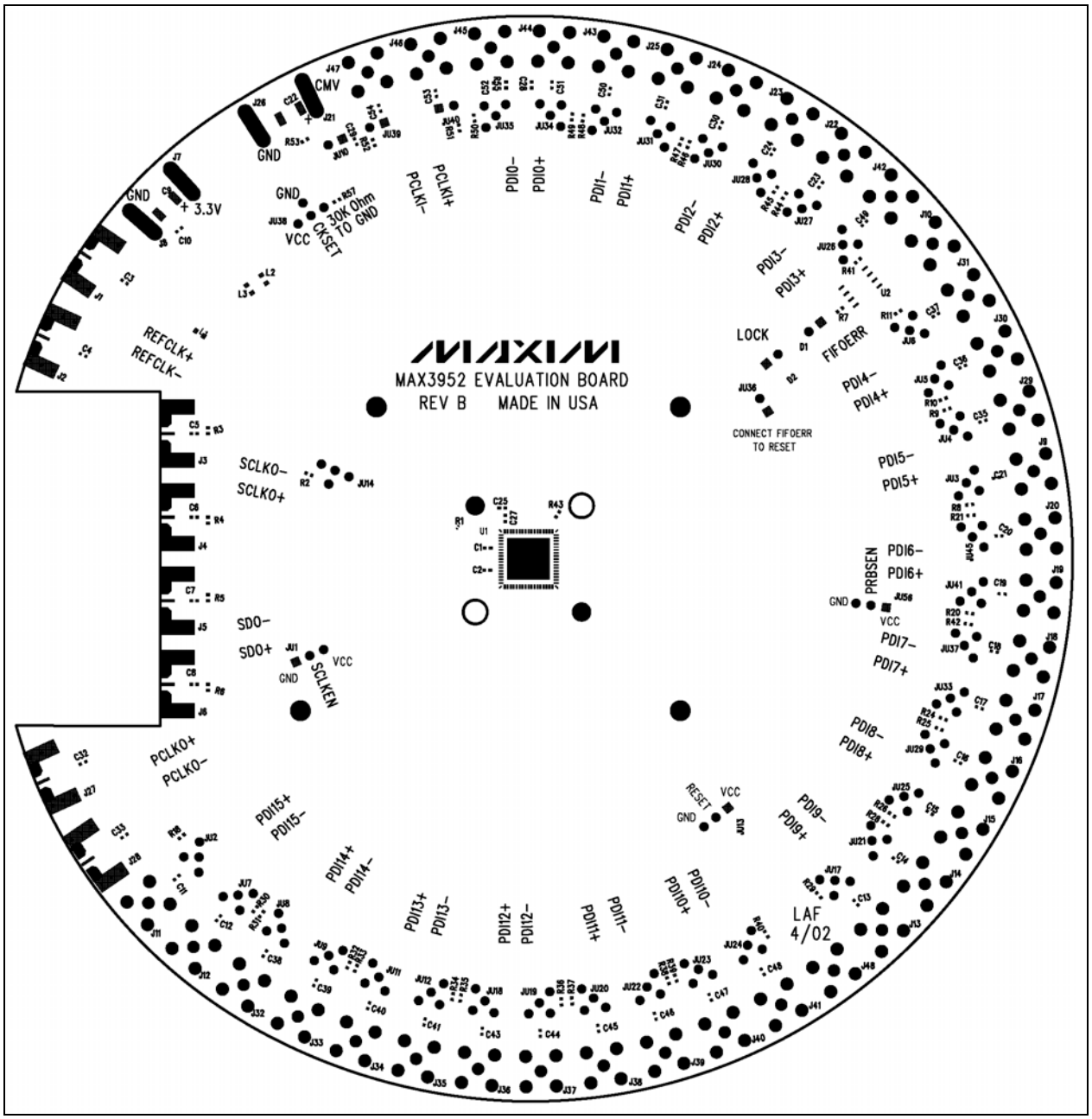

Figure 4. MAX3952 EV Kit Placement Guide–Component Side

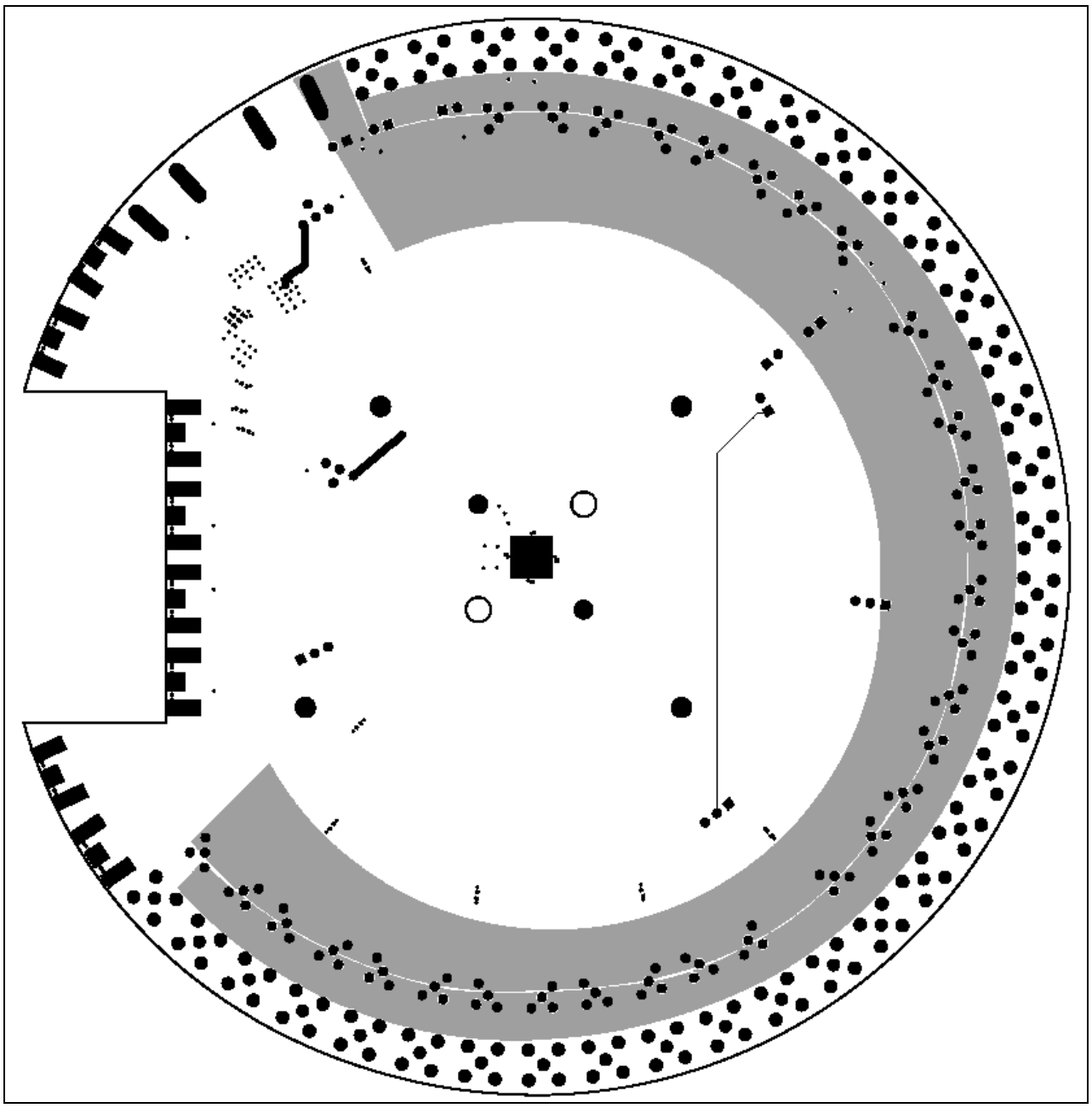

Figure 5. MAX3952 EV Kit Component Placement Guide–Solder Side

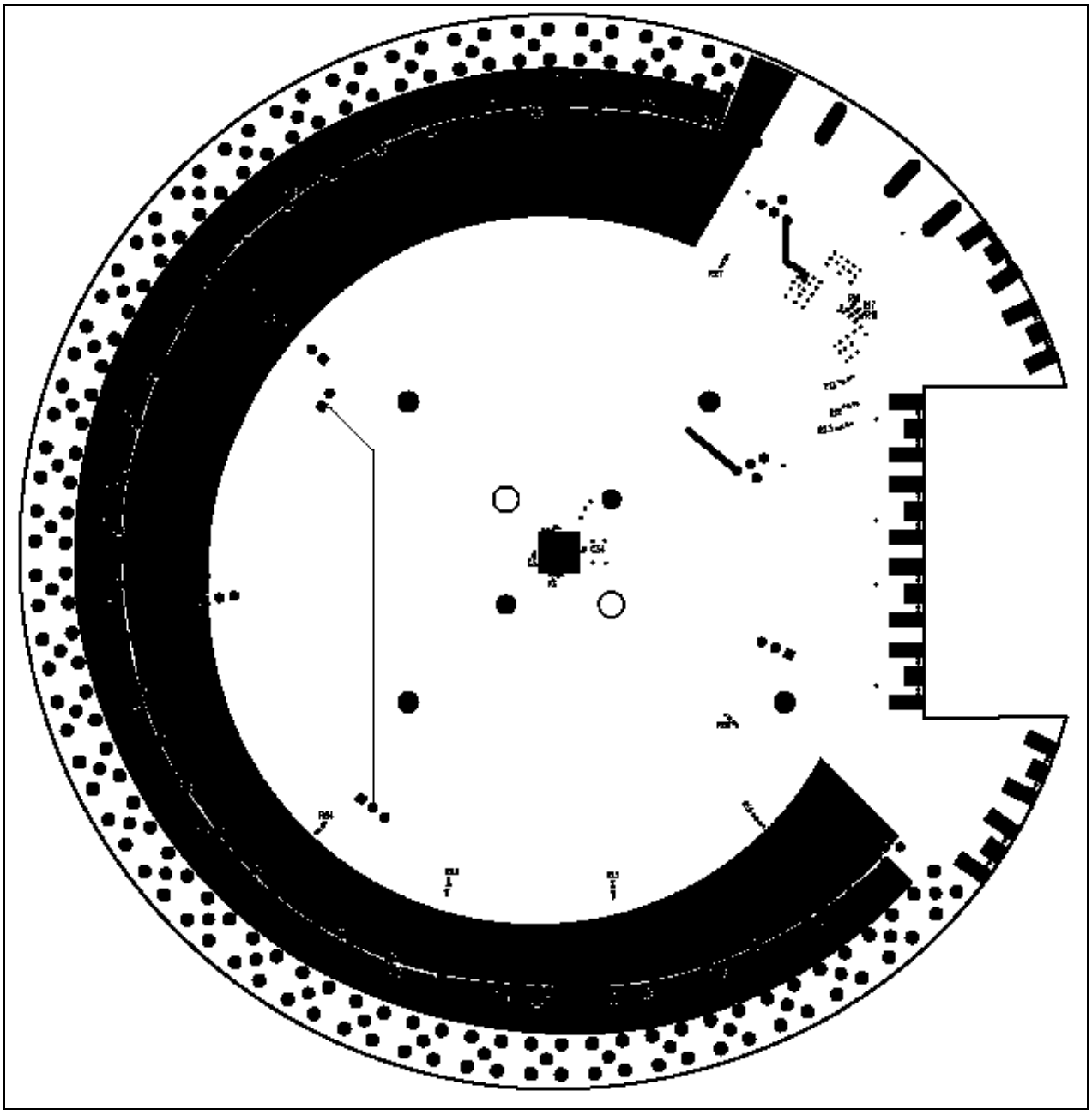

Figure 6. MAX3952 EV Kit PC Board Layout–Solder Side

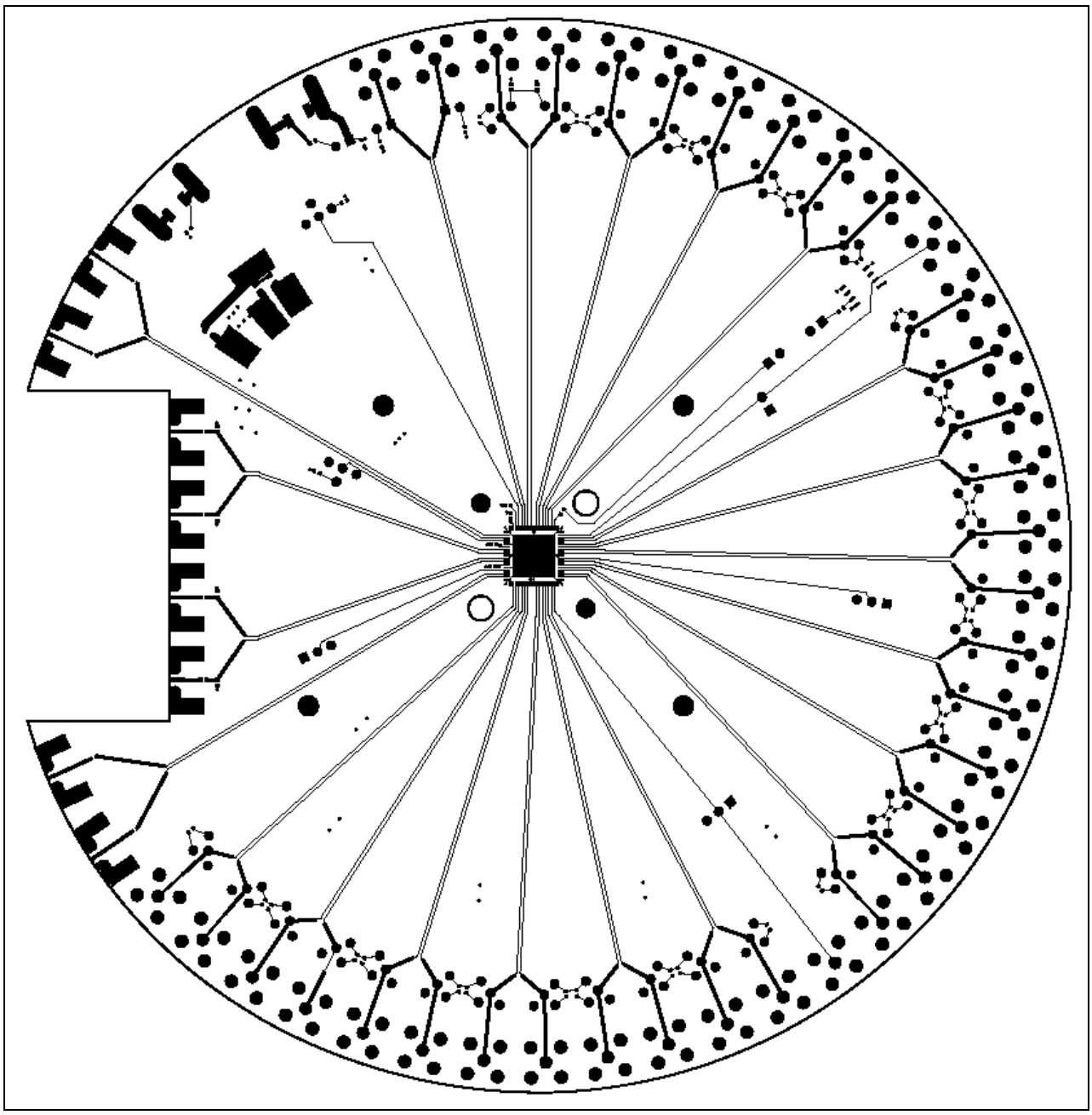

Figure 7. MAX3952 EV Kit PC Board Layout–Component Side

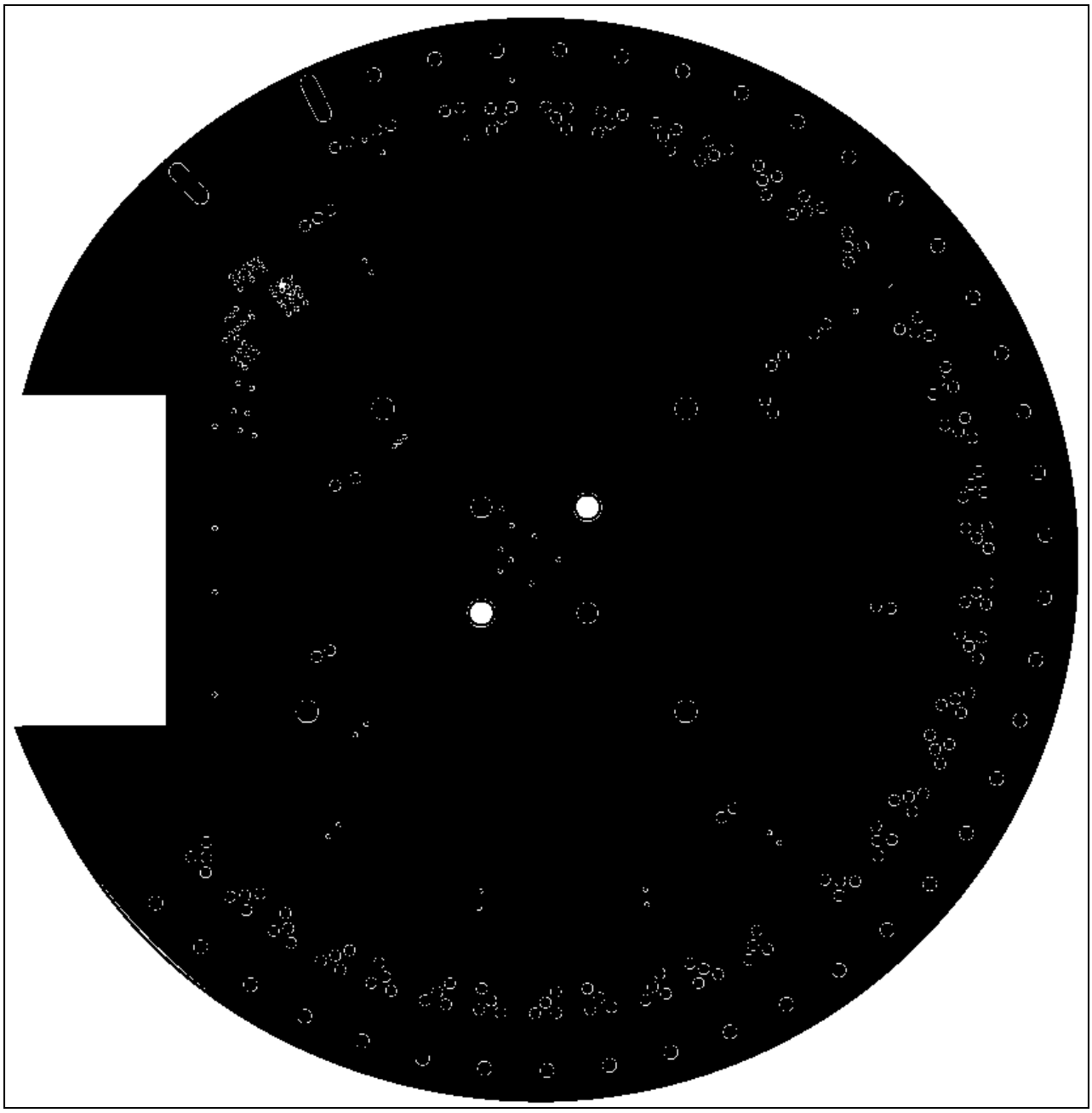

Figure 8. MAX3952 EV Kit PC Board Layout–Ground Plane

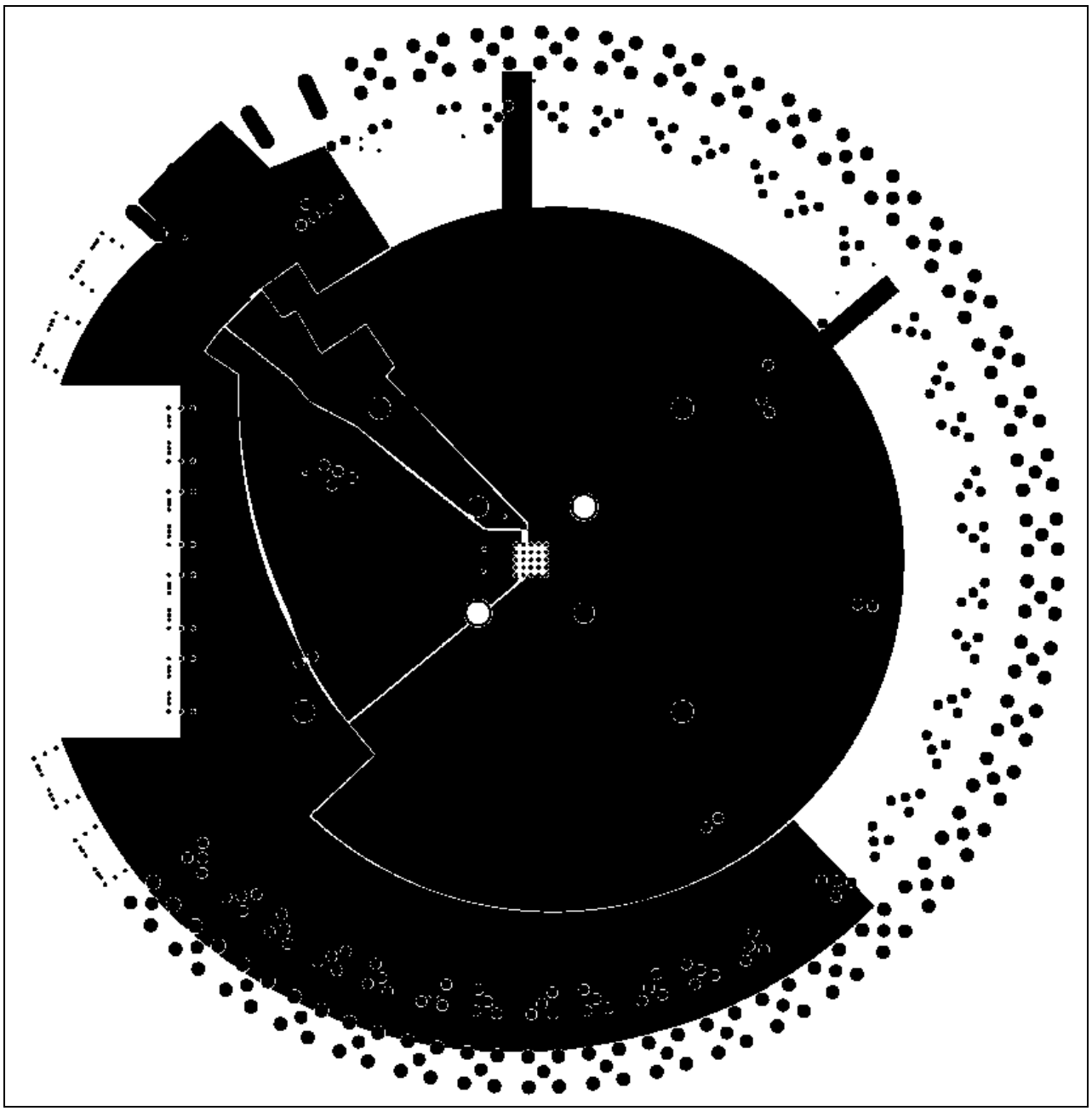

Figure 9. MAX3952 EV Kit PC Board Layout–Power Plane