Ordering number: EN3956C

CMOS LSI

SANYO No. 3956C

LC5872, LC5873, LC5874, LC5876

4-bit Single-chip Microcontrollers

with LCD driver, 12KB/8KB/6KB/4KB ROM, 1Bk RAM on chip

Overview

The LC5872, LC5873, LC5874 and LC5876 are 4-bit single-chip microcontrollers designed for low-voltage operation. They incorporate dual oscillators, a direct LCD interface and a carrier generator, making them ideal for use in VCRs, tuner remote-controllers, cameras, CD players and tuners, as well as compact measuring instrument and medical equipment applications.

Seven, 4-bit I/O ports are available in a variety of configurations which can be specified as mask options. These include on-chip pull-up or pull-down and hold transistors, open-drain or complementary outputs, key debounce circuitry, rising- or falling-edge detector inputs, interrupt generator and serial I/O circuitry. Other mask options include rising- or falling-edge interrupt inputs, a LOW- or HIGH-level reset input, four frequency divider ratios and a number of oscillator combinations for crystal and ceramic filter resonators and RC circuits, or an external clock input.

The direct LCD interface, which can be used as a general-purpose 35-line output port, can deliver 1/1 to 1/3 bias at 1/1 to 1/4 duty, providing support for a variety of displays. Three different LCD control frequencies are available.

The LC587x series devices also incorporate on-chip ROM and RAM, a software-programmable serial I/O timer counter, two general-purpose timers, a program-runaway watchdog timer, a clock timer, a speed control circuit, a frequency divider and a system clock generator. An alarm circuit is also provided.

The LC587x series microcontrollers operate from a 2.0 to 6.0 V supply and are available in 80-pin QIPs and as 82-pad dice.

Features

- Two on-chip oscillators support a 32, 38 or 65 kHz crystal resonator, a 400 kHz to 4 MHz ceramic filter resonator, a 200 kHz to 1 MHz RC circuit or an external clock input
- Programming-free four-common, 35-segment direct LCD interface port
- 1/1 to 1/4 duty for 35- to 140-segment LCDs
- CMOS, p-channel or n-channel segment output mask options
- 35-line segment outputs available as a general-purpose output port
- 15-stage frequency divider for LCD drive waveform generation
- 20 universal inputs/outputs
  - Five universal inputs
  - Four universal outputs have direct LED drive capacity, internal alarm and carrier outputs
  - Key debounce circuitry
  - Pull-up/pull-down resistor and transistor mask options
  - Software-selectable pull-up/pull-down transistors
  - Complementary or open-drain outputs
- 3-pin, 8-bit serial interface
- One dedicated and eight selectable rising- or falling-edge interrupt inputs
- LOW- or HIGH-level reset input
- Serial I/O timer, 8-bit programmable timer, 8-bit programmable-reloadable timer and watchdog timer
- 2048 × 16-bit, 3072 × 16-bit, 4096 × 16-bit and 6144 × 16-bit on-chip ROM for LC5872, LC5873, LC5874 and LC5876, respectively
- 256 × 4-bit on-chip RAM
- HALT and HOLD standby functions
- Eight HALT-mode and seven HOLD-mode release functions
- Five interrupt levels
- Eight subroutine nesting levels
- 2 to 10 µs cycle time in high-speed mode
- 20 µA to 1.7 mA supply current
- 2.0 to 6.0 V supply range
- 80-pin QIP or 82-pad die

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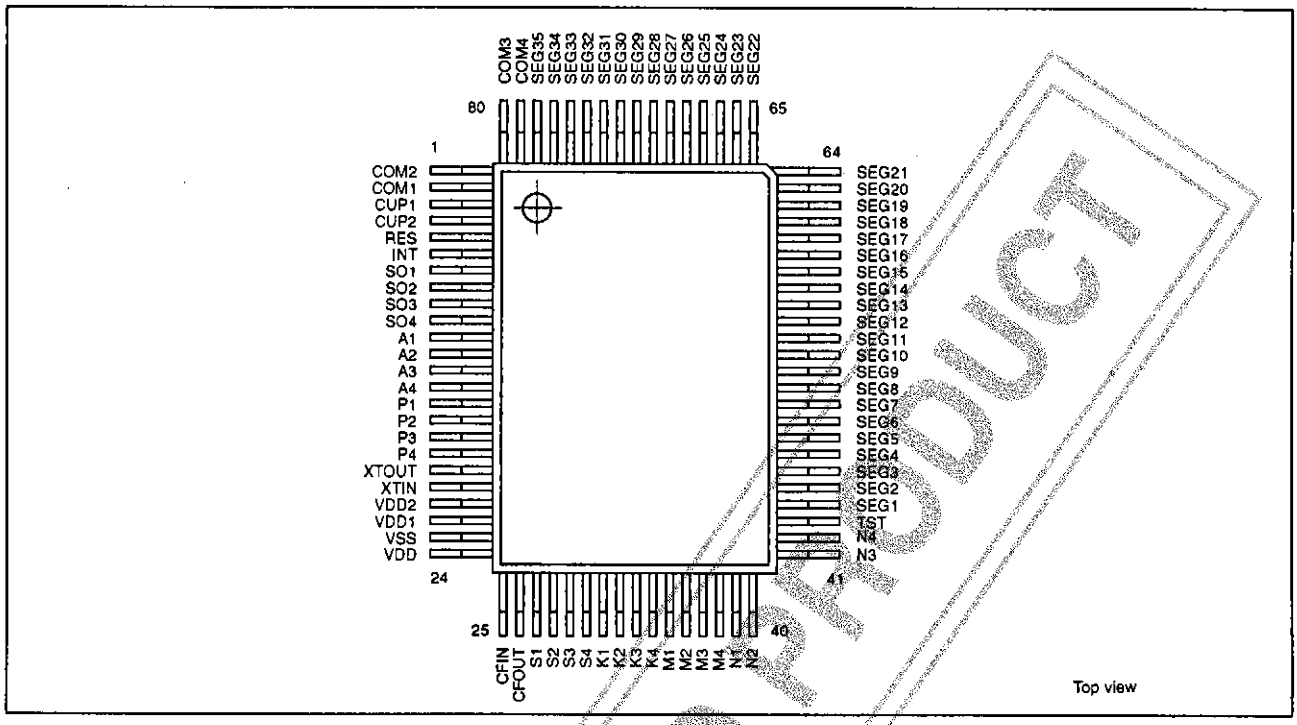
Pin Assignment



Note

Do not use dip-solder soldering when mounting the 80-pin QIP.

Die Specifications

Chip size	5.12 mm × 4.54 mm
Pad size	120 μm × 120 μm
Chip thickness	480 μm

Pad Coordinates

Pad number	Name	Coordinate (μm)		Pad number	Name	Coordinate (μm)	
		X	Y			X	Y
1	VDD	2236	−1946	42	SEG20	−2181	2068
2	CFIN	2236	−1637	43	SEG21	−2362	2068
3	CFOUT	2236	−1455	44	SEG22	−2362	1416
4	S1	2236	−1213	45	SEG23	−2362	1235
5	S2	2236	−1030	46	SEG24	−2362	1055
6	S3	2236	−797	47	SEG25	−2362	874
7	S4	2236	−615	48	SEG26	−2362	694
8	K1	2236	−390	49	SEG27	−2362	513
9	K2	2236	−207	50	SEG28	−2362	333
10	K3	2236	−24	51	SEG29	−2362	152
11	K4	2236	159	52	SEG30	−2362	−28
12	M1	2236	342	53	SEG31	−2362	−209
13	M2	2236	525	54	SEG32	−2362	−389
14	M3	2236	708	55	SEG33	−2362	−570
15	M4	2236	892	56	SEG34	−2362	−750
16	N1	2236	1247	57	SEG35	−2362	−931
17	N2	2236	1518	58	COM4	−2362	−1250

Pad number	Name	Coordinate (μm)		Pad number	Name	Coordinate (μm)	
		X	Y			X	Y
18	N3	2236	1790	59	COM3	−2362	−1432
19	N4	2236	2068	60	COM2	−2362	−1946
20	TST	1959	2068	61	COM1	−1912	−1946
21	SEG1	1733	2068	62	CUP1	−1730	−1946
22	SEG2	1507	2068	63	CUP2	−1548	−1946
23	SEG3	1280	2068	64	RES	−1362	−1946
24	SEG4	1055	2068	65	INT	−1145	−1946
25	SEG5	875	2068	66	SO1	−963	−1946
26	SEG6	695	2068	67	SO2	−780	−1946
27	SEG7	516	2068	68	SO3	−597	−1946
28	SEG8	336	2068	69	SO4	−414	−1946
29	SEG9	156	2068	70	A1	−231	−1946
30	SEG10	−24	2068	71	A2	−48	−1946
31	SEG11	−204	2068	72	A3	135	−1946
32	SEG12	−384	2068	73	A4	318	−1946
33	SEG13	−564	2068	74	P1	505	−1946
34	SEG14	−743	2068	75	P2	688	−1946
35	SEG15	−923	2068	76	P3	871	−1946
36	SEG16	−1103	2068	77	P4	1054	−1946
37	SEG17	−1282	2068	78	XTOUT	1280	−1946
38	SEG18	−1463	2068	79	XTIN	1463	−1946
39	SEG19	−1643	2068	80	VDD2	1686	−1946
40	TEST	−1820	2068	81	VDD1	1869	−1946
41	TEST	−2001	2068	82	VSS	2051	−1946

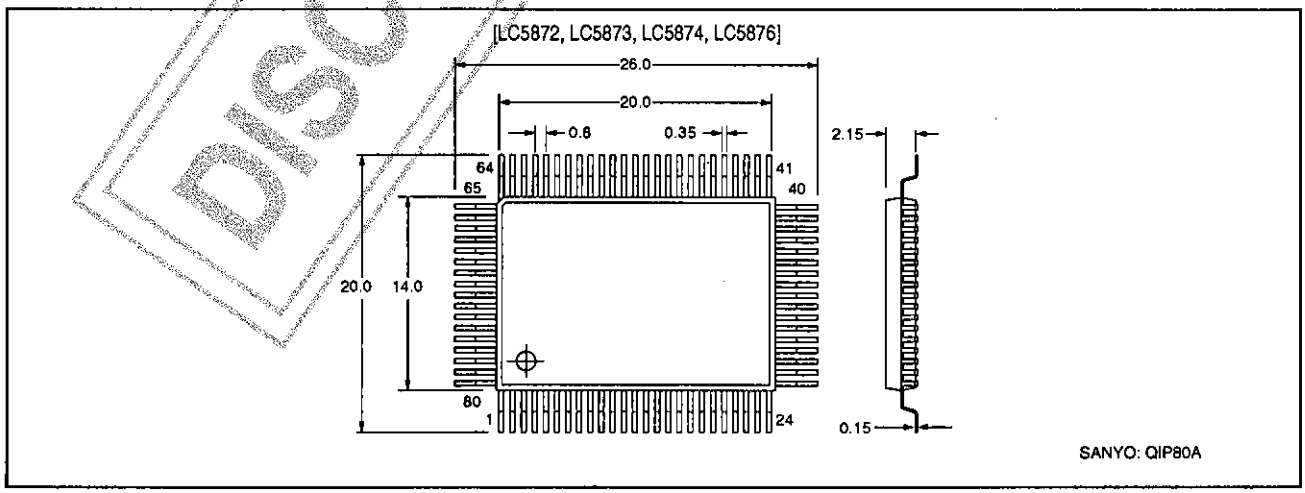
Note

Tie the test pin, pad 20, to V_{SS} for normal operation. Pads 40 and 41 should be left open. Tie the substrate to V_{SS} or leave it open.

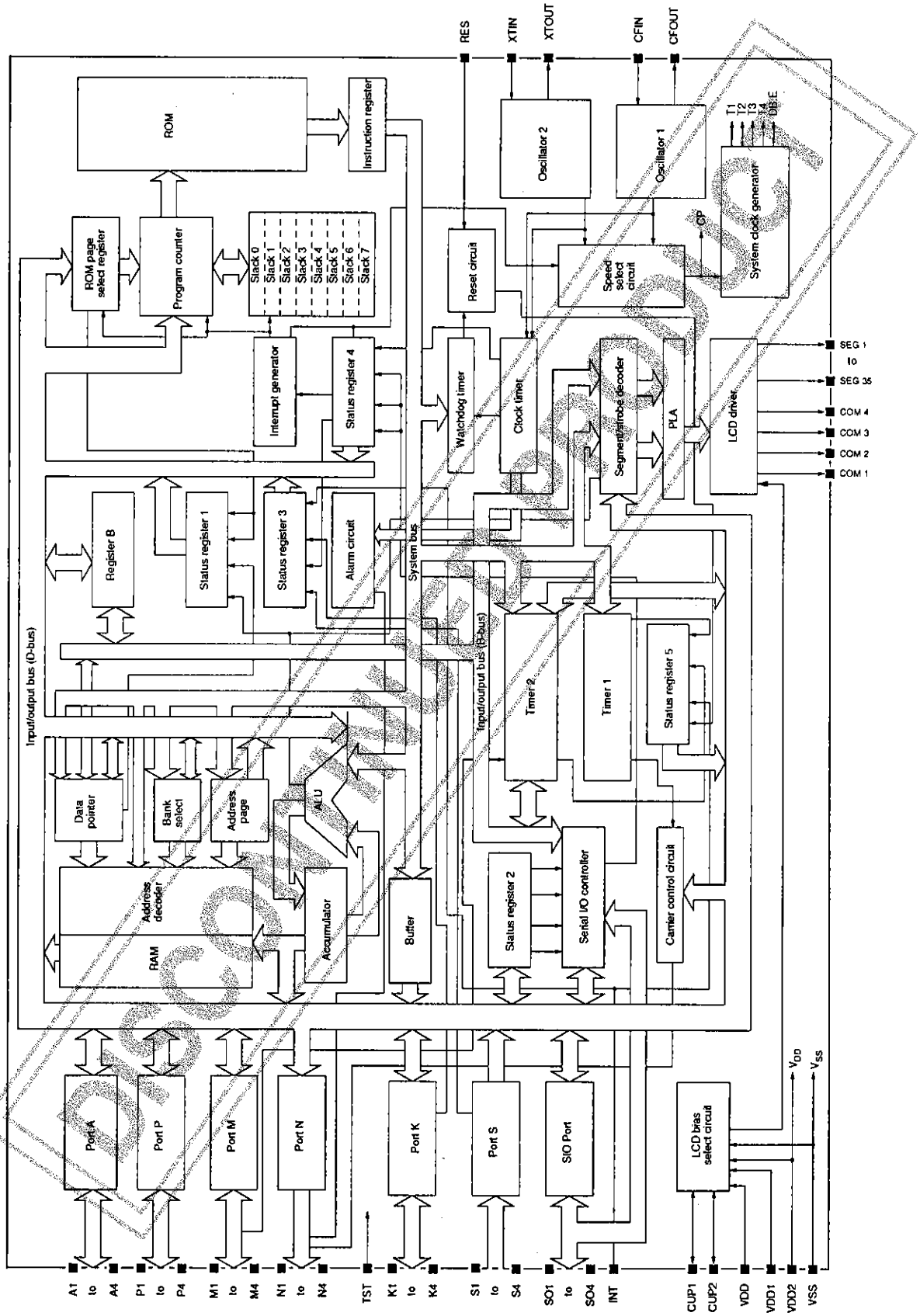
Package Dimensions

Unit: mm

3044B-QIP80A



Block Diagram



Pin Functions

Number	Name	Function
1	COM2	LCD common outputs 1 to 4
2	COM1	
79	COM4	
80	COM3	
3	CUP1	LCD drive bias select input 1
4	CUP2	LCD drive bias select input 2
5	RES	Reset input
6	INT	Interrupt input
7 to 10	SO1 to SO4	4-bit bidirectional serial input/output port
11 to 14	A1 to A4	4-bit bidirectional port A
15 to 18	P1 to P4	4-bit bidirectional port P
19	XTOUT	Crystal oscillator output
20	XTIN	Crystal oscillator input
21	VDD2	LCD drive supply input 2. See Figure 1.
22	VDD1	LCD drive supply input 1. See Figure 1.
23	VSS	Ground. See Figure 1.
24	VDD	5 V supply. See Figure 1.
25	CFIN	Ceramic filter oscillator input
26	CFOUT	Ceramic filter oscillator output
27 to 30	S1 to S4	4-bit input port S with key debounce circuit
31 to 34	K1 to K4	4-bit bidirectional port K with key debounce circuit
35 to 38	M1 to M4	4-bit bidirectional port M. Also, M4 is an external clock input for timer 2 in mode 3.
39 to 42	N1 to N4	4-bit output port N with carrier output at N3 and alarm circuit output at N4
43	TST	Test mode select input
44 to 78	SEG1 to SEG35	LCD segment outputs 1 to 35 which can be used as a general-purpose output port

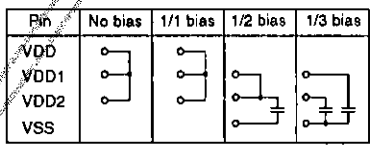


Figure 1. Supply connections

Specifications

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Ratings	Unit
Supply voltage range	V_{DD}	−0.3 to +7.0	V
LCD supply voltage 1 range	V_{DD1}	−0.3 to V_{DD}	V
LCD supply voltage 2 range	V_{DD2}	−0.3 to V_{DD}	V
Ports S, K, P, SO and A, and RES, INT and TST input voltage range	V_I	−0.3 to V_{DD} + 0.3	V
Ports K, P, SO, A and N, and CUP1, CUP2, SEG1 to SEG 35 and COM1 to COM4 output voltage range	V_O	−0.3 to V_{DD} + 0.3	V
Port N output current range	I_{O1}	−10 to +15	mA
Ports K, P, M, SO and A output current range	I_{O2}	−5 to +5	mA
Ports K, P, M, SO, A and N, and SEG1 to SEG 35 total output current range	ΣI_O	−70 to +70	mA
Power dissipation	P_D	500	mW
Operating temperature range	T_{opr}	−30 to +70	°C
Storage temperature range	T_{stg}	−55 to +125	°C

Allowable Operating Ranges

V_{SS} = 0 V, T_a = 25 °C

Parameter	Symbol	Ratings	Unit
Supply voltage range with LCD disabled. See Note 1.	V_{DD}	2.0 to 6.0	V
Supply voltage range with 1/1 bias. See Note 1.	V_{DD}	2.0 to 6.0	V
Supply voltage range with 1/2 bias. See Note 2.	V_{DD}	2.8 to 6.0	V
Supply voltage range with 1/3 bias. See Note 3.	V_{DD}	2.8 to 6.0	V
Minimum data retention voltage	V_{DR}	2.0	V

Notes

1. $V_{DD1} = V_{DD2} = V_{DD}$
2. $V_{DD1} = V_{DD2} = 1/2 \times V_{DD}$
3. $V_{DD1} = 2/3 \times V_{DD}$ and $V_{DD2} = 1/3 \times V_{DD}$

Electrical Characteristics

V_{DD} = 2.5 to 3.2 V

V_{SS} = 0 V, T_a = −30 to +70 °C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Port N LOW-level output voltage	V_{OL1}	I_{OL} = 1.0 mA	–	–	0.5	V
Port N HIGH-level output voltage	V_{OH1}	I_{OH} = −500 µA	V_{DD} − 0.5	–	–	V
Ports K, P, M, SO and A LOW-level output voltage	V_{OL2}	I_{OL} = 400 µA	–	–	0.5	V
Ports K, P, M, SO and A HIGH-level output voltage	V_{OH2}	I_{OH} = −400 µA	V_{DD} − 0.5	–	–	V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Port N output leakage current	I_{leak1}	V_{OH} = 10.5 V	–	–	1.0	µA
SEG1 to SEG35 CMOS LOW-level output voltage	V_{OL3}	I_{OL} = 100 µA. See Note.	–	–	0.5	V
SEG1 to SEG35 CMOS HIGH-level output voltage	V_{OH3}	I_{OH} = –100 µA. See Note.	V_{DD} – 0.5	–	–	V
SEG1 to SEG35 p-channel HIGH-level output voltage	V_{OH3}	I_{OH} = –100 µA. See Note.	V_{DD} – 0.5	–	–	V
SEG1 to SEG35 p-channel output leakage current	I_{leak2}	V_{OL} = V_{SS}. See Note.	–	–	1.0	µA
SEG1 to SEG35 n-channel LOW-level output voltage	V_{OL3}	I_{OL} = 100 µA. See Note.	–	–	0.5	V
SEG1 to SEG35 n-channel output leakage current	I_{leak3}	V_{OH} = V_{DD}. See Note.	–	–	1.0	µA
SEG1 to SEG35, 1/1 duty LOW-level output voltage	V_{OL4}	I_{OL} = 20 µA	–	–	0.2	V
SEG1 to SEG35, 1/1 duty HIGH-level output voltage	V_{OH4}	I_{OH} = –20 µA	V_{DD} – 0.2	–	–	V
COM1 to COM4, 1/1 bias LOW-level output voltage	V_{OL5}	I_{OL} = 100 µA	–	–	0.2	V
COM1 to COM4, 1/1 bias HIGH-level output voltage	V_{OH5}	I_{OH} = –100 µA	V_{DD} – 0.2	–	–	V
Ports S, K, P, M, SO and A LOW-level hold transistor input resistance	R_{IL1}	V_I = 0.2V_{DD}	60	300	1200	kΩ
Ports S, K, P, M, SO and A HIGH-level hold transistor input resistance	R_{IH1}	V_I = 0.8V_{DD}	60	300	1200	kΩ
Ports S, K, P, M, SO and A pull-up transistor input resistance	R_{PU1}	V_I = V_{SS}	30	150	500	kΩ
Ports S, K, P, M, SO and A pull-down transistor input resistance	R_{PD1}	V_I = V_{DD}	30	150	500	kΩ
INT LOW-level hold transistor input resistance	R_{IL2}	V_I = 0.2V_{DD}	60	300	1200	kΩ
INT HIGH-level hold transistor input resistance	R_{IH2}	V_I = 0.8V_{DD}	60	300	1200	kΩ
INT pull-up transistor resistance	R_{PU2}	V_I = V_{SS}	300	1500	5000	kΩ
INT pull-down transistor resistance	R_{PD2}	V_I = V_{DD}	300	1500	5000	kΩ
RES pull-up transistor resistance	R_{PU3}	V_I = V_{SS}	10	30	50	kΩ
RES pull-down transistor resistance	R_{PD3}	V_I = V_{DD}	10	30	50	kΩ
TST pull-down transistor resistance	R_{PD4}	V_I = V_{DD}	80	250	1000	kΩ

Note

Complementary (CMOS), p-channel or n-channel segment output mask options. See Figures 27 and 28.

V_{DD} = 3.0 to 4.5 V

V_{SS} = 0 V, T_a = −30 to 70 °C

Parameter	Symbol	Conditions		Ratings min	Ratings typ	Ratings max	Unit
LCD supply voltage 1	V_{DD1}	V_{DD} = 3.0 V, C1 = C2 = 0.1 µF, 1/2 bias, f_{opg} = 32.768 kHz		1.3	1.5	1.7	V
Supply current	I_{DD}	V_{DD} = 3.0 V, 32 kHz crystal resonator, C_g = 20 pF, Z_c = 25 kΩ, HALT mode, 1/3 bias. See Figure 5.	T_a = 25 °C	–	4.0	8.0	µA
			T_a = 50 °C	–	–	20	
		V_{DD} = 3.0 V, 38 or 65 kHz crystal resonator, C_g = 10 pF, Z_c = 25 kΩ, HALT mode, 1/3 bias. See Figure 5.	T_a = 25 °C	–	6.0	10	
			T_a = 50 °C	–	–	30	
		V_{DD} = 3.0 V, 400 kHz ceramic resonator, C_{cg} = C_{cd} = 330 pF, HALT mode. See Figure 6.	T_a = 25 °C	–	150	300	
			T_a = 50 °C	–	–	500	
Supply leakage current	I_{DD}	V_{DD} = 3.0 V. See Figure 2.	T_a = 25 °C	–	0.2	1.0	µA
			T_a = 50 °C	–	1.0	5.0	
Ports S, K, M, SO and A, and INT and RES input leakage current	I_{leak}	V_{DD} = 3.0 V	V_I = V_{SS}	−1.0	–	–	µA
			V_I = V_{DD}	–	–	1.0	
Port N LOW-level output voltage	V_{OL1}	I_{OL} = 2.0 mA		–	–	0.5	V
Port N HIGH-level output voltage	V_{OH1}	I_{OH} = −1.0 mA		V_{DD} − 0.5	–	–	V
Ports K, P, M, SO and A LOW-level output voltage	V_{OL2}	I_{OL} = 500 µA		–	–	0.5	V
Ports K, P, M, SO and A HIGH-level output voltage	V_{OH2}	I_{OH} = −500 µA		V_{DD} − 0.5	–	–	V
Port N output leakage current	I_{leak1}	V_{OH} = 10.5 V		–	–	1.0	µA
SEG1 to SEG35 CMOS LOW-level output voltage	V_{OL3}	I_{OL} = 300 µA. See Note.		–	–	0.5	V
SEG1 to SEG35 CMOS HIGH-level output voltage	V_{OH3}	I_{OH} = −300 µA. See Note.		V_{DD} − 0.5	–	–	V
SEG1 to SEG35 p-channel HIGH-level output voltage	V_{OH3}	I_{OH} = −300 µA. See Note.		V_{DD} − 0.5	–	–	V
SEG1 to SEG35 p-channel output leakage current	I_{leak2}	V_{OL} = V_{SS}. See Note.		–	–	1.0	µA
SEG1 to SEG35 n-channel LOW-level output voltage	V_{OL3}	I_{OL} = 300 µA. See Note.		–	–	0.5	V
SEG1 to SEG35 n-channel output leakage current	I_{leak3}	V_{OH} = V_{DD}. See Note.		–	–	1.0	µA
SEG1 to SEG35, 1/1 duty LOW-level output voltage	V_{OL4}	I_{OL} = 20 µA		–	–	0.2	V
SEG1 to SEG35, 1/1 duty HIGH-level output voltage	V_{OH4}	I_{OH} = −20 µA		V_{DD} − 0.2	–	–	V
COM1 to COM4, 1/1 bias LOW-level output voltage	V_{OL5}	I_{OL} = 100 µA		–	–	0.2	V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
COM1 to COM4, 1/1 bias HIGH-level output voltage	V_{OH5}	I_{OH} = −100 µA	V_{DD} − 0.2	−	−	V
SEG1 to SEG35, 1/2 bias LOW-level output voltage	V_{OL4}	I_{OL} = 20 µA	−	−	0.2	V
SEG1 to SEG35, 1/2 bias HIGH-level output voltage	V_{OH4}	I_{OH} = −20 µA	V_{DD} − 0.2	−	−	V
COM1 to COM4, 1/2 bias LOW-level output voltage	V_{OL5}	I_{OL} = 100 µA	−	−	0.2	V
COM1 to COM4, 1/2 bias MID-level output voltage	V_{OM}	I_{OL} = 100 µA, I_{OH} = −100 µA	$(V_{DD} + 2)$ − 0.2	−	$(V_{DD} + 2)$ + 0.2	V
COM1 to COM4, 1/2 bias HIGH-level output voltage	V_{OH5}	I_{OH} = −100 µA	V_{DD} − 0.2	−	−	V
Ports S, K, P, M, SO and A LOW-level hold transistor input resistance	R_{IL1}	V_I = 0.2 V_{DD}	35	200	800	kΩ
Ports S, K, P, M, SO and A HIGH-level hold transistor input resistance	R_{IH1}	V_I = 0.8V_{DD}	35	200	800	kΩ
Ports S, K, P, M, SO and A pull-up transistor input resistance	R_{PU1}	V_I = V_{SS}	15	80	300	kΩ
Ports S, K, P, M, SO and A pull-down transistor input resistance	R_{PD1}	V_I = V_{DD}	15	80	300	kΩ
INT LOW-level hold transistor input resistance	R_{IL2}	V_I = 0.2V_{DD}	35	200	800	kΩ
INT HIGH-level hold transistor input resistance	R_{IH2}	V_I = 0.8V_{DD}	35	200	800	kΩ
INT pull-up transistor resistance	R_{PU2}	V_I = V_{SS}	150	800	3000	kΩ
INT pull-down transistor resistance	R_{PD2}	V_I = V_{DD}	150	800	3000	kΩ
RES pull-up transistor resistance	R_{PU3}	V_I = V_{SS}	10	30	50	kΩ
RES pull-down transistor resistance	R_{PD3}	V_I = V_{DD}	10	30	50	kΩ
TST pull-down transistor resistance	R_{PD4}	V_I = V_{DD}	25	130	500	kΩ

Note
Complementary (CMOS), p-channel or n-channel segment output mask options. See Figures 27 and 28.

V_{DD} = 4.5 to 6.0 V

V_{SS} = 0 V, T_a = −30 to 70 °C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
LCD supply voltage 1	V_{DD1}	V_{DD} = 5.0 V, C1 = C2 = 0.1 µF, 1/2 bias, f_{opg} = 32.768 kHz. See Figure 3.	2.40	2.50	2.60	V
		V_{DD} = 5.0 V, C1 = C2 = 0.1 µF, 1/3 bias, f_{opg} = 32.768 kHz. See Figure 3.	3.10	3.33	3.50	
LCD supply voltage 2	V_{DD2}	V_{DD} = 5.0 V, C1 = C2 = 0.1 µF, 1/3 bias, f_{opg} = 32.768 kHz. See Figure 3.	1.40	1.67	1.80	V

Parameter	Symbol	Conditions		Ratings min	Ratings typ	Ratings max	Unit
Supply current	I_{DD}	V_{DD} = 5.0 V, 32 kHz crystal resonator, C_g = 20 pF, Z_c = 25 kΩ, HALT mode, 1/3 bias. See Figure 5.	T_a = 25 °C	–	15	30	μA
			T_a = 50 °C	–	–	50	
		V_{DD} = 5.0 V, 38 or 65 kHz crystal resonator, C_g = 10 pF, Z_c = 25 kΩ, HALT mode, 1/3 bias. See Figure 5.	T_a = 25 °C	–	15	30	
			T_a = 50 °C	–	–	50	
		V_{DD} = 5.0 V, 400 kHz ceramic resonator, C_g = C_{cd} = 330 pF, HALT mode. See Figure 6.	T_a = 25 °C	–	400	600	
			T_a = 50 °C	–	–	600	
		V_{DD} = 5.0 V, 1 MHz ceramic resonator, C_g = C_{cd} = 100 pF, HALT mode. See Figure 6.	T_a = 25 °C	–	450	650	
			T_a = 50 °C	–	–	700	
		V_{DD} = 5.0 V, 2 MHz ceramic resonator, C_g = C_{cd} = 33 pF, HALT mode. See Figure 6.	T_a = 25 °C	–	500	700	
			T_a = 50 °C	–	–	750	
		V_{DD} = 5.0 V, 4 MHz ceramic resonator, C_g = C_{cd} = 33 pF, HALT mode. See Figure 6.	T_a = 25 °C	–	700	900	
			T_a = 50 °C	–	–	1000	
		T_a = 25 °C, 32 kHz crystal resonator, 1/3 bias. See Figure 5.	V_{DD} = 3 V	–	20	30	
			V_{DD} = 5 V	–	40	60	
		T_a = 25 °C, 400 kHz ceramic resonator. See Figure 5.	V_{DD} = 3 V	–	240	300	
			V_{DD} = 5 V	–	620	780	
		T_a = 25 °C, 1 MHz ceramic resonator. See Figure 5.	V_{DD} = 3 V	–	350	480	
			V_{DD} = 5 V	–	850	1200	
		T_a = 25 °C, 4 MHz ceramic resonator. See Figure 5.	V_{DD} = 5 V	–	1700	2500	
Supply leakage current	I_{DD}	V_{DD} = 6.0 V. See Figure 2.	T_a = 25 °C	–	0.2	1.0	μA
			T_a = 50 °C	–	1.0	5.0	
Ports S, K, M, SO and A, and INT and RES input leakage current	I_{leak}	V_{DD} = 6.0 V.	V_I = V_{SS}	–1.0	–	–	μA
			V_I = V_{DD}	–	–	1.0	
Port N LOW-level output voltage	V_{OL1}	I_{OL} = 10.0 mA		–	–	0.5	V
Port N HIGH-level output voltage	V_{OH1}	I_{OH} = –5.0 mA		V_{DD} – 0.5	–	–	V
Ports K, P, M, SO and A LOW-level output voltage	V_{OL2}	I_{OL} = 2.0 mA		–	0.2	0.5	V
Ports K, P, M, SO and A HIGH-level output voltage	V_{OH2}	I_{OH} = –1.0 mA		V_{DD} – 0.5	V_{DD} – 0.2	–	V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Port N output leakage current	I_{leak1}	V_{OH} = 10.5 V	–	–	1.0	μA
SEG1 to SEG35 CMOS LOW-level output voltage	V_{OL3}	I_{OL} = 500 μA. See Note.	–	–	0.5	V
SEG1 to SEG35 CMOS HIGH-level output voltage	V_{OH3}	I_{OH} = –500 μA. See Note.	V_{DD} – 0.5	V_{DD} – 0.2	–	V
SEG1 to SEG35 p-channel HIGH-level output voltage	V_{OH3}	I_{OH} = –500 μA. See Note.	V_{DD} – 0.5	V_{DD} – 0.2	–	V
SEG1 to SEG35 p-channel output leakage current	I_{leak2}	V_{OL} = V_{SS}. See Note.	–	–	1.0	μA
SEG1 to SEG35 n-channel LOW-level output voltage	V_{OL3}	I_{OL} = 500 μA. See Note.	–	0.2	0.5	V
SEG1 to SEG35 n-channel output leakage current	I_{leak2}	V_{OH} = V_{DD}. See Note.	–	–	1.0	μA
SEG1 to SEG35, 1/1 duty LOW-level output voltage	V_{OL4}	I_{OL} = 40 μA	–	–	0.2	V
SEG1 to SEG35, 1/1 duty HIGH-level output voltage	V_{OH4}	I_{OH} = –40 μA	V_{DD} – 0.2	–	–	V
COM1 to COM4, 1/1 bias LOW-level output voltage	V_{OL5}	I_{OL} = 400 μA	–	–	0.2	V
COM1 to COM4, 1/1 bias HIGH-level output voltage	V_{OH5}	I_{OH} = –400 μA	V_{DD} – 0.2	–	–	V
SEG1 to SEG35, 1/2 bias LOW-level output voltage	V_{OL4}	I_{OL} = 40 μA	–	–	0.2	V
SEG1 to SEG35, 1/2 bias HIGH-level output voltage	V_{OH4}	I_{OH} = –40 μA	V_{DD} – 0.2	–	–	V
COM1 to COM4, 1/2 bias LOW-level output voltage	V_{OL5}	I_{OL} = 400 μA	–	–	0.2	V
COM1 to COM4, 1/2 bias MID-level output voltage	V_{OM}	I_{OL} = 400 μA, I_{OH} = –400 μA	(V_{DD} ÷ 2) – 0.2	–	(V_{DD} ÷ 2) + 0.2	V
COM1 to COM4, 1/2 bias HIGH-level output voltage	V_{OH5}	I_{OH} = –400 μA	V_{DD} – 0.2	–	–	V
SEG1 to SEG35, 1/3 bias LOW-level output voltage	V_{OL6}	I_{OL} = 40 μA	–	–	0.2	V
SEG1 to SEG35, 1/3 bias MID-level output voltage	V_{OM1-1}	I_{OL} = 40 μA, I_{OH} = –40 μA	2 × (V_{DD} ÷ 3) – 0.2	–	2 × (V_{DD} ÷ 3) + 0.2	V
SEG1 to SEG35, 1/3 bias MID-level output voltage	V_{OM1-2}	I_{OH} = –40 μA, I_{OL} = 40 μA	(V_{DD} ÷ 3) – 0.2	–	(V_{DD} ÷ 3) + 0.2	V
SEG1 to SEG35, 1/3 bias HIGH-level output voltage	V_{OH4}	I_{OH} = –40 μA	V_{DD} – 0.2	–	–	V
COM1 to COM4, 1/3 bias LOW-level output voltage	V_{OL6}	I_{OL} = 400 μA	–	–	0.2	V
COM1 to COM4, 1/3 bias MID-level output voltage	V_{OM2-1}	I_{OH} = –400 μA, I_{OL} = 400 μA	(2V_{DD} ÷ 3) – 0.2	–	(2V_{DD} ÷ 3) + 0.2	V
COM1 to COM4, 1/3 bias MID-level output voltage	V_{OM2-2}	I_{OL} = 400 μA, I_{OH} = –400 μA	(V_{DD} ÷ 3) – 0.2	–	(V_{DD} ÷ 3) + 0.2	V
COM1 to COM4, 1/3 bias HIGH-level output voltage	V_{OH6}	I_{OH} = –400 μA	V_{DD} – 0.2	–	–	V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Ports S, K, P, M, SO and A LOW-level hold transistor input resistance	R_{IL1}	$V_I = 0.2V_{DD}$	30	120	500	kΩ
Ports S, K, P, M, SO and A HIGH-level hold transistor input resistance	R_{IH1}	$V_I = 0.8V_{DD}$	30	120	500	kΩ
Ports S, K, P, M, SO and A pull-up transistor input resistance	R_{PU1}	$V_I = V_{SS}$	10	50	200	kΩ
Ports S, K, P, M, SO and A pull-down transistor input resistance	R_{PD1}	$V_I = V_{DD}$	10	50	200	kΩ
INT LOW-level hold transistor input resistance	R_{IL2}	$V_I = 0.2V_{DD}$	30	120	500	kΩ
INT HIGH-level hold transistor input resistance	R_{IH2}	$V_I = 0.8V_{DD}$	30	120	500	kΩ
INT pull-up transistor resistance	R_{PU2}	$V_I = V_{SS}$	100	500	2000	kΩ
INT pull-down transistor resistance	R_{PD2}	$V_I = V_{DD}$	100	500	2000	kΩ
RES pull-up transistor resistance	R_{PU3}	$V_I = V_{SS}$	10	30	50	kΩ
RES pull-down transistor resistance	R_{PD3}	$V_I = V_{DD}$	10	30	50	kΩ
TST pull-down transistor resistance	R_{PD4}	$V_I = V_{DD}$	20	70	300	kΩ

Note
Complementary (CMOS), p-channel or n-channel segment output mask options. See Figures 27 and 28.

Input specifications

V_{SS} = 0 V, T_a = −30 to 70 °C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Ports S, K, P, M, SO and A, and INT LOW-level input voltage	V_{IL1}		0	–	$0.3V_{DD}$	V
Ports S, K, P, M, SO and A, and INT HIGH-level input voltage	V_{IH1}		$0.7V_{DD}$	–	V_{DD}	V
RES LOW-level input voltage	V_{IL2}		0	–	$0.25V_{DD}$	V
RES HIGH-level input voltage	V_{IH2}		$0.75V_{DD}$	–	V_{DD}	V
CFIN LOW-level input voltage	V_{IL3}		0	–	$0.25V_{DD}$	V
CFIN HIGH-level input voltage	V_{IH3}		$0.75V_{DD}$	–	V_{DD}	V

Clock specifications

V_{SS} = 0 V, T_a = −30 to 70 °C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Crystal oscillator operating frequency	f_{xtal}	V_{DD} = 2.0 to 6.0 V, 32 kHz range	32	–	33	kHz
		V_{DD} = 2.2 to 6.0 V, 38 kHz range	37	38	39	
		V_{DD} = 2.2 to 6.0 V, 65 kHz range	60	65	70	

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Ceramic filter oscillator operating frequency	f_{cer}	V_{DD} = 2.2 to 6.0 V	190	–	810	kHz
		V_{DD} = 2.5 to 6.0 V	190	–	1200	
		V_{DD} = 3.0 to 6.0 V	190	–	2300	
		V_{DD} = 4.5 to 6.0 V	190	–	4200	
		V_{DD} = 4.0 to 6.0 V, RC oscillator	100	–	1500	
		V_{DD} = 2.0 to 6.0 V, external oscillator	190	–	800	
Serial interface clock frequency	f_{ser}	V_{DD} = 3.0 to 6.0 V	0	–	200	kHz

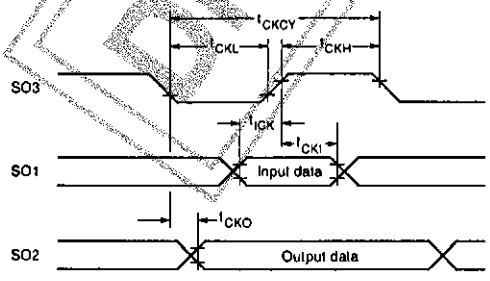
Oscillator specifications

T_a = 25 °C

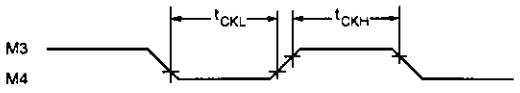
Parameter	Symbol	Conditions		Ratings			Unit
				min	typ	max	
Oscillator 1 start voltage	V_{st}	400 kHz ceramic filter resonator, C_{cg} = C_{cd} = 330 pF. See Figure 6.	t_{st} ≤ 30 ms	–	–	2.4	V
Oscillator 1 sustain voltage	V_{sus}			2.2	–	6.0	V
Oscillator 1 start time	t_{st}		V_{DD} = 2.4 V	–	–	30	ms
Oscillator 1 start voltage	V_{st}	800 kHz ceramic filter resonator, C_{cg} = C_{cd} = 330 pF. See Figure 6.	t_{st} ≤ 30 ms	–	–	2.4	V
Oscillator 1 sustain voltage	V_{sus}			2.2	–	6.0	V
Oscillator 1 start time	t_{st}		V_{DD} = 2.4 V	–	–	30	ms
Oscillator 2 start voltage	V_{st}	32 kHz crystal resonator, C_g = 10 pF, Z_c = 25 kΩ. See Figure 5.	t_{st} ≤ 5 s	–	–	2.2	V
Oscillator 2 sustain voltage	V_{sus}			2.0	–	6.0	V
Oscillator 2 start time	t_{st}		V_{DD} = 2.2 V	–	–	5	s
Oscillator stability	Δf		V_{DD} = 2.95 to 3.05 V	–	–	3	ppm
Oscillator 2 start voltage	V_{st}	38 or 65 kHz crystal resonator, C_g = 10 pF, Z_c = 25 kΩ. See Figure 5.	t_{st} ≤ 5 s	–	–	2.4	V
Oscillator 2 sustain voltage	V_{sus}			2.2	–	6.0	V
Oscillator 2 start time	t_{st}		V_{DD} = 2.4 V	–	–	5	s
XTOUT oscillator compensation capacitor	C_d	V_{DD} = 3.0 V		16	20	24	pF

Timing Diagrams

Serial I/O timing



Timer 2 external clock input timing

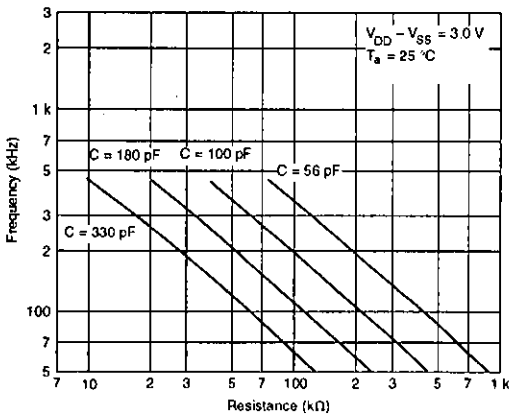


Note

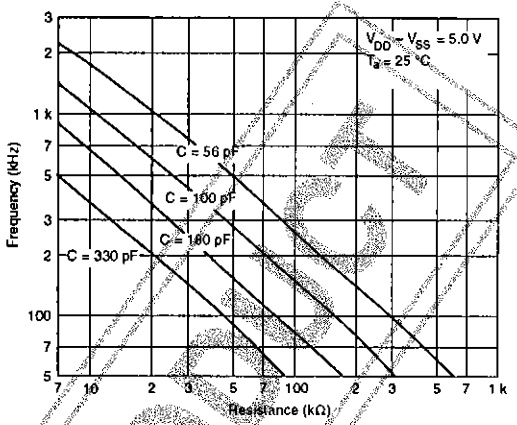
t_{CKCY} > 5 µs, t_{CKL} = t_{CKH} > 2.4 µs, t_{ICK} > 1 µs, t_{CKI} > 1 µs, t_{CKO} < 1 µs (max) and V_{DD} = 3.0 to 6.0 V

Typical Performance Characteristics

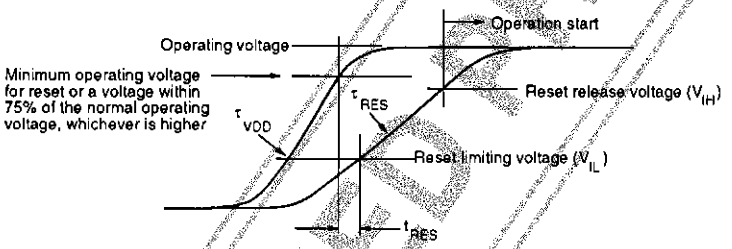
RC oscillator characteristics (3.0 V supply)



RC oscillator characteristics (5.0 V supply)



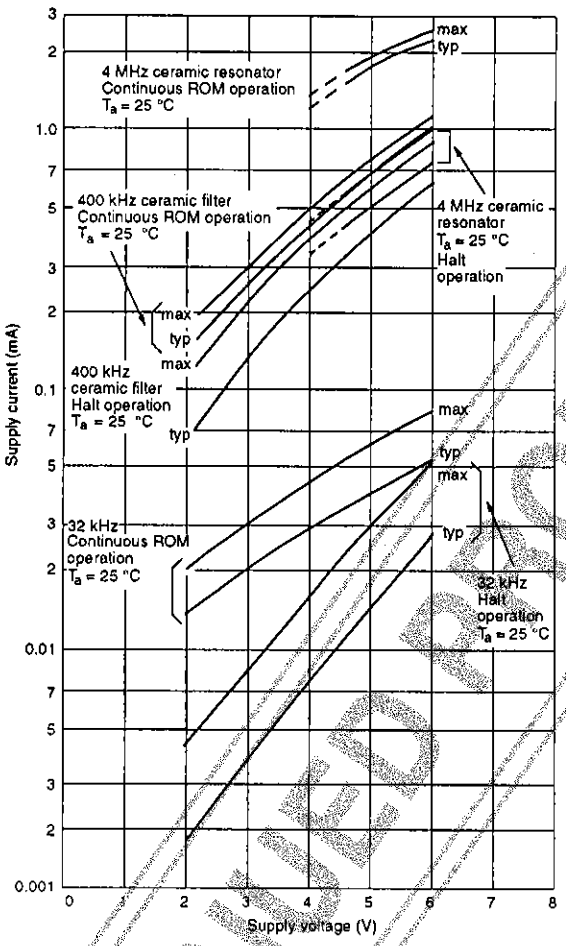
Power-ON reset timing



Note

τ_{VDD} = supply voltage rising-edge time constant
τ_{RES} = RES rising-edge time constant
t_{RES} = reset signal delay time

Supply current vs. voltage



Test Circuits

The following conditions apply to Figures 2 to 8.

- Port S input transistor enabled
- I/O ports in output mode. Data lines HIGH
- RES and INT open. Internal input resistor enabled
- LCD interface open
- 32 to 65 kHz crystal resonator
- 200 kHz to 4 MHz ceramic filter resonator
- C1 = C2 = C3 = 0.1 µF

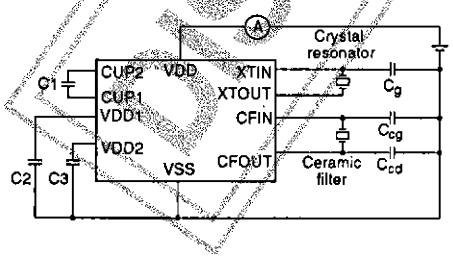


Figure 2. Supply leakage measurement

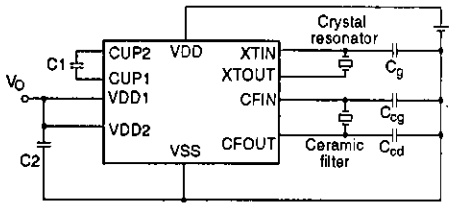


Figure 3. Output voltage measurement 1

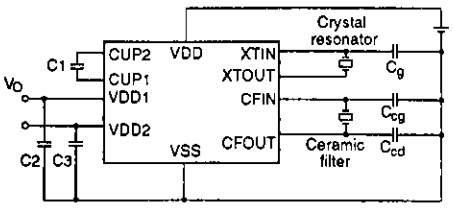


Figure 4. Output voltage measurement 2

Note

STOP mode

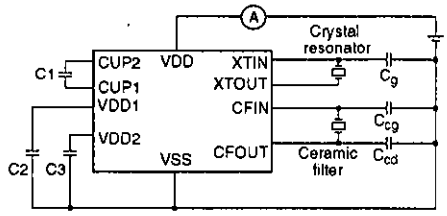


Figure 5. Supply current measurement 1

Notes

1. Oscillator 1 (ceramic filter) stopped
2. 32, 38 or 65 kHz crystal

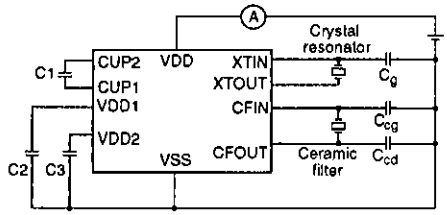


Figure 6. Supply current measurement 2

Note

Oscillator 2 (crystal) stopped

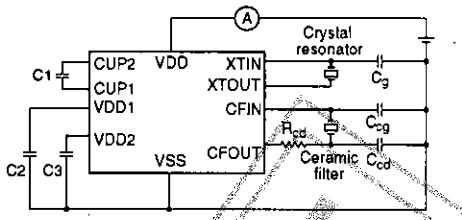


Figure 7. Supply current measurement 3

Note

Oscillator 2 (crystal) stopped

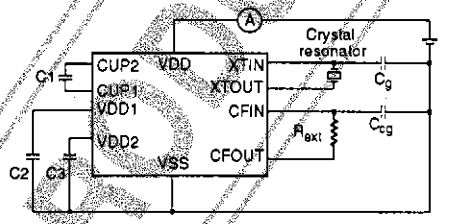


Figure 8. Supply current measurement 4

Note

Oscillator 2 (crystal) stopped

Instruction Set

The instruction set uses the following abbreviations and symbols.

AC	Accumulator	SCF*n*	Start condition flag *n*
AC*n*	Accumulator bit *n*	PDF	Pull-down flag
APG*n*	RAM page flag *n*	OPG*n*	ROM page flag *n*
Breg	Register B	HQF	Hold request flag
BNK	Bank register	HEF*n*	Hold release enable flag *n*
CF	Carry flag	HRF*n*	Hold release request flag *n*
DP	Data pointer	TM	Timer
DPF	Data pointer flag	L	LCD latch
DPL	Data pointer low nibble	STS	Status register
DPH	Data pointer high nibble	MS	Timer mode select
PC	Program counter	()	Contents
RX	Memory location X	←	Transfer direction, result
RX*n*	Memory location X bit *n*	∧	Logical AND
IEF*n*	Interrupt enable flag *n*	∨	Logical OR
WRF*n*	Working register flag *n*	∀	Logical exclusive-OR
E/SF	Interrupt/switch select flag		

Opcode	Description	Operation	Flag	Instruction code							
				D7	D6	D5	D4	D3	D2	D1	D0
		Accumulator									
SR0 X	Memory contents (RX) are shifted right and 0 is entered into the MSB position, and the result is stored in the accumulator.	0 → RX3 → RX2 → RX1 → RX0; AC ← (RX)		0 X7	1 X6	1 X5	0 X4	0 X3	0 X2	0 X1	0 X0
SR1 X	Memory contents (RX) are shifted right and 1 is entered into the MSB position, and the result is stored in the accumulator.	1 → RX3 → RX2 → RX1 → RX0; AC ← (RX)		0 X7	1 X6	1 X5	0 X4	0 X3	0 X2	0 X1	1 X0
SL0 X	Memory contents (RX) are shifted left and 0 is entered into the LSB position, and the result is stored in the accumulator.	RX3 ← RX2 ← RX1 ← RX0 ← 0; AC ← (RX)		0 X7	1 X6	1 X5	0 X4	0 X3	0 X2	1 X1	0 X0
SL1 X	Memory contents (RX) are shifted right and 1 is entered into the LSB position, and the result is stored in the accumulator.	RX3 ← RX2 ← RX1 ← RX0 ← 1; AC ← (RX)		0 X7	1 X6	1 X5	0 X4	0 X3	0 X2	1 X1	1 X0
RRC X	Memory contents (RX) including carry flag are rotated right and the result is stored in the accumulator.	RX3 → RX2 → RX1→ RX0 ↓ ↑←←←←← CF ←←←←←; AC ← (RX)	CF	0 X7	1 X6	1 X5	0 X4	1 X3	0 X2	0 X1	1 X0

Opcode	Description	Operation	Flag	Instruction code							
				D7	D6	D5	D4	D3	D2	D1	D0
RLC X	Memory contents (RX) including carry flag are rotated left and the result is stored in the accumulator.	RX3 ← RX2 ← RX1 ← RX0 ↑ ↓→→→→→ CF →→→→→; AC ← (RX)	CF	0 X7	1 X6	1 X5	0 X4	1 X3	0 X2	1 X1	1 X0
MPF X	ROM page flags 1 and 2, the data pointer flag and carry flag are copied into the accumulator and memory location RX.	(RX), AC ← OPG1, OPG2, DPF, CF		0 X7	1 X6	1 X5	0 X4	1 X3	1 X2	1 X1	1 X0
MROPF X	Memory contents (RX) are copied into ROM page flags 1 and 2, and the carry flag, into the accumulator. The data pointer flag is not affected.	AC ← OPG1, OPG2, CF ← (RX)	CF OPG	0 X7	0 X6	1 X5	0 X4	1 X3	1 X2	1 X1	1 X0
SCF	The carry flag is set to 1.	CF ← 1	CF	1 0	1 0	1 0	1 0	0 0	0 0	0 0	0 1
RCF	The carry flag is cleared to 0 (reset).	CF ← 0	CF	1 0	1 0	1 0	1 0	0 0	0 0	1 0	0 1
Memory manipulation											
SRAPF D	256 × 4-bit memory page units are selected.	APG1 ← D0; APG2 ← D1	APG	1 0	1 0	1 0	0 0	1 0	1 0	1 D1	0 D0
LRAPF X	The RAM page is stored in bits 0 and 1, and the RAM save page is stored in bits 2 and 3 of memory location RX and the accumulator.	RX0 ← APG1; RX1 ← APG2; RX2, RX3 ← RAM save page		0 X7	1 X6	1 X5	0 X4	1 X3	1 X2	0 X1	1 X0
SBNK D	Immediate data (D0 to D3) is copied into the RAM bank register.	BNK ← D0 to D3		1 0	1 0	1 0	0 0	1 D3	0 D2	1 D1	0 D0
MRBK X	Memory contents (RX) are copied into the RAM bank register.	BNK ← (RX)		0 X7	1 X6	1 X5	0 X4	0 X3	1 X2	0 X1	1 X0
MBNK X	The RAM bank register contents are copied into the accumulator and memory location (RX).	AC ← BNK; RX ← BNK		0 X7	1 X6	1 X5	0 X4	1 X3	1 X2	1 X1	0 X0
SDP D	Immediate data (D0 to D7) is copied into the data pointer.	DP ← D0 to D7	DPH DPL	1 D7	1 D6	1 D5	0 D4	1 D3	1 D2	1 D1	1 D0
MRDH X	Memory contents (RX) are copied into the data pointer high nibble.	DPH ← (RX)	DPH	0 X7	1 X6	1 X5	0 X4	0 X3	1 X2	1 X1	0 X0
MRDL X	Memory contents (RX) are copied into the data pointer low nibble.	DPL ← (RX)	DPL	0 X7	1 X6	1 X5	0 X4	0 X3	1 X2	1 X1	1 X0
MDPR X	The data pointer low nibble is copied into the accumulator and memory location RX, and the data pointer high nibble is copied into register B.	RX ← AC ← DPL; Breg ← DPH		0 X7	1 X6	1 X5	1 X4	1 X3	1 X2	0 X1	1 X0
Arithmetic											
ADC X	Memory contents (RX), accumulator contents and carry flag are added and the result is stored in the accumulator.	AC ← (RX) + AC + CF	CF	0 X7	1 X6	0 X5	0 X4	0 X3	0 X2	0 X1	0 X0
ADC* X	Memory contents (RX) and the accumulator contents are added and the result is stored in the accumulator.	AC ← (RX) + AC + CF; RX ← AC	CF	0 X7	1 X6	0 X5	0 X4	0 X3	0 X2	0 X1	1 X0
SBC X	The accumulator contents are subtracted from memory contents (RX) with carry (borrow) and the result is stored in the accumulator.	AC ← (RX) + $\overline{AC}$ + CF	CF	0 X7	1 X6	0 X5	0 X4	0 X3	0 X2	1 X1	0 X0
SBC* X	The accumulator contents are subtracted from memory contents (RX) and the result is stored in the accumulator and memory location RX.	AC ← (RX) + $\overline{AC}$ + CF; RX ← AC	CF	0 X7	1 X6	0 X5	0 X4	0 X3	0 X2	1 X1	1 X0
ADD X	Memory contents (RX) and accumulator contents are added and the result is stored in memory location RX.	AC ← (RX) + AC	CF	0 X7	1 X6	0 X5	0 X4	0 X3	1 X2	0 X1	0 X0
ADD* X	Memory contents (RX) and accumulator contents are added and the result is stored in the accumulator and memory location RX.	AC ← (RX) + AC; RX ← AC	CF	0 X7	1 X6	0 X5	0 X4	0 X3	1 X2	0 X1	1 X0
SUB X	The accumulator contents are subtracted from memory contents (RX) and the result is stored in the accumulator.	AC ← (RX) + $\overline{AC}$ + 1	CF	0 X7	1 X6	0 X5	0 X4	0 X3	1 X2	1 X1	0 X0
SUB* X	The accumulator contents are subtracted from the memory contents (RX) and the result is stored in the accumulator and memory location RX.	AC ← (RX) + $\overline{AC}$ + 1; RX ← AC	CF	0 X7	1 X6	0 X5	0 X4	0 X3	1 X2	1 X1	1 X0
ADN X	Memory contents (RX) and the accumulator contents are added and the result is stored in the accumulator.	AC ← (RX) + AC		0 X7	1 X6	0 X5	0 X4	1 X3	0 X2	0 X1	0 X0
ADN* X	Memory contents (RX) and the accumulator contents are added and the result is stored in the accumulator and memory location RX.	AC ← (RX) + AC; RX ← AC		0 X7	1 X6	0 X5	0 X4	1 X3	0 X2	0 X1	1 X0
ADCI X, Y	Memory contents (RX) and immediate data (Y0 to Y3) are added with carry and the result is stored in the accumulator.	AC ← (RX) + Y + CF	CF	0 Y3	1 Y2	0 Y1	1 Y0	0 X3	0 X2	0 X1	0 X0
ADCI* X, Y	Memory contents (RX) and immediate data (Y0 to Y3) are added with carry and the result is stored in the accumulator and memory location RX.	AC ← (RX) + Y + CF; RX ← AC	CF	0 Y3	1 Y2	0 Y1	1 Y0	0 X3	0 X2	0 X1	1 X0

Opcode	Description	Operation	Flag	Instruction code							
				D7	D6	D5	D4	D3	D2	D1	D0
SBCI X, Y	Immediate data (Y0 to Y3) is subtracted from memory contents (RX) with carry (borrow) and the result is stored in the accumulator.	AC ← (RX) + $\overline{Y}$ + CF	CF	0 Y3	1 Y2	0 Y1	1 Y0	0 X3	0 X2	1 X1	0 X0
SBCI* X, Y	Immediate data (Y0 to Y3) is subtracted from memory contents (RX) with carry (borrow) and the result is stored in the accumulator and memory location RX.	AC ← (RX) + $\overline{Y}$ + CF; RX ← AC	CF	0 Y3	1 Y2	0 Y1	1 Y0	0 X3	0 X2	1 X1	1 X0
ADDI X, Y	Memory contents (RX) and immediate data (Y0 to Y3) are added and the result is stored in the accumulator.	AC ← (RX) + Y	CF	0 Y3	1 Y2	0 Y1	1 Y0	0 X3	1 X2	0 X1	0 X0
ADDI* X, Y	Memory contents (RX) and immediate data (Y0 to Y3) are added and the result is stored in the accumulator.	AC ← (RX) + Y; RX ← AC	CF	0 Y3	1 Y2	0 Y1	1 Y0	0 X3	1 X2	0 X1	1 X0
SUBI X, Y	Immediate data (Y0 to Y3) is subtracted from memory contents (RX) and the result is stored in the accumulator.	AC ← (RX) + $\overline{Y}$ + 1	CF	0 Y3	1 Y2	0 Y1	1 Y0	0 X3	1 X2	1 X1	0 X0
SUBI* X, Y	Immediate data (Y0 to Y3) is subtracted from memory contents (RX) and the result is stored in the accumulator and memory location RX.	AC ← (RX) + $\overline{Y}$ + 1; RX ← AC	CF	0 Y3	1 Y2	0 Y1	1 Y0	0 X3	1 X2	1 X1	1 X0
ADNI X, Y	Memory contents (RX) and immediate data (Y0 to Y3) are added and the result is stored in the accumulator. The carry flag is not affected.	AC ← (RX) + Y		0 Y3	1 Y2	0 Y1	1 Y0	1 X3	0 X2	0 X1	0 X0
ADNI* X, Y	Memory contents (RX) and immediate data (Y0 to Y3) are added and the result is stored in the accumulator and memory location RX. The carry flag is not affected.	AC ← (RX) + Y; RX ← AC		0 Y3	1 Y2	0 Y1	1 Y0	1 X3	0 X2	0 X1	1 X0
Logic											
AND X	Memory contents (RX) and accumulator contents are ANDed and the result is stored in the accumulator.	AC ← (RX) ∧ AC		0 X7	1 X6	0 X5	0 X4	1 X3	0 X2	1 X1	0 X0
AND* X	Memory contents (RX) and accumulator contents are ANDed and the result is stored in the accumulator and memory location RX.	AC ← (RX) ∧ AC; RX ← AC		0 X7	1 X6	0 X5	0 X4	1 X3	0 X2	1 X1	1 X0
EOR X	Memory contents (RX) and accumulator contents are exclusive-ORed and the result is stored in the accumulator.	AC ← (RX) ∀ AC		0 X7	1 X6	0 X5	0 X4	1 X3	1 X2	0 X1	0 X0
EOR* X	Memory contents (RX) and accumulator contents are exclusive-ORed and the result is stored in the accumulator and memory location RX.	AC ← (RX) ∀ AC; RX ← AC		0 X7	1 X6	0 X5	0 X4	1 X3	1 X2	0 X1	1 X0
OR X	Memory contents (RX) and accumulator contents are ORed and the result is stored in the accumulator.	AC ← (RX) ∨ AC		0 X7	1 X6	0 X5	0 X4	1 X3	1 X2	1 X1	0 X0
OR* X	Memory contents (RX) and accumulator contents are ORed and the result is stored in the accumulator and memory location RX.	AC ← (RX) ∨ AC; RX ← AC		0 X7	1 X6	0 X5	0 X4	1 X3	1 X2	1 X1	1 X0
ANDI X, Y	Memory contents (RX) and immediate data (Y0 to Y3) are ANDed and the result is stored in the accumulator.	AC ← (RX) ∧ Y		0 Y3	1 Y2	0 Y1	1 Y0	1 X3	0 X2	1 X1	0 X0
ANDI* X, Y	Memory (RX) contents and immediate data (Y0 to Y3) are ANDed and the result is stored in the accumulator and memory location RX.	AC ← (RX) ∧ Y; RX ← AC		0 Y3	1 Y2	0 Y1	1 Y0	1 X3	0 X2	1 X1	1 X0
EORI X,Y	Memory contents (RX) and immediate data (Y0 to Y3) are exclusive-ORed and the result is stored in the accumulator.	AC ← (RX) ∀ Y		0 Y3	1 Y2	0 Y1	1 Y0	1 X3	1 X2	0 X1	0 X0
EOR* X, Y	Memory contents (RX) and immediate data (Y0 to Y3) are exclusive-ORed and the result is stored in the accumulator and memory location RX.	AC ← (RX) ∀ Y; RX ← AC		0 Y3	1 Y2	0 Y1	1 Y0	1 X3	1 X2	0 X1	1 X0
ORI X,Y	Memory contents (RX) and immediate data (Y0 to Y3) are ORed and the result is stored in the accumulator.	AC ← (RX) ∨ Y		0 Y3	1 Y2	0 Y1	1 Y0	1 X3	1 X2	1 X1	0 X0
ORI* X	Memory contents (RX) and immediate data (Y0 to Y3) are ORed and the result is stored in the accumulator and memory location RX.	AC ← (RX) ∨ Y; RX ← AC		0 Y3	1 Y2	0 Y1	1 Y0	1 X3	1 X2	1 X1	1 X0
Branch and subroutine											
JMP X	The address specified by immediate data (X0 to X10) is jumped to.	PC0 to PC10 ← X0 to X10; PC11 ← OPG1; PC12 ← OPG2		1 X7	1 X6	0 X5	0 X4	0 X3	X10 X2	X9 X1	X8 X0
BAB0 X	The address specified by immediate data (X0 to X10) is branched to if accumulator bit 0 is 1. No operation if bit 0 is 0.	If AC0 = 1; PC0 to PC10 ← X0 to X10; PC11 ← OPG1; PC12 ← OPG2		1 X7	0 X6	0 X5	0 X4	0 X3	X10 X2	X9 X1	X8 X0
BAB1 X	The address specified by immediate data (X0 to X10) is branched to if accumulator bit 1 is 1. No operation if bit 1 is 0.	If AC1 = 1; PC0 to PC10 ← X0 to X10; PC11 ← OPG1; PC12 ← OPG2		1 X7	0 X6	0 X5	0 X4	1 X3	X10 X2	X9 X1	X8 X0
BAB2 X	The address specified by immediate data (X0 to X10) is branched to if accumulator bit 2 is 1. No operation if bit 2 is 0.	If AC2 = 1; PC0 to PC10 ← X0 to X10; PC11 ← OPG1; PC12 ← OPG2		1 X7	0 X6	0 X5	1 X4	0 X3	X10 X2	X9 X1	X8 X0
BAB3 X	The address specified by immediate data (X0 to X10) is branched to if accumulator bit 3 is 1. No operation if bit 3 is 0.	If AC3 = 1; PC0 to PC10 ← X0 to X10; PC11 ← OPG1; PC12 ← OPG2		1 X7	0 X6	0 X5	1 X4	1 X3	X10 X2	X9 X1	X8 X0

Opcode	Description	Operation	Flag	Instruction code							
				D7	D6	D5	D4	D3	D2	D1	D0
BAZ X	The address specified by immediate data (X0 to X10) is branched to if the accumulator contents are 0. No operation if the contents are not 0.	If AC = 0; PC0 to PC10 ← X0 to X10; PC11 ← OPG1; PC12 ← OPG2		1 X7	0 X6	1 X5	1 X4	0 X3	X10 X2	X9 X1	X8 X0
BANZ X	The address specified by immediate data (X0 to X10) is branched to if the accumulator contents are not 0. No operation if the contents are 0.	If AC ≠ 0; PC0 to PC10 ← X0 to X10; PC11 ← OPG1; PC12 ← OPG2		1 X7	0 X6	1 X5	0 X4	0 X3	X10 X2	X9 X1	X8 X0
BCH X	The address specified by immediate data (X0 to X10) is branched to if the carry flag is 1. No operation if the carry flag is 0.	If CF = 1; PC0 to PC10 ← X0 to X10; PC11 ← OPG1; PC12 ← OPG2		1 X7	0 X6	1 X5	1 X4	1 X3	X10 X2	X9 X1	X8 X0
BCNH X	The address specified by immediate data (X0 to X10) is branched to if the carry flag is 0. No operation if the carry flag is 1.	If CF = 0; PC0 to PC10 ← X0 to X10; PC11 ← OPG1; PC12 ← OPG2		1 X7	0 X6	1 X5	0 X4	1 X3	X10 X2	X9 X1	X8 X0
CALL X	The subroutine address specified by immediate data (X0 to X10) is called.	(STACK) ← PC + 1; PC0 to PC10 ← X0 to X10; PC11 ← OPG1; PC12 ← OPG2		1 X7	1 X6	0 X5	0 X4	1 X3	X10 X2	X9 X1	X8 X0
RTS	The previous (calling) subroutine is returned to.	PC0 to PC12, DPF ← (STACK)	DPF	1 0	1 0	1 0	1 0	1 0	0 0	0 0	0 0
RTSR	The previous (calling) subroutine is returned to and the halt condition is released.	PC0 to PC12, DPF ← (STACK)	DPF	1 0	1 0	1 0	1 0	1 0	0 0	0 0	0 1
POP	The stack pointer is moved to the stack pointer minus 1.	STACK ← STACK − 1		1 0	1 0	1 0	1 0	1 0	0 0	0 0	1 0
CPU control											
SLOW	Low-speed system clock is selected.	SLOW		1 0	1 0	1 1	1 0	1 0	1 0	0 0	0 0
FAST	High-speed system clock is selected.	FAST		1 0	1 1	1 0	1 0	1 0	1 0	0 0	0 0
HALT	The system is halted and the CPU ceases operation. HALT mode is released when an interrupt occurs or one of the stop condition flags changes state.	HALT		1 1	1 0	1 0	1 0	1 0	1 0	0 0	0 0
HLTF	The system clock is halted and the CPU ceases operation when high-speed system clock mode is selected.	FAST and HALT		1 1	1 1	1 0	1 0	1 0	1 0	0 0	0 0
HLTL	The system clock is halted and the CPU ceases operation when low-speed system clock mode is selected.	SLOW and HALT		1 1	1 0	1 1	1 0	1 0	1 0	0 0	0 0
STOP	The system clock is halted and the CPU ceases operation, and then the oscillators are halted.	STOP		1 0	1 0	1 0	1 0	1 0	1 0	0 0	1 0
STPF	The system clock is halted and the CPU ceases operation, and then the oscillators are halted when high-speed system clock mode is selected.	FAST and STOP		1 0	1 1	1 0	1 0	1 0	1 0	0 0	1 0
STPL	The system clock is halted and the CPU ceases operation, and then the oscillators are halted when low-speed system clock mode is selected.	SLOW and STOP		1 0	1 0	1 1	1 0	1 0	1 0	0 0	1 0
SHRF D	Interrupt and hold conditions are selected by immediate data (A0 to A7) as follows. D0 INT input interrupt requests are disabled when 0, and enabled, when 1. D1 Timer 1 interrupt requests are disabled when 0, and enabled, when 1. D2 Timer 2 interrupt requests are disabled when 0, and enabled, when 1. D3 Serial I/O port interrupt requests are disabled when 0, and enabled, when 1. D4 Frequency divider overflow hold release requests are disabled when 0, and enabled, when 1. D5 Timer 1 underflow hold release requests are disabled when 0, and enabled, when 1. D6 Timer 2 underflow hold release requests are disabled when 0, and enabled, when 1. D7 Serial I/O register overflow hold release requests are disabled when 0, and enabled, when 1.		IEF0 to IEF3, HRF0 to HRF3	1 D7	1 D6	1 D5	1 D4	1 D3	0 D2	1 D1	0 D0
SIC D	Interrupt flags (IEF0 to IEF3) are set or cleared by immediate data (D0 to D3). Each interrupt is disabled when the corresponding flag is 0, and enabled, when 1.	IEF0 to IEF3 ← D0 to D3	IEF0 to IEF3	1 0	1 0	1 0	1 0	1 D3	0 D2	1 D1	1 D0
MRI X	Interrupt flags (IEF0 to IEF3) are set or cleared by memory contents (RX). Each interrupt is disabled when the corresponding flag is 0, and enabled, when 1.	IEF0 to IEF3 ← (RX)	IEF0 to IEF3	0 X7	1 X6	1 X5	0 X4	0 X3	1 X2	0 X1	0 X0
PLC D	The following internal resets are generated when the corresponding immediate data bits (D0 to D7) are set to 1. D0 The INT input halt release flag is reset. D1 Timer 1 halt release flag is reset. D2 Timer 2 halt release flag is reset. D3 Serial I/O halt release flag is reset. D4 Frequency divider overflow halt release flag is reset. D5 Frequency divider stages 11 to 15 are reset. D6 Watchdog timer 1 is reset. D7 Watchdog timer 2 is reset.			1 D7	1 D6	1 D5	1 D4	1 D3	1 D2	1 D1	0 D0

Opcode	Description	Operation	Flag	Instruction code							
				D7	D6	D5	D4	D3	D2	D1	D0
MSB X	Start condition flags (SCF0 to SCF3) are copied into the accumulator and memory location RX. They are set by the following conditions. SCF0 The INT input changes state. SCF1 Port K (K1 to K4) changes state. SCF2 Status register 4 changes state. SCF3 Port S (S1 to S4) changes state.	AC ← (SCF0 to SCF3); RX ← AC		0 X7	1 X6	1 X5	1 X4	1 X3	0 X2	0 X1	0 X0
MSC X	Start condition flags (SCF4 to SCF7) are copied into the accumulator and memory location RX. They are set by the following conditions. SCF4 The frequency divider overflows. SCF5 Timer 1 underflows. SCF6 Timer 2 underflows. SCF7 Serial I/O input (SO1), output (SO2) or (S04) changes state.	AC ← (SCF4 to SCF7); RX ← AC		0 X7	1 X6	1 X5	1 X4	1 X3	0 X2	0 X1	1 X0
		Timer control									
MSTR X	Accumulator bits 0 and 1 are cleared to 0, the INT input state is copied into accumulator bit 2 and the LCD strobe flag is copied into accumulator bit 3. The accumulator contents are copied into memory location RX.	AC0, AC1 ← 0; AC2 ← INT state; AC3 ← STBL; RX ← AC	STBL	0 X7	1 X6	1 X5	1 X4	0 X3	1 X2	1 X1	0 X0
STM1 M, D	Timer mode is selected by immediate data (M0 to M1) and timer 1 is loaded with immediate data (D0 to D7). Timer 1 then starts.	MS ← M0, M1; TM1 ← D0 to D7		1 D7	1 D6	1 D5	0 D4	0 D3	0 D2	M1 D1	M0 D0
STM2 M, D	Timer mode is selected by immediate data (M0 to M1) and timer 2 is loaded with immediate data (D0 to D7). Timer 2 then starts.	MS ← M0, M1; TM2 ← D0 to D7		1 D7	1 D6	1 D5	0 D4	0 D3	1 D2	M1 D1	M0 D0
MRTM2 M, X	Timer mode is selected by immediate data (M0 to M1) and timer 2 is loaded with memory contents (RX). Timer 2 then starts.	MS ← M0 to M1; TM2 ← (RX)		0 X7	0 X6	1 X5	0 X4	0 X3	1 X2	M1 X1	M0 X0
MT2R X	Timer 2 low byte is copied into the accumulator and memory location RX, timer 2 high byte is copied into register B.	RX ← AC ← TM2L; Breg ← TM2H		0 X7	1 X6	1 X5	1 X4	1 X3	0 X2	1 X1	1 X0
		Serial I/O register									
MSOR X	The serial I/O register low byte is copied into the accumulator and memory location RX, and the serial I/O register high byte is copied into register B	RX ← AC ← SIOL; Breg ← SIOH		0 X7	1 X6	1 X5	1 X4	1 X3	1 X2	0 X1	0 X0
MRSI X	Memory contents (RX) are copied into the accumulator and the serial I/O register low byte, and register B contents are copied into the serial I/O register high byte.	SIOL ← AC ← (RX) SIOH ← Breg		0 X7	1 X6	1 X5	0 X4	1 X3	0 X2	1 X1	0 X0
MSCF X	Status register 2 contents are copied into the accumulator and memory location RX. Status register 2 bit allocation is as follows. CSTF (bit 0) The serial I/O start flag is cleared to 0 during normal operation and set to 1 to start the counter. SIOF (bit 1) The serial I/O status flag is cleared to 0 to halt the counter and set to 1 during normal operation. OSELF (bit 2) The serial I/O output enable flag is cleared to 0 to enable the register output and set to 1 to disable the output. ICF (bit 3) The clock flag is cleared to 0 for an external clock and set to 1 for an internal clock.	AC ← STS2; RX ← AC		0 X7	1 X6	1 X5	1 X4	0 X3	1 X2	1 X1	1 X0
SSCF D	Immediate data (D0 to D3) is copied into status register 2.	STS2 ←D0 to D3		1 0	1 0	1 0	0 0	1 D3	0 D2	1 D1	1 D0
MRSC X	Memory contents (RX) are copied into the accumulator and status register 2.	STS2 ← AC ← (RX)		0 X7	1 X6	1 X5	0 X4	1 X3	0 X2	0 X1	0 X0
		Data manipulation									
MRW W, X	Memory contents (RX) are copied into the accumulator and memory location RW.	AC ← (RX); RW ← AC		0 X7	0 X6	1 X5	1 X4	0 X3	W2 X2	W1 X1	W0 X0
MWR X, W	Memory contents (RW) are copied into the accumulator and memory location RX.	AC ← (RW); RX ← AC		0 X7	0 X6	1 X5	1 X4	1 X3	W2 X2	W1 X1	W0 X0
LDA X	Memory contents (RX) are copied into the accumulator.	AC ← (RX)		0 X7	1 X6	1 X5	0 X4	1 X3	1 X2	0 X1	0 X0
STA X	The accumulator contents are copied into memory location RX.	RX ← AC		0 X7	1 X6	1 X5	1 X4	1 X3	1 X2	1 X1	1 X0
LDS X, D	Immediate data (D0 to D3) is copied into the accumulator and memory location RX.	AC ← D0 to D3; RX ← AC		1 X7	1 X6	0 X5	1 X4	D3 X3	D2 X2	D1 X1	D0 X0
MRB X	Memory contents (RX) are copied into register B.	Breg ← (RX)		0 X7	0 X6	1 X5	0 X4	1 X3	1 X2	1 X1	0 X0
MBR X	Register B contents are copied into the accumulator and memory location RX.	AC ← Breg; RX ← AC		0 X7	1 X6	1 X5	1 X4	1 X3	1 X2	1 X1	0 X0
IPS X	Port S data (S1 to S4) is copied into the accumulator and memory location RX.	AC ← S1 to S4; RX ← AC		0 X7	1 X6	1 X5	1 X4	0 X3	0 X2	0 X1	0 X0

Opcode	Description	Operation	Flag	Instruction code							
				D7	D6	D5	D4	D3	D2	D1	D0
IPK X	Port K data (K1 to K4) is copied into the accumulator and memory location RX.	AC ← K1 to K4; RX ← AC		0 X7	1 X6	1 X5	1 X4	0 X3	0 X2	0 X1	1 X0
IPM X	Port M data (M1 to M4) is copied into the accumulator and memory location RX.	AC ← M1 to M4; RX ← AC		0 X7	1 X6	1 X5	1 X4	0 X3	0 X2	1 X1	0 X0
IPP X	Port P data (P1 to P4) is copied into the accumulator and memory location RX.	AC ← P1 to P4; RX ← AC		0 X7	1 X6	1 X5	1 X4	0 X3	0 X2	1 X1	1 X0
IPSO X	Port SO data (SO1 to SO4) is copied into the accumulator and memory location RX.	AC ← SO1 to SO4; RX ← AC		0 X7	1 X6	1 X5	1 X4	0 X3	1 X2	0 X1	0 X0
IPA X	Port A data (A1 to A4) is copied into the accumulator and memory location RX.	AC ← A1 to A4; RX ← AC		0 X7	1 X6	1 X5	1 X4	0 X3	1 X2	0 X1	1 X0
WRT Y, X	Memory contents (RX) are copied into the LCD decoder and LCD latch (L). The carry flag is copied into the LCD latch (L). Immediate data Y0 to Y3 is copied to the strobe decoder.	LCD decoder ← (RX); L ← LCD decoder; L ← CF; Strobe decoder ← Y0 to Y3		0 X7	0 X6	0 X5	0 X4	Y3 X3	Y2 X2	Y1 X1	Y0 X0
WRP Y, X	Memory (RX) and register B contents are copied into the LCD latch (L). Immediate data Y0 to Y3 is copied to the strobe decoder.	L ← (RX); L ← Breg; Strobe decoder ← Y0 to Y3		0 X7	0 X6	0 X5	1 X4	Y3 X3	Y2 X2	Y1 X1	Y0 X0
OPN X	Memory contents (RX) are loaded into port N.	N1 to N4 ← (RX)		0 X7	0 X6	1 X5	0 X4	1 X3	0 X2	0 X1	0 X0
OPK X	Memory contents (RX) are loaded into port K.	K1 to K4 ← (RX)		0 X7	0 X6	1 X5	0 X4	1 X3	0 X2	0 X1	1 X0
OPM X	Memory contents (RX) are loaded into port M.	M1 to M4 ← (RX)		0 X7	0 X6	1 X5	0 X4	1 X3	0 X2	1 X1	0 X0
OPP X	Memory contents (RX) are loaded into port P.	P1 to P4 ← (RX)		0 X7	0 X6	1 X5	0 X4	1 X3	0 X2	1 X1	1 X0
OPSO X	Memory contents (RX) are loaded into port SO.	SO1 to SO4 ← (RX)		0 X7	0 X6	1 X5	0 X4	1 X3	1 X2	0 X1	0 X0
OPA X	Memory contents (RX) are loaded into port A.	A1 to A4 ← (RX)		0 X7	0 X6	1 X5	0 X4	1 X3	1 X2	0 X1	1 X0
		Flag setting/resetting									
SF1 D	The following functions are selected when the corresponding immediate data bit (D0 to D7) is set to 1. D0 The carry flag (CF) is set to 1. D1 The data pointer flag (DPF) is set to 1. D2 125/250 millisecond frequency divider overflow is selected. D3 Port K output mode is selected. D4 Port M output mode is selected. D5 Port P output mode is selected. D6 Port SO output mode is selected. D7 Port A output mode is selected.		DPF, HRFO, CF	1 D7	1 D6	1 D5	1 D4	0 D3	0 D2	0 D1	0 D0
RF1 D	The following functions are selected when the corresponding immediate data bit (D0 to D8) is set to 1. D0 The carry flag (CF) is reset (cleared). D1 The data pointer flag (DPF) is reset (cleared). D2 500/1000 millisecond frequency divider overflow is selected. D3 Port K input mode is selected. D4 Port M input mode is selected. D5 Port P input mode is selected. D6 Port SO input mode is selected. D7 Port A input mode is selected. D8 The serial I/O counter is reset.		DPF, HRFO, CF	1 D7	1 D6	1 D5	1 D4	0 D3	0 D2	1 D1	D8 D0
SF2 D	The following functions are selected when the corresponding immediate data bit (D0 to D8) is set to 1. D0 The interrupt input (INT) hold release is enabled. D1 10H to 1FH LCD strobe is selected. D2 Port S pull-up/pull-down transistor is enabled. D3 Port K pull-up/pull-down transistor is enabled. D4 Port M (p-channel, open-drain output) pull-up/pull-down transistor is enabled. D5 Port P (p-channel, open-drain output) pull-up/pull-down transistor is enabled. D6 Port SO (n-channel, open-drain output) pull-up/pull-down transistor is enabled. D7 Port A (p-channel, open-drain output) pull-up/pull-down transistor is enabled. D8 1/2 carrier signal duty is selected.			1 D7	1 D6	1 D5	1 D4	0 D3	1 D2	0 D1	D8 D0
RF2 D	The following functions are selected when the corresponding immediate data bit (D0 to D8) is set to 1. D0 The interrupt input (INT) hold release is disabled. D1 00H to 0FH LCD strobe is selected. D2 Port S pull-up/pull-down transistor is disabled. D3 Port K pull-up/pull-down transistor is disabled. D4 Port M (CMOS output) pull-up/pull-down transistor is disabled. D5 Port P (CMOS output) pull-up/pull-down transistor is disabled. D6 Port SO (CMOS output) pull-up/pull-down transistor is disabled. D7 Port A (CMOS output) pull-up/pull-down transistor is disabled. D8 1/3 carrier signal duty is selected.			1 D7	1 D6	1 D5	1 D4	0 D3	1 D2	1 D1	D8 D0
COMD D	Same as the SF1 instruction for D3 to D7			1 D7	1 D6	1 D5	1 D4	0 D3	0 0	0 0	0 0

Opcode	Description	Operation	Flag	Instruction code D7	D6	D5	D4	D3	D2	D1	D0
CIMD D	Same as the RF1 instruction for D3 to D7			1 D7	1 D6	1 D5	1 D4	0 D3	0 0	1 0	0 0
SPDF D	Same as the SF2 instruction for D2 to D7			1 D7	1 D6	1 D5	1 D4	0 D3	1 D2	0 0	0 0
RPDF D	Same as the SF2 instruction for D2 to D7			1 D7	1 D6	1 D5	1 D4	0 D3	1 D2	1 0	0 0
SSW D	The following functions are selected by the corresponding immediate data bit (D0 to D7). D0 S1 rising-edge or falling-edge interrupt request (and halt release) enable when 1, and disable when 0. D1 S2 rising-edge or falling-edge interrupt request (and halt release) enable when 1, and disable when 0. D2 S3 rising-edge or falling-edge interrupt request (and halt release) enable when 1, and disable when 0. D3 S4 rising-edge or falling-edge interrupt request (and halt release) enable when 1, and disable when 0. D4 Port K (K1 to K4) interrupt request (and halt release) inputs are active on a rising edge, when 1. D5 Port K (K1 to K4) interrupt request (and halt release) inputs are active on a falling edge, when 1. D6 Port S is disabled for direct transfer of input data to the accumulator and memory location (RX) when 0, and enabled, when 1. D7 7.8 milliseconds debounce delay is selected for port S and port K when 0, and 2 milliseconds, when 1 for a clock frequency of 32.768 kHz.			1 D7	1 D6	1 D5	0 D4	1 D3	0 D2	0 D1	0 D0
STOF	Carrier signal enable			1 1	1 0	1 1	0 0	1 0	0 0	0 0	1 0
RTOF	Carrier signal disable			1 1	1 0	1 0	0 1	1 0	0 0	0 0	1 0
Miscellaneous											
SROPF D	Immediate data (D0 and D1) is copied into OPG1 and OPG2, respectively.	OPG1 ← D0, OPG2 ← D1	OPG	1 0	1 0	1 0	0 0	1 0	0 0	0 D1	1 D0
SAS D	The alarm output frequency (N4 output) is selected by immediate data (D0 to D8), as follows.			1 D7	1 D6	1 D5	0 D4	1 D3	1 D2	0 D1	D8 D0
NOP	No operation	No operation		1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1

Output frequency (Hz)	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	×	×	1	0	0	0	0	0
2	0	×	×	0	1	0	0	0	0
4	0	×	×	0	0	1	0	0	0
8	0	×	×	0	0	0	1	0	0
16	0	×	×	0	0	0	0	1	0
32	0	×	×	0	0	0	0	0	1
1 kHz	1	0	0	×	×	×	×	×	×
2 kHz	1	0	1	×	×	×	×	×	×
4 kHz	1	1	0	×	×	×	×	×	×
DC	1	1	1	×	×	×	×	×	×

Note
Clock frequency = 32.768 kHz

Opcode/Instruction Code Summary

High nibble (hex)	Instruction code: Low nibble (hex) 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	WRT															
	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
1	WRP															
	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
2					MRTM2				OUT						MRB	MROPF
					+ 1	+ 8	+ 64	EXT	OPN	OPK	OPM	OPP	OPSO	OPA		
3	MRW								MWR							
4	ADC	ADC*	SBC	SBC*	ADD	ADD*	SUB	SUB*	ADN	ADN*	AND	AND*	EOR	EOR*	OR	OR*
5	ADCI	ADCI*	SBCI	SBCI*	ADDI	ADDI*	SUBI	SUBI*	ADNI	ADNI*	ANDI	ANDI*	EORI	EORI*	ORI	ORI*

Instruction code																
High nibble (hex)	Low nibble (hex)															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
6	SR0	SR1	SL0	SL1	MRI	MRBK	MRDH	MRDL	MRSC	RRC	MRSI	RLC	LDA	LRAPF	MBNK	MPF
7	INPUT						MSTR	MSCF	MSB	MSC		MT2R	MSOR	MDPR	MBR	STA
	IPS	IPK	IPM	IPP	IPSO	IPA										
8	BAB0								BAB1							
9	BAB2								BAB3							
A	BANZ								BCNH							
B	BAZ								BCH							
C	JMP								CALL							
D	LDS															
E	STM1				STM2				SSW	SROPF	SBNK	SSCF	SAS		SRAPF	SDP
F	SF1		RF1		SF2		RF2		RTS	POP	SHRF	SIC	HALT	STOP	PLC	NOP

User Mask Options

The following user-specified mask options are available.

Oscillator Options

RC oscillator and crystal resonator

Frequency divider internal outputs (ϕ1 to ϕ15) are used for time base generation, LCD drive waveform generation and ports S and K switch debounce. Cycle time is $4n$ times the RC oscillator period where n, the divider ratio, is 2. The RC oscillator frequency range is 200 kHz to 1 MHz and the crystal resonator frequency can be either 32, 38 or 65 kHz.

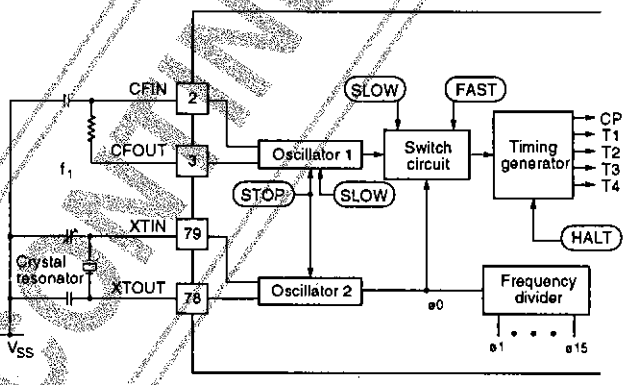


Figure 9. RC oscillator and crystal resonator

Ceramic filter and crystal resonators

Frequency divider internal outputs (ϕ1 to ϕ15) are used for time base generation, LCD drive waveform generation and ports S and K switch debounce. Oscillator 1 stops when the SLOW instruction is executed. Cycle time is $4n$ times the ceramic filter resonator period where n, the divider ratio, is 2. The ceramic filter resonator frequency range is 400 kHz to 4 MHz and the crystal resonator frequency can be either 32, 38 or 65 kHz.

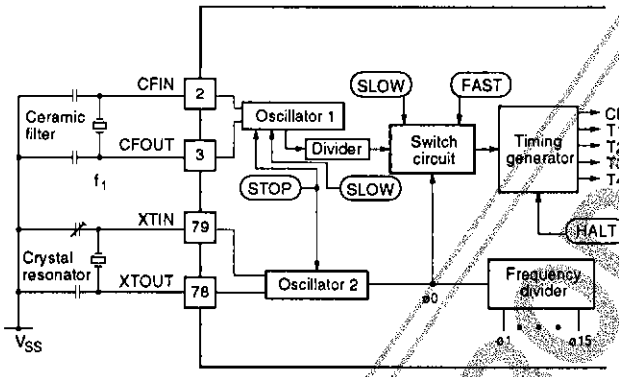


Figure 10. Ceramic filter and crystal resonators

RC oscillator

Frequency divider internal outputs (ϕ1 to ϕ15) are used for time base generation, LCD drive waveform generation and ports S and K switch debounce. Cycle time is four times the RC oscillator period. The RC oscillator frequency range is 200 kHz to 1 MHz.

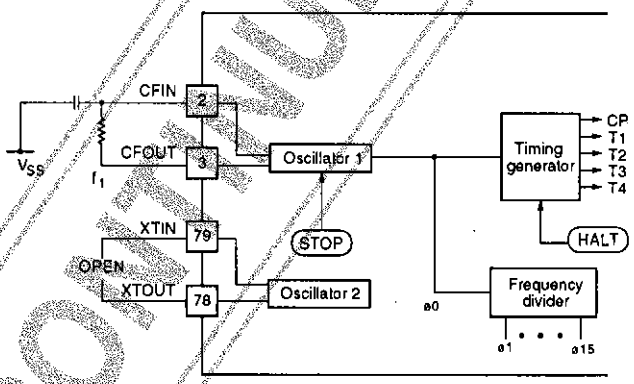


Figure 11. RC oscillator

Ceramic filter resonator

Frequency divider internal outputs (ϕ1 to ϕ15) are used for time base generation, LCD drive waveform generation and ports S and K switch debounce. Oscillator 1 stops when the SLOW instruction is executed. Cycle time is $4n$ times the ceramic filter resonator period where n, the divider ratio, is 2. The ceramic filter resonator frequency range is 400 kHz to 4 MHz.

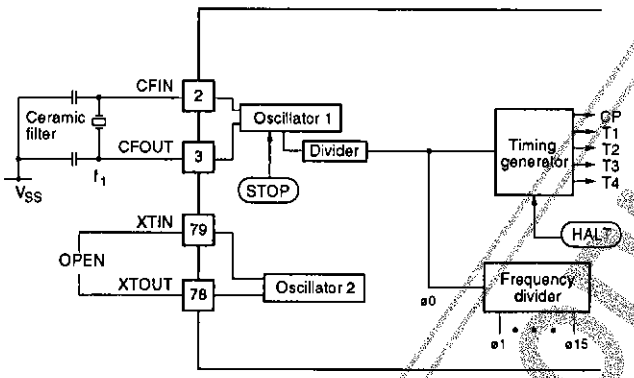


Figure 12. Ceramic filter resonator

Crystal resonator

Frequency divider internal outputs (ϕ1 to ϕ15) are used for time base generation, LCD drive waveform generation and ports S and K switch debounce. Cycle time is four times the crystal resonator period. The crystal resonator frequency can be either 32, 38 or 65 kHz.

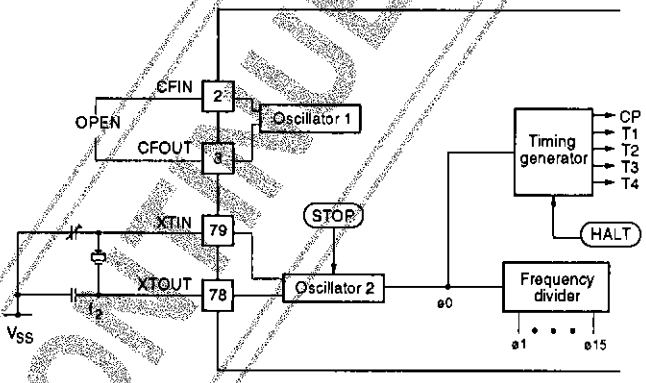


Figure 13. Crystal resonator

External input

Frequency divider internal outputs (ϕ1 to ϕ15) are used for time base generation, LCD drive waveform generation and ports S and K switch debounce. Cycle time is $4n$ times the external clock period where n, the divider ratio, is 2.

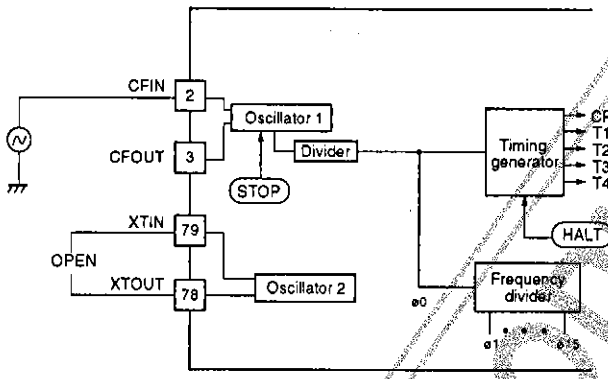


Figure 14. External input

32 kHz crystal oscillator

A 200 kΩ (typ) resistor R_d is incorporated for 32 kHz crystal oscillator operation.

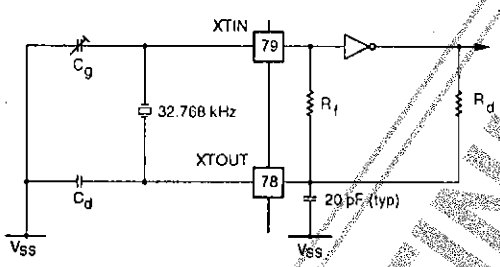


Figure 15. 32 kHz crystal

38 or 65 kHz crystal oscillator

Resistor R_d is removed for 38 or 65 kHz operation. Frequency divider internal outputs (ϕ1 to ϕ15) are used for time base generation, LCD drive waveform generation and ports S and K switch debounce. Cycle time is four times the crystal resonator period. Oscillator 1 stops when the SLOW instruction is executed.

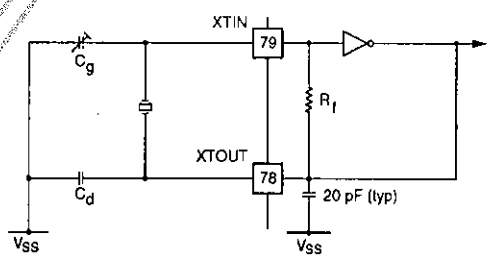


Figure 16. 38 or 65 kHz crystal

I/O Port Options

I/O port input transistors

Ports S, K, M, P, SO and A can have either pull-up or pull-down transistors. These transistors are ON during a reset and OFF after the reset. They are enabled and disabled using the SF2 and RF2 instructions, respectively.

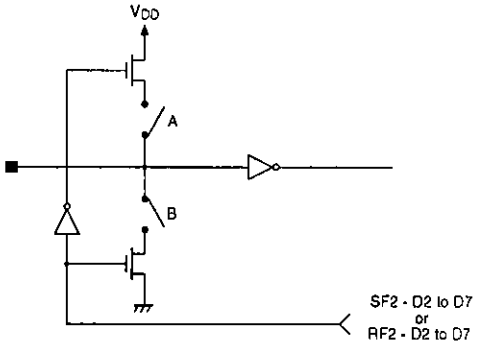


Figure 17. I/O port input transistors

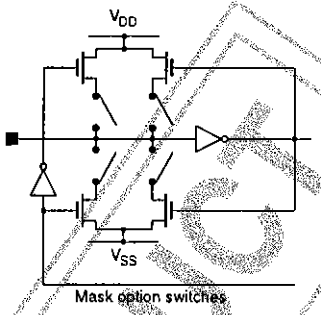


Figure 18. I/O port structure

I/O port hold level

Ports S, K, M, P, SO and A can have either LOW- or HIGH-level hold transistors or neither. When the input is open, the pull-up transistor or pull-down transistor, whichever is selected, turns ON before and turns OFF after reading the input state. At this point, the input is floating and either the LOW-level or HIGH-level transistor operates to hold the input state.

The hold transistors do not operate when

- either the pull-up or pull-down transistor is ON.
- an external signal is applied (the line is not floating).

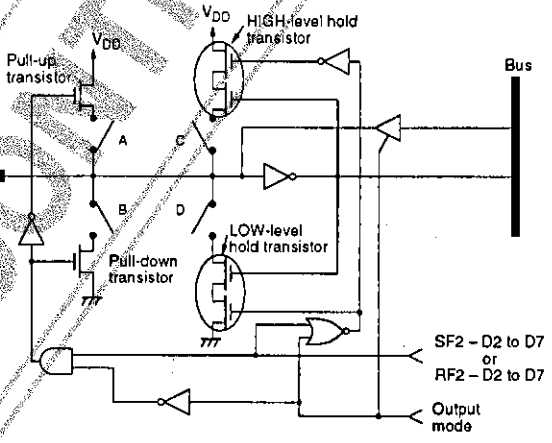


Figure 19. I/O port hold level

Option	Switch	Type			
		1	2	3	4
Pull-up	A	ON	ON	–	–
Pull-down	B	–	–	ON	ON
LOW-level hold transistor	C	–	–	ON	–
HIGH-level hold transistor	D	ON	–	–	–

INT Input Options

The interrupt (INT) input has three mask options—pull-up or pull-down resistor, LOW- or HIGH-level hold transistor and rising- or falling-edge detector circuit.

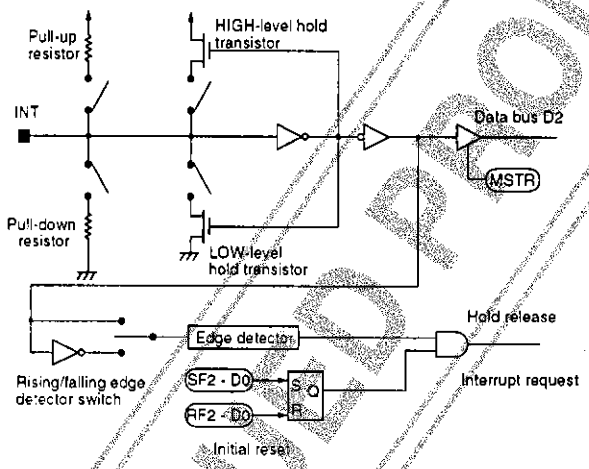


Figure 20. INT input options

RES Input Options

The reset (RES) input has two mask options—pull-up or pull-down resistor and LOW- or HIGH-level reset.

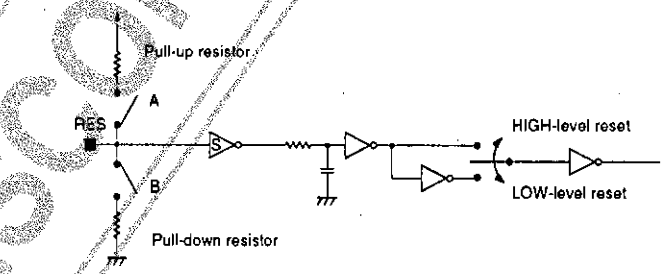


Figure 21. RES input options

Port N Output Options

Port N outputs have two mask options—open-drain (n-channel) or complementary and LOW- or HIGH-level after reset.

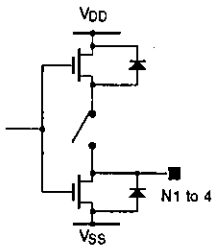


Figure 22. Port N output options

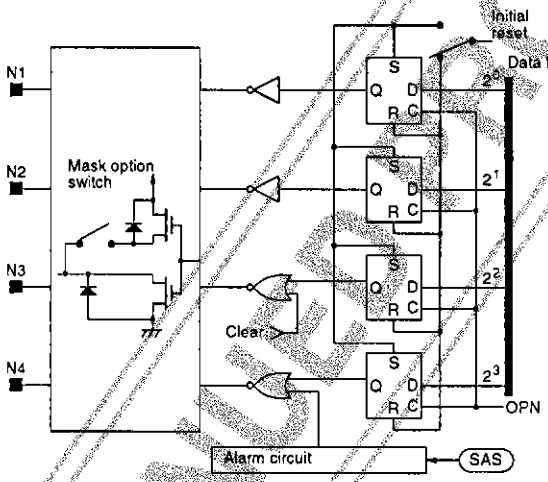


Figure 23. Port N output

Overflow Timer Options

The 15-stage overflow timer has two mask options—125 or 250 ms and 500 or 1000 ms delays (32.768 kHz input clock). The SF1 instruction immediate data bit D2 is used to select the 125/250 ms delay, and the RF1 instruction bit D2, the 500/1000 ms range.

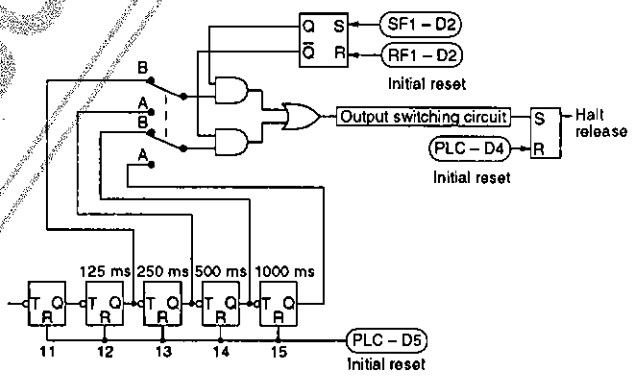


Figure 24. Overflow timer options

Port K Edge Detector Options

Port K can be masked for either pull-down or pull-up and level-hold transistors. Selecting the pull-down transistor configures port K as a falling-edge detector (option A), and the pull-up transistor, as a rising-edge detector (option B).

The detector is disabled until all inputs are active. For example, all inputs must be HIGH before the falling-edge detector (option A) is enabled.

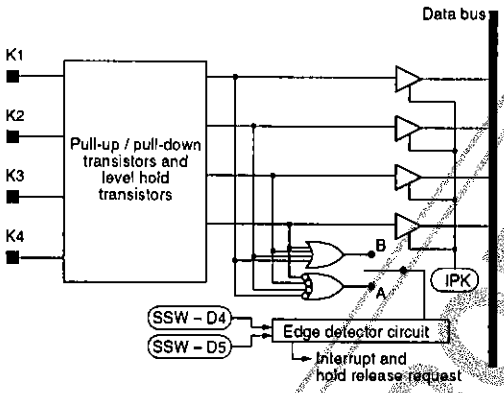


Figure 25. Port K edge detector options

Summary

Option	Selection
Ports S, K, P, M, A and SO transistor	Pull-up or pull-down. All ports are selected together.
Ports S, K, P, M, A and SO level hold transistor	Connected or not connected. Each port is selected independently.
INT input edge and resistor	Rising edge (pull-down resistor) or falling edge (pull-up resistor)
INT input edge with no resistor	Rising edge (open input) or falling edge (open input)
INT hold transistor	LOW- or HIGH-level
RES input level and resistor	LOW-level reset (pull-up resistor) or HIGH-level reset (pull-down resistor)
RES input level with no resistor	LOW-level reset (open input) or HIGH-level reset (open input)
Port N output type	Open-drain (n-channel) or complementary (CMOS). Each output is selected independently.
Port N state after reset	LOW- or HIGH-level
Oscillator 1 and 2 combination	Oscillator 1 only (ceramic filter), oscillator 1 only (RC circuit), oscillator 2 only (crystal), oscillator 1 only (external input), oscillator 1 and 2 (ceramic filter and crystal), oscillator 1 and 2 (RC circuit and crystal) or oscillator 1 and 2 (external input and crystal)
Ceramic filter and external input frequency	400 or 800 kHz and 1, 2 or 4 MHz, respectively
Crystal frequency	32, 38 or 65 kHz
15-stage overflow counter divide ratio	$\Phi \div 2048$ and $\Phi \div 8196$ or $\Phi \div 4096$ and $\Phi \div 16384$. Note that one of the two ratios selected by mask option is enabled using the SF1 and RF1 instructions immediate data bit D2.
Serial I/O internal clock period	Cycle time × 1 × 2, cycle time × 2 × 2 or cycle time × 4 × 2
LCD drive waveform	1/1 bias and 1/1 duty, 1/2 bias and 1/2 duty, 1/2 bias and 1/3 duty, 1/2 bias and 1/4 duty, 1/3 bias and 1/3 duty or 1/3 bias and 1/4 duty
LCD control frequency	Slow, medium or fast
Internal reset circuit	Enabled or disabled
LCD segment output state after reset	ON or OFF
LCD output drivers	LOW- or HIGH-level

Note

Φ = counter input clock frequency

LCD Interface

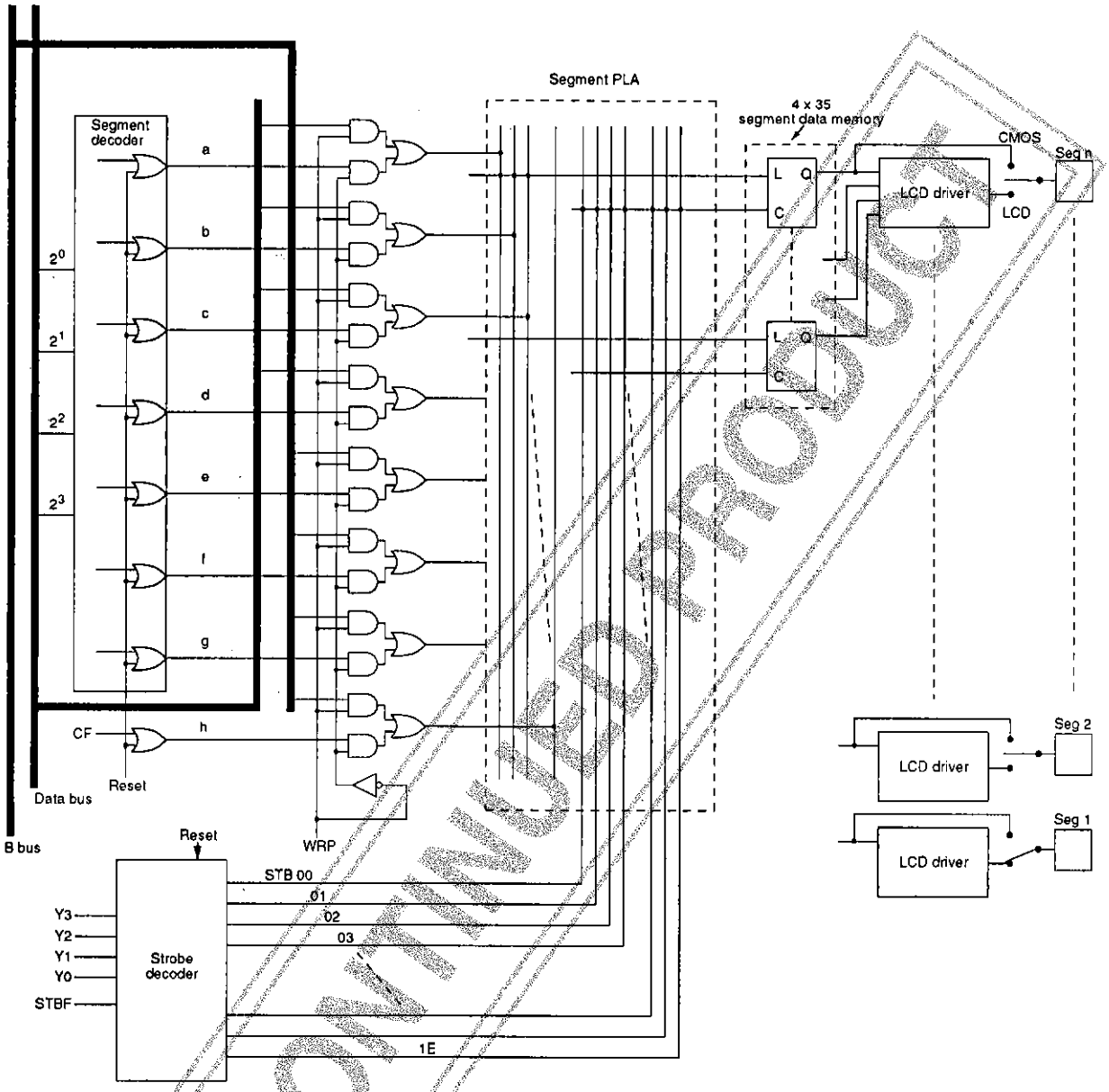


Figure 26. Segment outputs

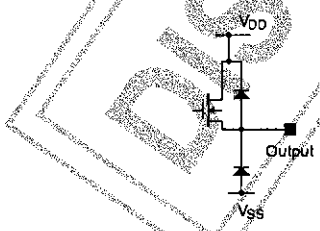


Figure 27. P-channel output option

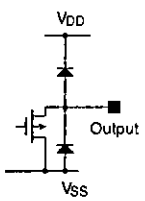


Figure 28. N-channel output option

Display data decoding

Instruction	Data byte	Segment							
		a	b	c	d	e	f	g	h
WRT	0	1	1	1	1	1	1	0	CF
	1	0	1	1	0	0	0	0	CF
	2	1	1	0	1	1	0	1	CF
	3	1	1	1	1	0	0	1	CF
	4	0	1	1	0	0	1	1	CF
	5	1	0	1	1	0	1	1	CF
	6	1	0	1	1	1	1	1	CF
	7	1	1	1	0	0	0	0	CF
	8	1	1	1	1	1	1	1	CF
	9	1	1	1	1	0	1	1	CF
	10	1	0	0	1	1	1	1	CF
	11	1	0	0	1	1	1	1	CF
	12	0	0	0	0	0	0	1	CF
	13	0	0	0	0	0	0	1	CF
	14	0	0	0	0	0	0	0	CF
	15	0	0	0	0	0	0	0	CF
WRP	00 to FF	RAM				Register B			
		Bit0	Bit1	Bit2	Bit3	Bit0	Bit1	Bit2	Bit3

Note
CF = carry flag

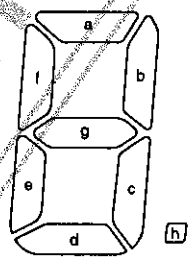


Figure 29. 7-segment character

Common outputs

Duty	COM4	COM3	COM2	COM1	Drive frequency
1/1 duty	Not used	Not used	Not used	Output	32.0 Hz
1/2 duty	Not used	Not used	Output	Output	32.0 Hz
1/3 duty	Not used	Output	Output	Output	42.7 Hz
1/4 duty	Output	Output	Output	Output	32.0 Hz

Bias control

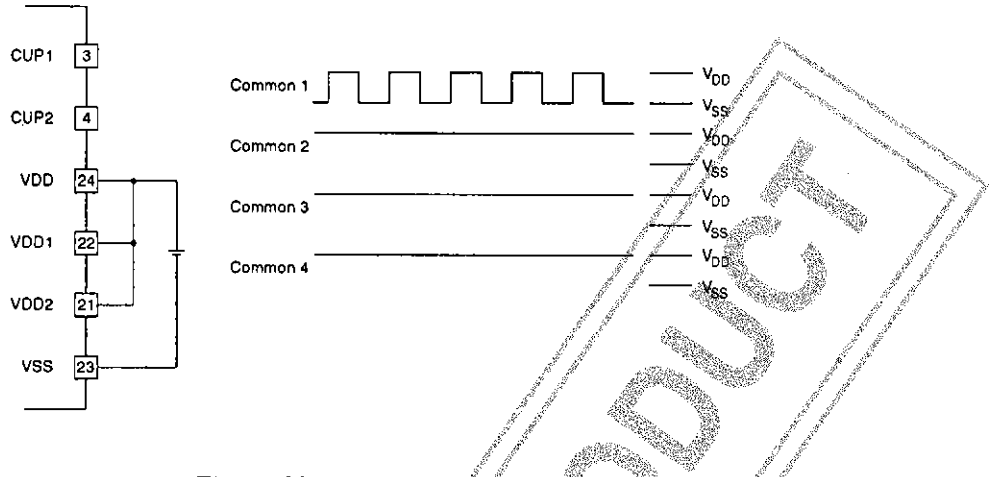


Figure 30. 1/1 bias, 1/1 duty

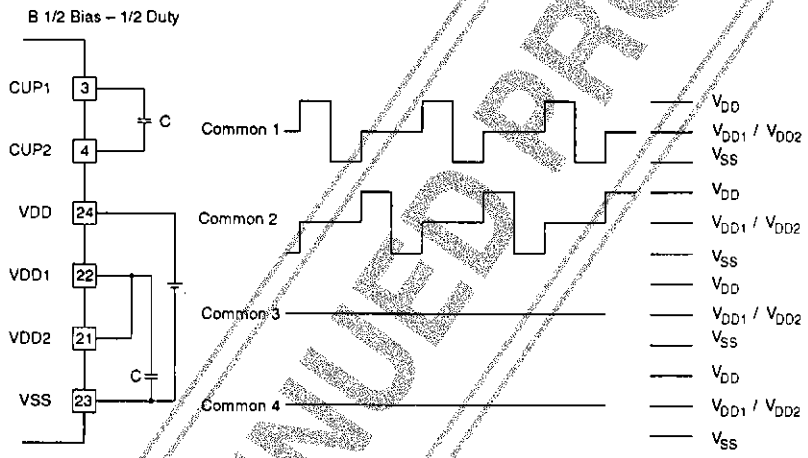


Figure 31. 1/2 bias, 1/2 duty

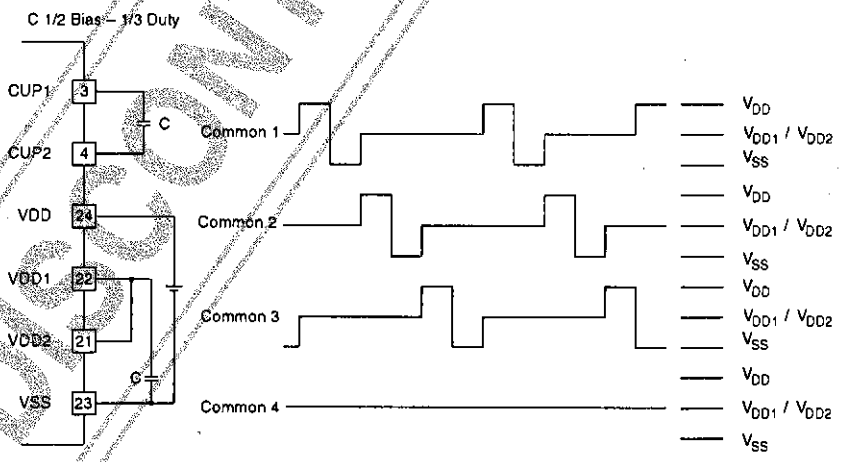


Figure 32. 1/2 bias, 1/3 duty

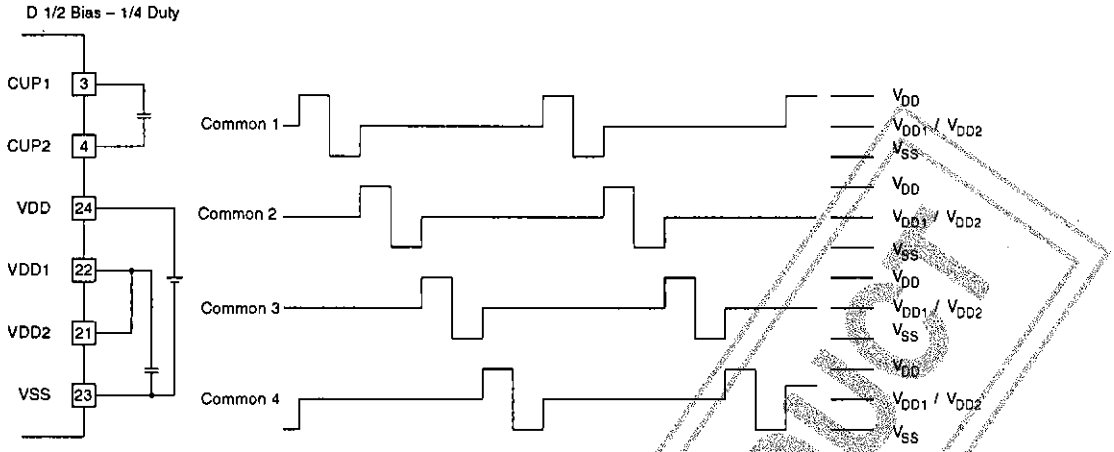


Figure 33. 1/2 bias, 1/4 duty

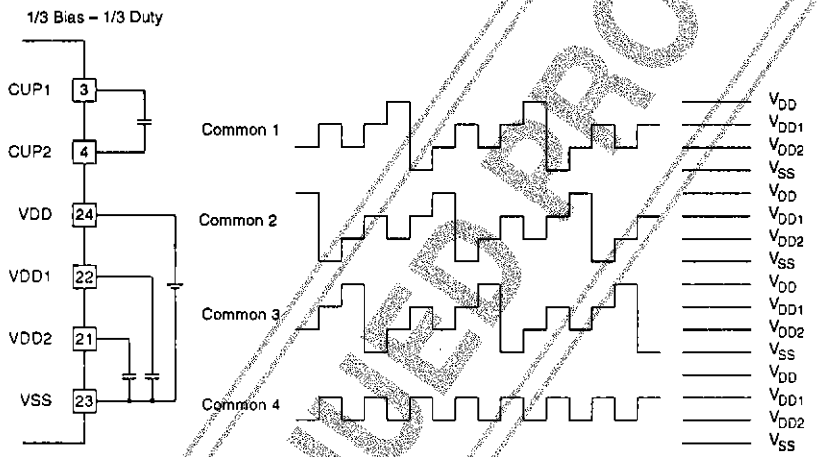


Figure 34. 1/3 bias, 1/3 duty

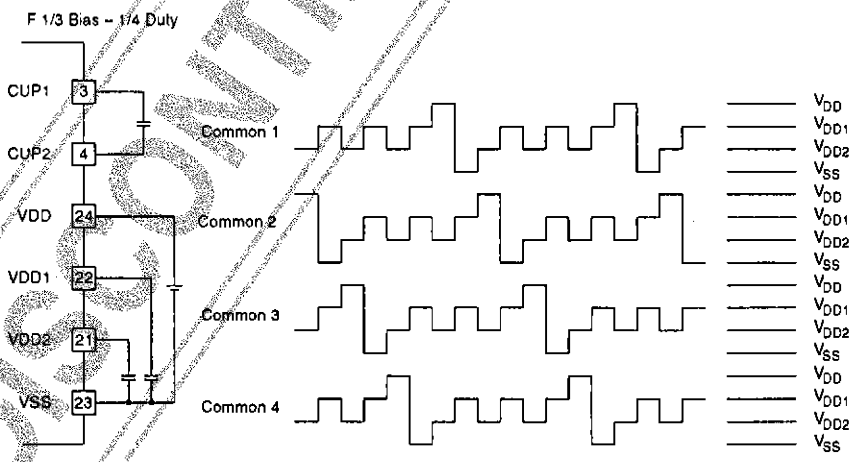
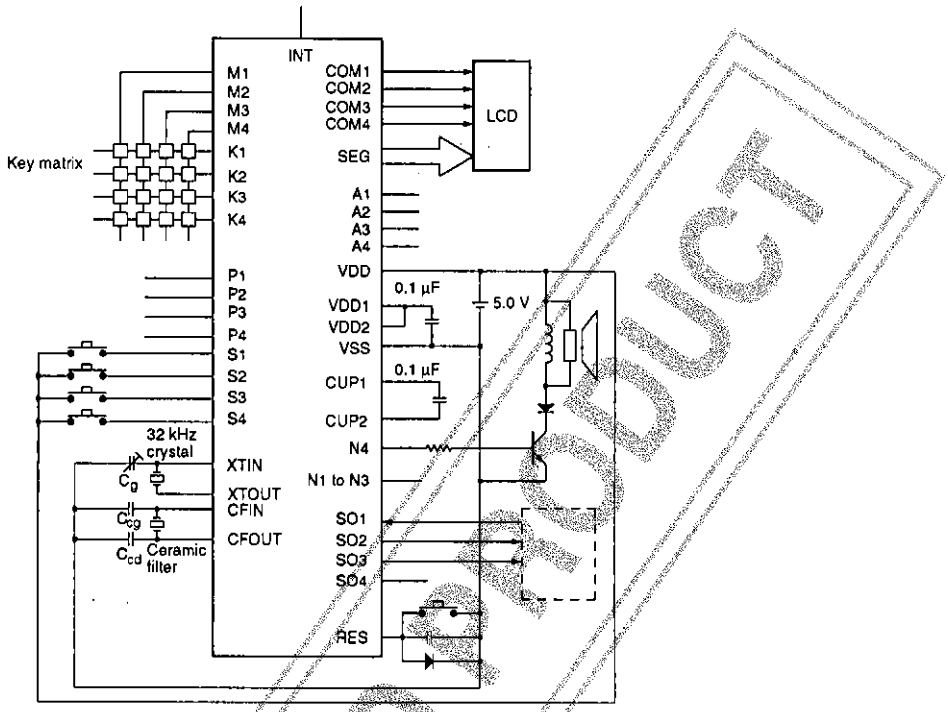


Figure 35. 1/3 bias, 1/4 duty

Typical Application



Design Notes

Resonators

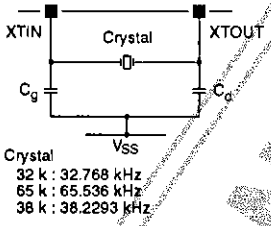


Figure 36. Crystal resonator circuit

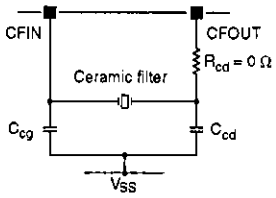


Figure 37. Ceramic filter resonator circuit

Resonator constants

Frequency	Murata			Kyocera		
	Product number	C_{cg} (pF)	C_{cd} (pF)	Product number	C_{cg} (pF)	C_{cd} (pF)
400 kHz	CSB 400P	330	330	KBR-400B	330	330
800 kHz	CSB 800J	220	220	KBR-800H	100	100
1 MHz	CSB 1000J	220	220	KBR-1000H/Y	100	100
2 MHz	CSA 2.00MG CST 2.00MG	33. Built-in	33. Built-in	KBR-2.0MS	33	33
4 MHz	CSA 4.00MG CST 4.00MGW	33. Built-in	33. Built-in	KBR-4.0MSA/MCA KBR-4.0MKS/MWS	33. Built-in	33. Built-in

Crystal oscillator element constants

Frequency	Daishinku		Kyocera	
	Product number	C_g (pF)	Product number	C_g (pF)
32 kHz	DT-38, 32.768kHz	15	KF-38G KF-26G	15 12
65 kHz	DT-381, 65.536kHz	5	KF-38Y	13
38 kHz	DT-381, 38.2293kHz	5	KF-38E	16