

- ◇ STRUCTURE Silicon Monolithic Integrated Circuit
- ◇ PRODUCT Microwire BUS Serial EEPROMs
- ◇ SERIES SIGNATURE SERIES
- ◇ FAMILY BR93C□□ family
- ◇ TYPE Supply voltage 2.5V~5.5V/Operating temperature -40°C~+85°Ctype
- ◇ PART NUMBER BR93C□□-□W□□6TP

PART NUMBER	PACKAGE	DENSITY
BR93C46- WMN6TP	SO8 narrow	1Kbit
BR93C56- WMN6TP		2Kbit
BR93C66- WMN6TP		4Kbit
BR93C76- WMN6TP		8Kbit
BR93C86- WMN6TP		16Kbit
BR93C46-TWMN6TP	SO8 narrow (different pin assignment)	1Kbit
BR93C56-TWMN6TP		2Kbit
BR93C66-TWMN6TP		4Kbit
BR93C76-TWMN6TP		8Kbit
BR93C86-TWMN6TP		16Kbit
BR93C46- WDW6TP	TSSOP8	1Kbit
BR93C56- WDW6TP		2Kbit
BR93C66- WDW6TP		4Kbit
BR93C76- WDW6TP		8Kbit
BR93C86- WDW6TP		16Kbit
BR93C46- WDS6TP	TSSOP8 3 × 3mm ²	1Kbit
BR93C56- WDS6TP		2Kbit
BR93C66- WDS6TP		4Kbit
BR93C76- WDS6TP		8Kbit
BR93C86- WDS6TP		16Kbit

◇ FEATURES

- Microwire BUS interface
- Endurance : 1,000,000 erase/write cycles
- Data retention : 40 years
- Initial Data FFFFh in all address

◇ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
T _{STG}	Storage Temperature	-65	125	°C
V _{OUT}	Output Range(Q=V _{OH} or Hi-Z)	-0.3	V _{CC} +0.3	V
V _{IN}	Input range	-0.3	V _{CC} +0.3	V
V _{CC}	Supply Voltage	-0.3	6.5	V

◇ POWER DISSIPATION (Ta=25°C)

PACKAGE	Rating	Unit
SO8 narrow	450 *1	mW
TSSOP8	330 *2	mW
TSSOP8 3 × 3mm ²	310 *3	mW

* Degradation is done at 4.5mW/°C(*1), 3.3mW/°C(*2), 3.1mW/°C(*3) for operation above 25°C

◇ RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V _{CC}	Supply Voltage	2.5	5.5	V
T _A	Ambient Operating Temperature	-40	85	°C

◇ DC OPERATING CHARACTERISTICS

(Unless otherwise specified, T_a=-40~85°C, V_{CC}=2.5~5.5V)

Parameter	Symbol	Specification			Unit	Test Condition
		Min.	Typ.	Max.		
Input Leakage Current	I _{LI}	-	-	±2.5	μA	0V ≤ V _{IN} ≤ V _{CC}
Output Leakage Current	I _L	-	-	±2.5	μA	0V ≤ V _{OUT} ≤ V _{CC} , Q in Hi-Z
Supply Current (CMOS Inputs)	I _{CC}	-	-	2	mA	V _{CC} =5V, S=V _{BH} , F=2MHz
		-	-	1	mA	V _{CC} =2.5V, S=V _{BH} , F=2MHz
Supply Current(Stand-by)	I _{CC1}	-	-	5	μA	V _{CC} =2.5V, S=V _{SS} , C=V _{SS}
Input Low Voltage(D,C,S)	V _{LI}	-0.3	-	0.2V _{CC}	V	
Input High Voltage(D,C,S)	V _{HI}	0.7V _{CC}	-	V _{CC} +0.3	V	
Output Low Voltage(Q)	V _{OL}	-	-	0.4	V	V _{CC} =5V, I _{OL} =2.1mA
		-	-	0.2	V	V _{CC} =2.5V, I _{OL} =100 μA
Output High Voltage(Q)	V _{OH}	2.4	-	-	V	V _{CC} =5V, I _{OH} =-400 μA
		V _{CC} -0.2	-	-	V	V _{CC} =2.5V, I _{OH} =-100 μA

◇ AC OPERATING CHARACTERISTICS

(Unless otherwise specified, T_a=-40~85°C, V_{CC}=2.5~5.5V)

Parameter	Symbol	Specification			Unit
		Min.	Typ.	Max.	
Clock Frequency	f _C	D.C	-	2	MHz
Chip Select Low to Clock High	t _{SLCH}	50	-	-	ns
Chip Select Set-up Time	t _{SHCH}	50	-	-	ns
Chip Select Low to Chip Select High	t _{SLSH}	200	-	-	ns
Clock High Time	t _{CHCL} *1	200	-	-	ns
Clock Low Time	t _{CLCH} *1	200	-	-	ns
Data In Set-up Time	t _{DVCH}	50	-	-	ns
Data In Hold Time	t _{CHDX}	50	-	-	ns
Clock Set-up Time(relative to S)	t _{CLSH}	50	-	-	ns
Chip Select Hold Time	t _{CLSL}	0	-	-	ns
Chip Select to Ready/Busy Status	t _{SHQV}	-	-	200	ns
Chip Select Low to Output Hi-Z	t _{SLOZ}	-	-	100	ns
Delay to Output Low	t _{CHQL}	-	-	200	ns
Delay to Output Valid	t _{CHQV}	-	-	200	ns
Erase/Write Cycle time	t _w	-	-	5	ms

*1 t_{CHCL}+t_{CLCH} ≥ 1/f_C

◇ BLOCK DIAGRAM

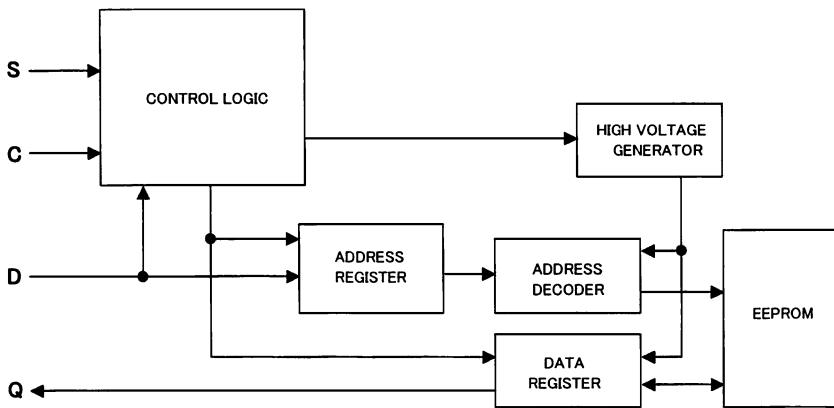


Fig.-1 BLOCK DIAGRAM

◇ PIN No., PIN NAME

PIN No.	PIN NAME	
1	S	DU
2	C	V _{CC}
3	D	S
4	Q	C
5	V _{SS}	D
6	DU	Q
7	DU	V _{SS}
8	V _{CC}	DU
PART NUMBER	BR93C48-WMN6TP	BR93C48-TWMN6TP
	BR93C56-WMN6TP	BR93C56-TWMN6TP
	BR93C66-WMN6TP	BR93C66-TWMN6TP
	BR93C76-WMN6TP	BR93C76-TWMN6TP
	BR93C86-WMN6TP	BR93C86-TWMN6TP
	BR93C46-WDW6TP	
	BR93C56-WDW6TP	
	BR93C66-WDW6TP	
	BR93C76-WDW6TP	
	BR93C86-WDW6TP	
	BR93C46-WDS6TP	
	BR93C56-WDS6TP	
BR93C66-WDS6TP		
BR93C76-WDS6TP		
BR93C86-WDS6TP		

◇ NOTES FOR POWER SUPPLY

This IC has a POR (Power On Reset) circuit as mistake write countermeasure. After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. However, if S is "H" at power ON/OFF, it may become write enable status owing to noises and the likes. For secure operations, observe the following conditions.

1. Set S = "L".
2. Turn on power so as to satisfy the recommended conditions of tR, tOFF, Vbot for POR circuit operation.

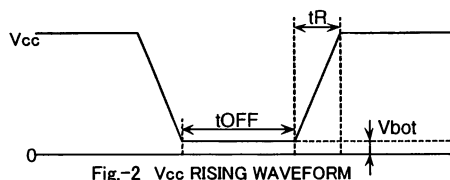


Fig.-2 Vcc RISING WAVEFORM

◇Recommended conditions of tR, tOFF, Vbot

tR	tOFF	Vbot
Below 10ms	Above 10ms	Below 0.3V
Below 100ms	Above 10ms	Below 0.2V

◇CAUTIONS ON USE

(1) Absolute maximum ratings

If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(2) Vss electric potential

Set the voltage of Vss terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of Vss terminal.

(3) Thermal design

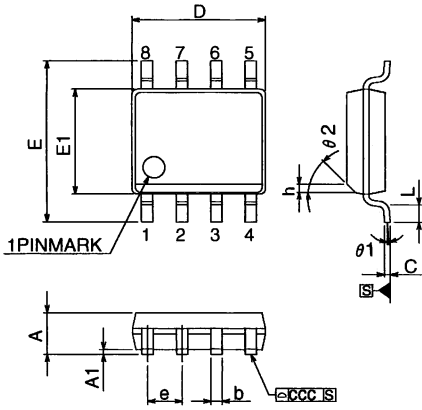
In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.

(4) Terminal to terminal shortcircuit and wrong packaging

When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and Vss owing to foreign matter, LSI may be destructed.

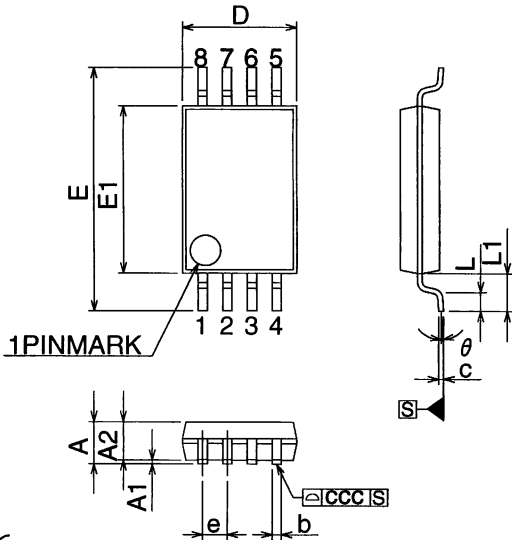
(5) Use in a strong electromagnetic field may cause malfunction, therefore, evaluated design sufficiently.

◇ PHYSICAL DIMENSION



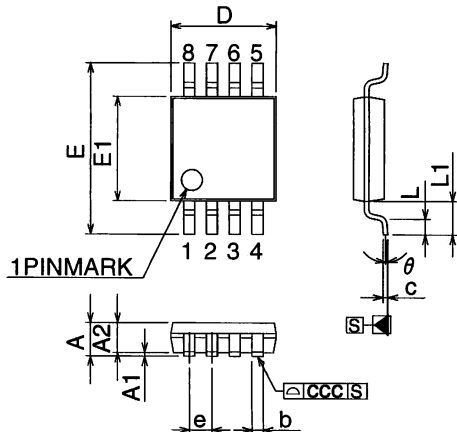
- Notes
- 1.This drawing is subject to change without notice.
 - 2.Body dimensions do not include mold flash or protrusion, or gate burns.
 - 3.Reference JEDEC MS-012 variation AA.

Fig.-3 SO8 narrow Package Outline



- Notes
- 1.This drawing is subject to change without notice.
 - 2.Body dimensions do not include mold flash or protrusion, or gate burns.
 - 3.Reference JEDEC MO-153.

Fig.-4 TSSOP Package Outline



- Notes
- 1.This drawing is subject to change without notice.
 - 2.Body dimensions do not include mold flash or protrusion, or gate burns.
 - 3.Reference JEDEC MO-187 variation AA.

Fig.-5 TSSOP 3 x 3mm² Package Outline

◇ SO8 narrow Package size data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	-	1.35	1.75	-	0.053	0.069
A1	-	0.10	0.25	-	0.004	0.010
b	-	0.33	0.51	-	0.013	0.020
c	-	0.19	0.25	-	0.007	0.010
D	-	4.80	5.00	-	0.189	0.197
e	1.27	-	-	0.05	-	-
E	-	5.80	6.20	-	0.228	0.244
E1	-	3.80	4.00	-	0.150	0.157
L	-	0.40	1.27	0.05	0.016	0.050
theta 1	-	0°	8°	-	0°	8°
ccc	-	-	0.10	-	-	0.004
h	-	0.25	0.50	-	0.010	0.020
theta 2	45°	-	-	45°	-	-

◇ TSSOP8 Package size data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	-	-	1.200	-	-	0.0472
A1	-	0.050	0.150	-	0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b	-	0.190	0.300	-	0.0075	0.0118
c	-	0.090	0.200	-	0.0035	0.0079
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	-	-	0.0256	-	-
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000	-	-	0.0394	-	-
ccc	-	-	0.100	-	-	0.0039
theta	-	0°	8°	-	0°	8°

◇ TSSOP8 3 x 3mm² Package size data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	-	-	1.100	-	-	0.0433
A1	-	0.050	0.150	-	0.0020	0.0059
A2	0.850	0.750	0.950	0.0335	0.0295	0.0374
b	-	0.250	0.400	-	0.0098	0.0157
c	-	0.120	0.230	-	0.0047	0.0091
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	-	-	0.0256	-	-
E	4.900	4.650	5.150	0.1929	0.1831	0.2028
E1	3.000	2.900	3.100	0.1181	0.1142	0.1220
L	0.550	0.400	0.700	0.0217	0.0157	0.0276
L1	0.950	-	-	0.0374	-	-
ccc	-	-	0.100	-	-	0.0039
theta	-	0°	6°	-	0°	6°

Notes

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